ECE 342
Electronic Circuits

Lecture 35
CMOS Logic

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Digital Logic - Generalization

De Morgan's Law

$$\overline{A + B + C + \ldots} = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \ldots$$

$$\overline{A \cdot B \cdot C \cdot \ldots} = \bar{A} + \bar{B} + \bar{C} + \ldots$$

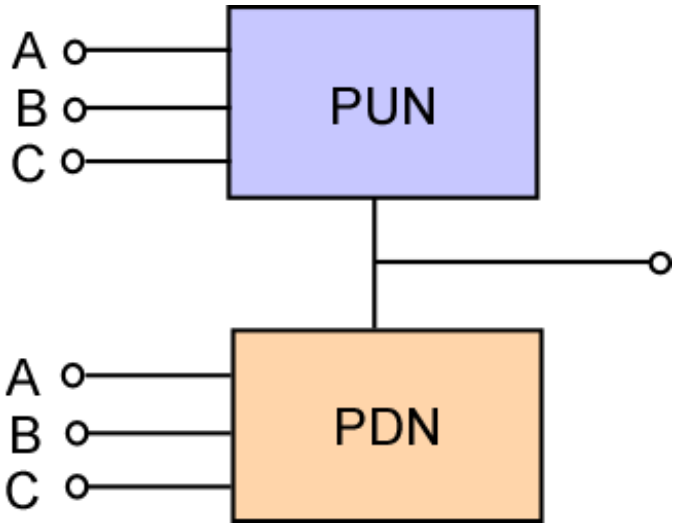
Distributive Law

$$AB + AC + BC + BD = A(B + C) + B(C + D)$$

- **General Procedure**
  1. Design PDN to satisfy logic function
  2. Construct PUN to be complementary of PDN in every way
  3. Optimize using distributive rule

CMOS Logic Gate Circuits

- **Two Networks**
  - Pull-down network (PDN) with NMOS
  - Pull-up network (PUN) with PMOS

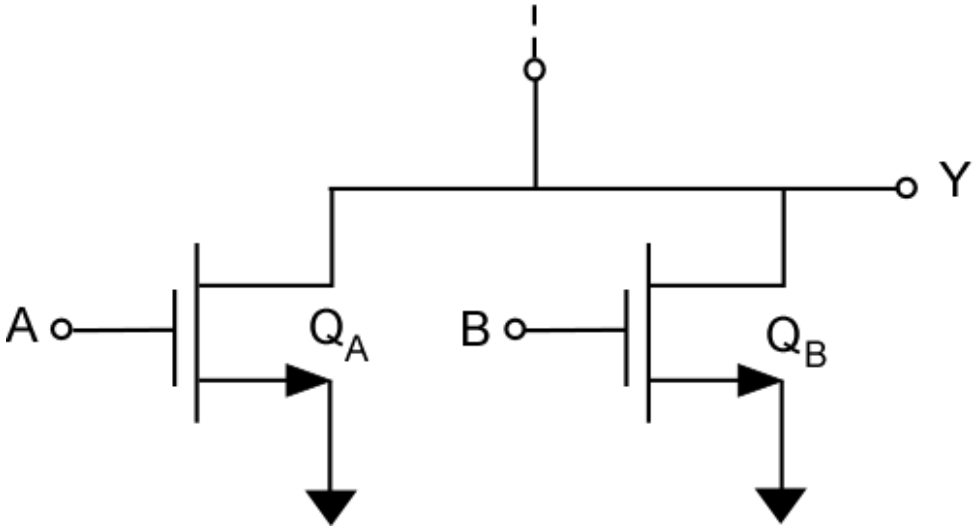


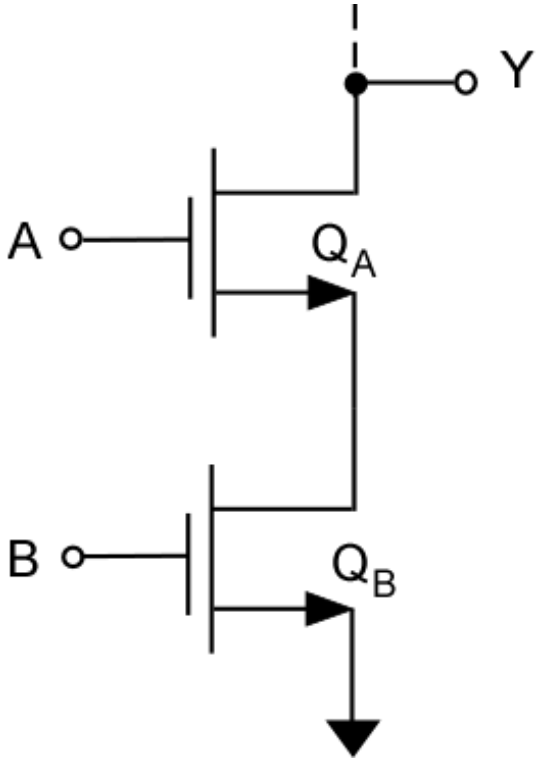
PUN conducts when inputs are low and consists of PMOS transistors

PDN consists of NMOS transistors and is active when inputs are high

- **PDN and PUN utilize devices**
  - In parallel to form OR functions
  - In series to form AND functions

Pull-Down Networks

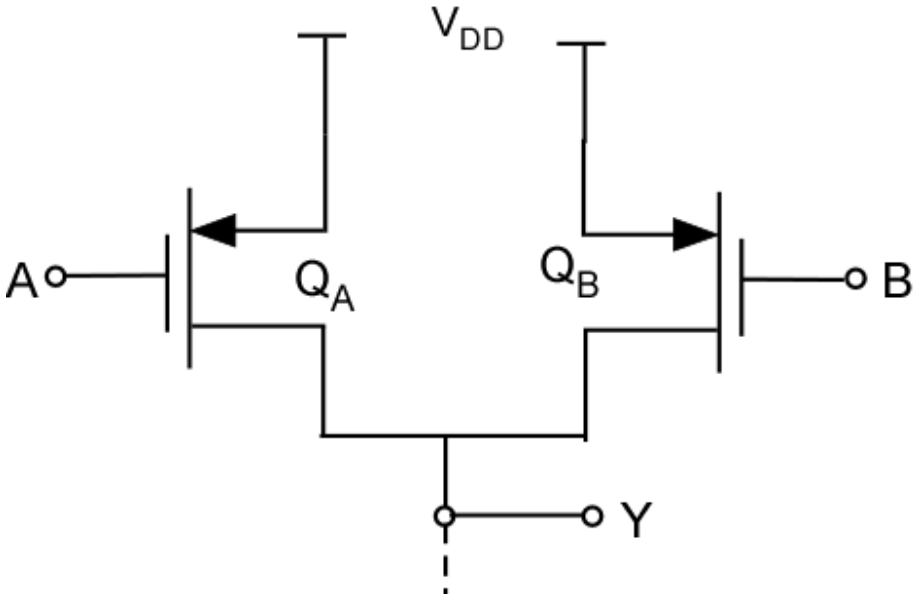




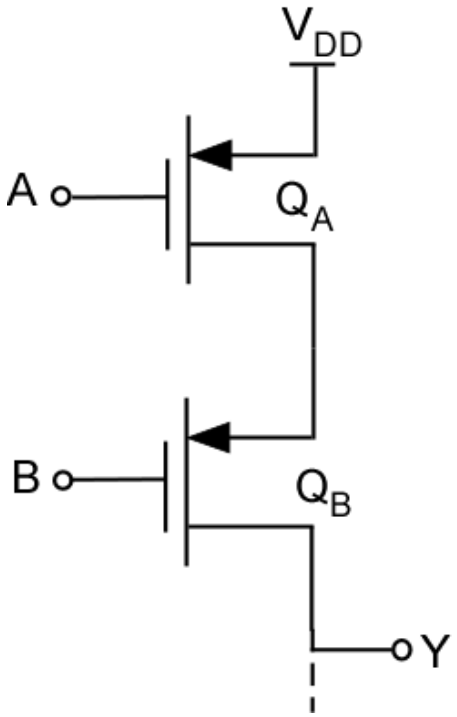
$$\overline{Y} = A + B$$

$$\overline{Y} = AB$$

Pull-Up Networks

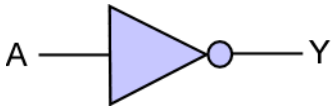
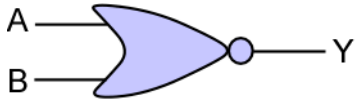
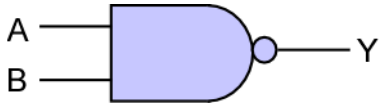
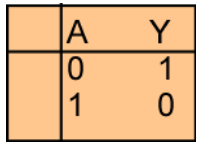
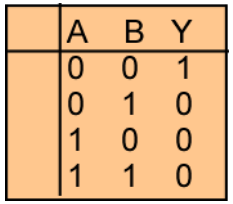
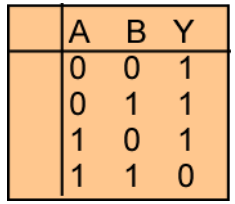


$$Y = \overline{A} + \overline{B}$$



$$Y = \overline{A}\,\overline{B}$$

Basic Logic Function

Basic Function	INVERTER	NOR	NAND
Symbol			
# Devices PUN	1 PMOS	2 PMOS-Series	2 PMOS-Parallel
# Devices PDN	1 NMOS	2 NMOS-Parallel	2 NMOS-Series
Truth Table			

A	Y
0	1
1	0

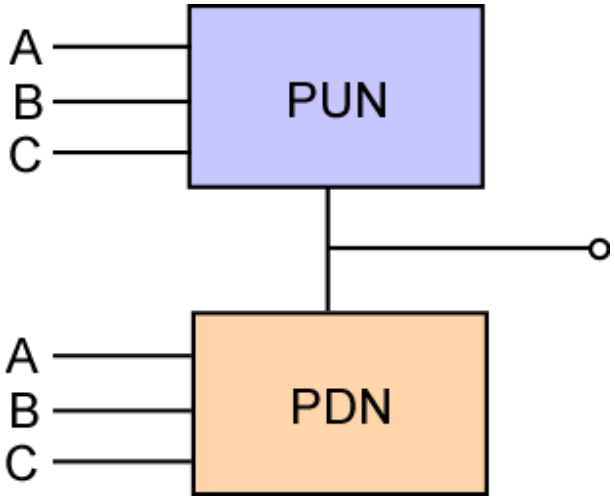
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Pull-Down and Pull-Up Functions

Pull-up network (PUN)

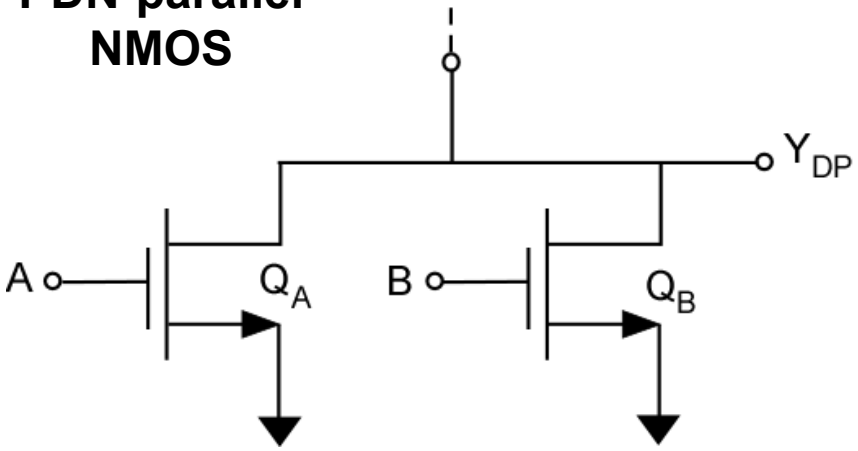
Pull-down network (PDN)



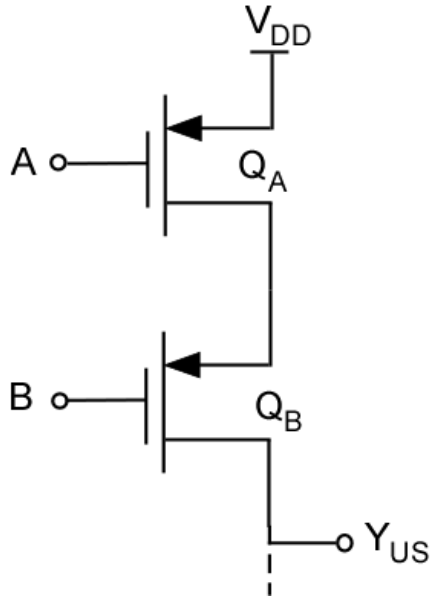
- **Key features**
  - When PDN switch is on, PUN switch is off and vice versa
  - Conditions for being on and off are complementary

Pull-Down and Pull-Up

PDN-parallel NMOS



PUN-series PMOS



Truth Tables

$$Y_{DP} = \overline{A + B}$$

A	B	Y_{DP}
0	0	1
0	1	0
1	0	0
1	1	0

$$Y_{US} = \overline{A}\,\overline{B}$$

A	B	Y_{US}
0	0	1
0	1	0
1	0	0
1	1	0

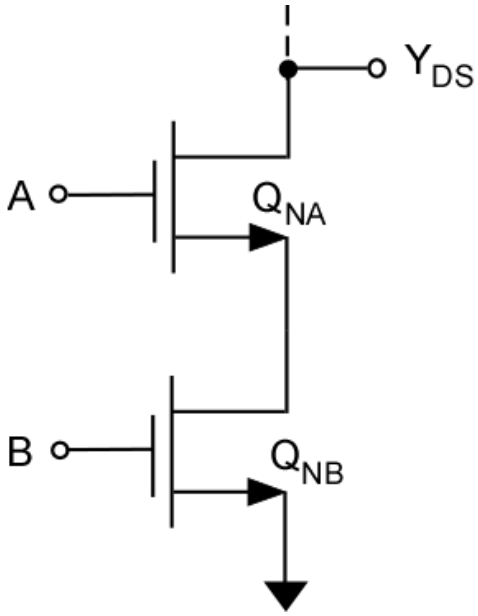
Pull-Down and Pull-Up

When Y_{DP} in PDN-parallel is low, this means that either A or B (or both) is high. When either A or B (or both) is high, either transistor (or both) in PUN-series are off➔Y_{US}=low

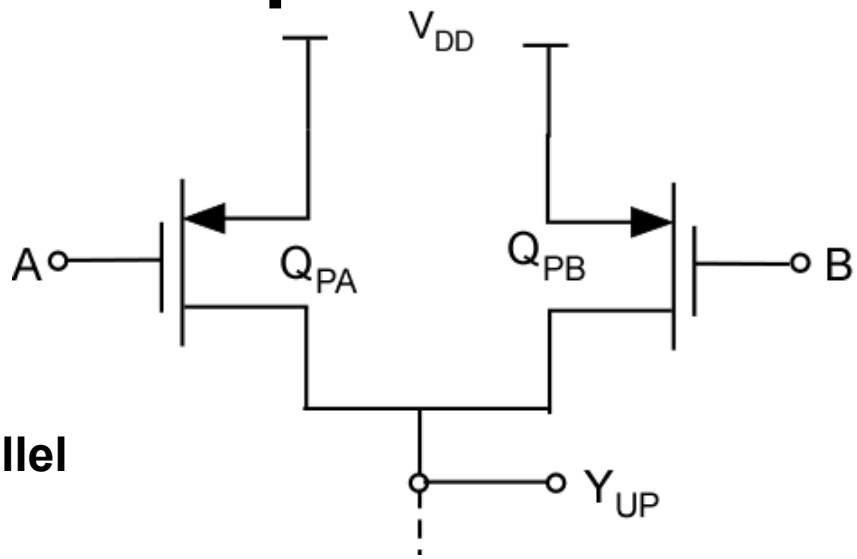
When Y_{DP} in PDN-parallel is high, both A and B are low. Both transistors in PUN-Series are on creating a path to VDD. Y_{US}=high➔Y_{US}=Y_{DP}.

PDN-Parallel and PUN-series are complementary

Pull-Down and Pull-Up



PDN-Series
NMOS



PUN-Parallel
PMOS

Truth Tables

$$Y_{DS} = A\overline{B}$$

A	B	Y_{DS}
0	0	1
0	1	1
1	0	1
1	1	0

$$Y_{UP} = \overline{A} + \overline{B}$$

A	B	Y_{UP}
0	0	1
0	1	1
1	0	1
1	1	0

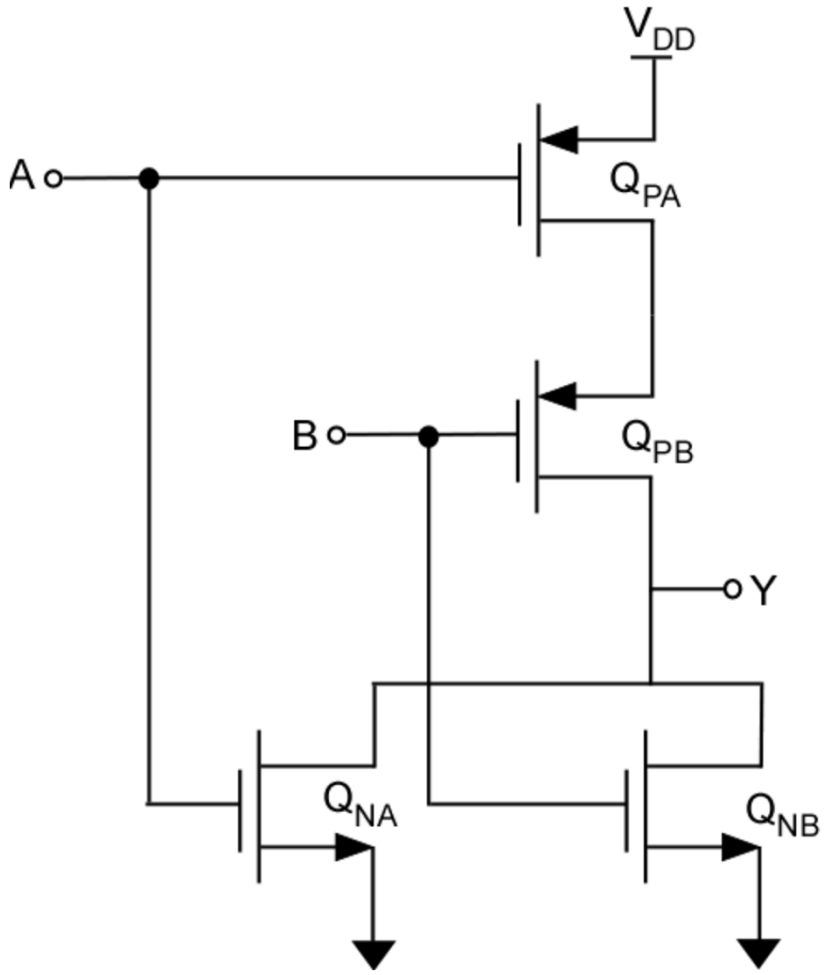
Pull-Down and Pull-Up

If Y_{DS} is low, both A and B must be high in which case both transistors in PUN-Parallel are off providing no path to V_{DD} → Y_{UP}=low → Y_{UP}=Y_{DS}.

If Y_{DS} is high, then either A or B (or both) are off (low) in which case either Q_{PA} or Q_{PB} in PUN-Parallel will be on and present a path to V_{DD}; thus Y_{UP}=high → Y_{UP}=Y_{DS}

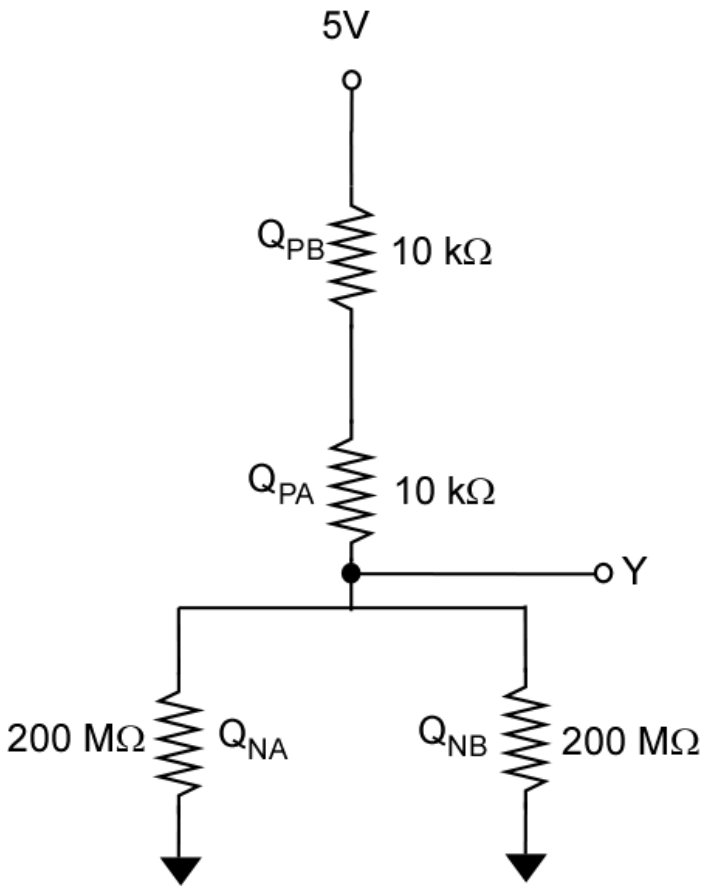
PDN-Series and PUN-Parallel are complementary

Two-Input NOR Gate

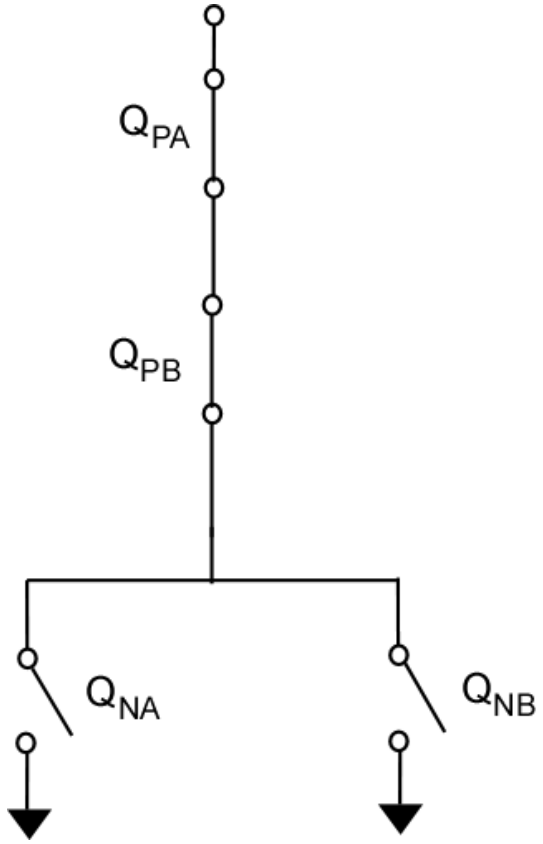


$$Y = \overline{A + B} = \bar{A}\bar{B}$$

Two-Input NOR Gate

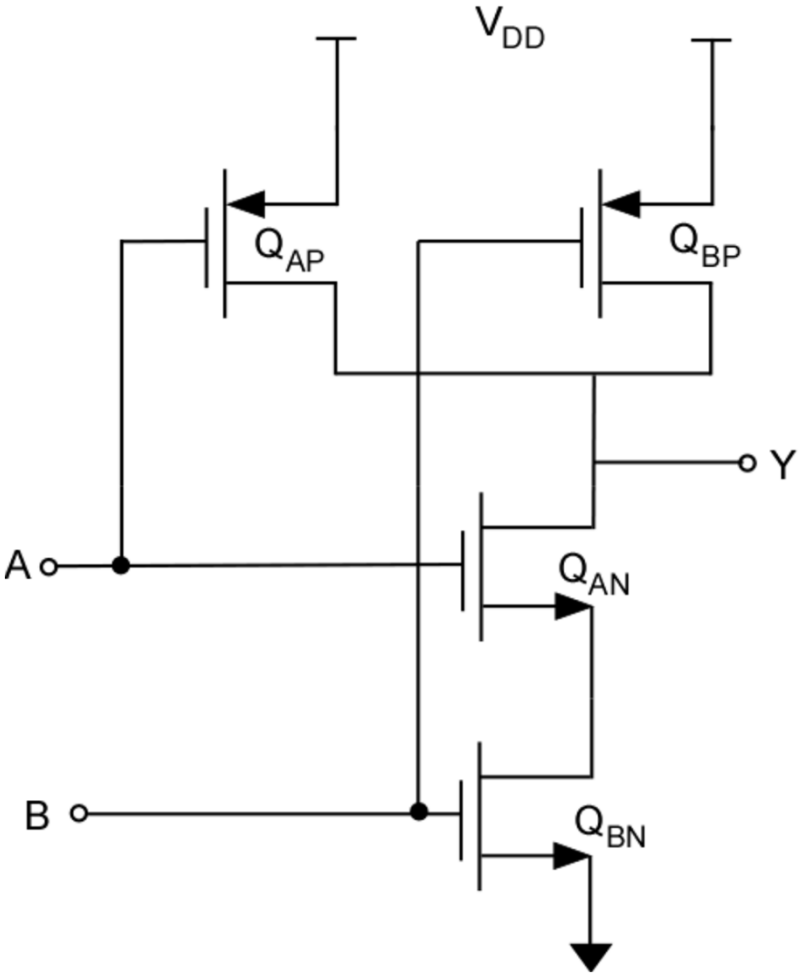


Actual



Ideal

Two-Input NAND Gate



$$Y = \overline{AB} = \overline{A} + \overline{B}$$

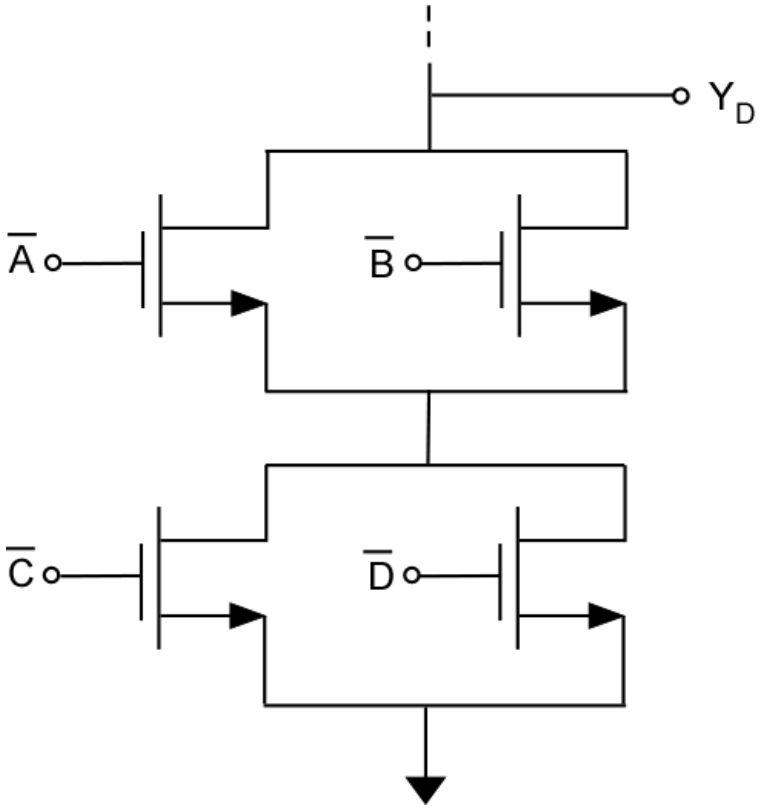
Example

$$Y = \overline{A\overline{B} \cdot \overline{C\overline{D}}}$$

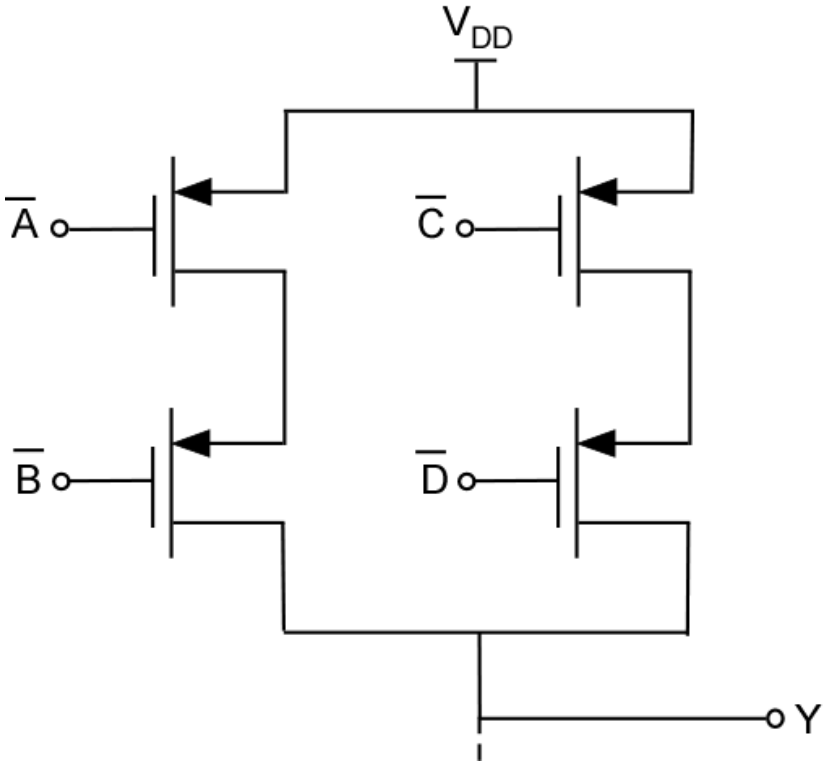
Using De Morgan's Law

$$Y = \overline{A\overline{B} \cdot \overline{C\overline{D}}} = AB + CD = \overline{(\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})}$$

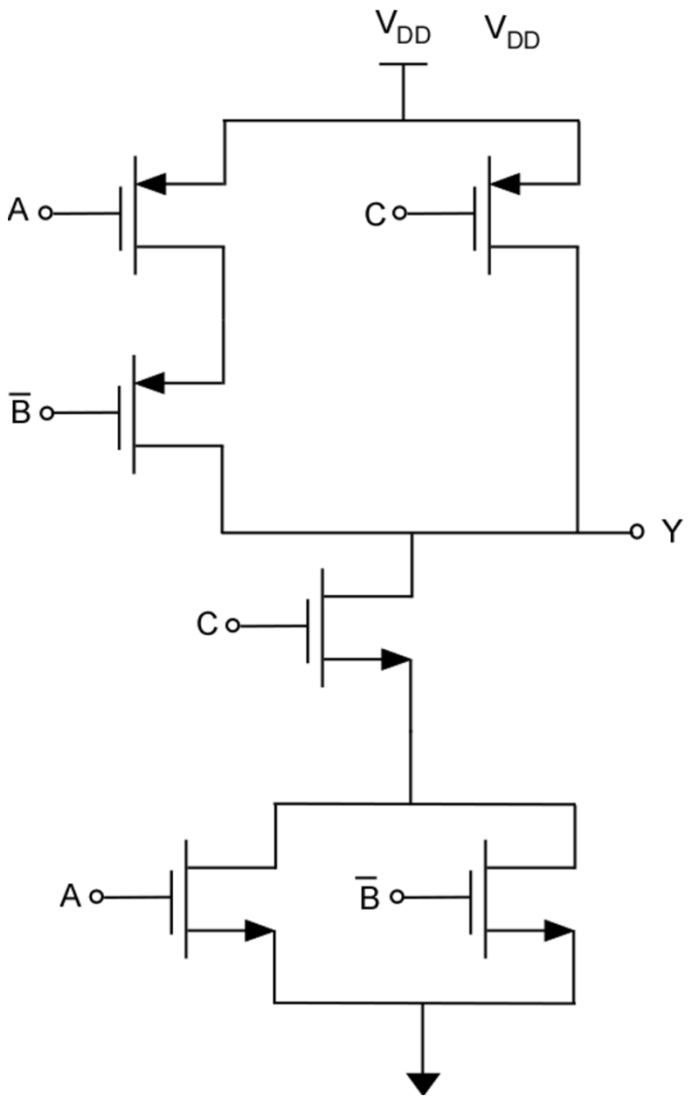
Pull-down network



Pull-up network



Example 1



Evaluate Logic Function

$$Y = \overline{(A + \overline{B})C}$$ from pull down

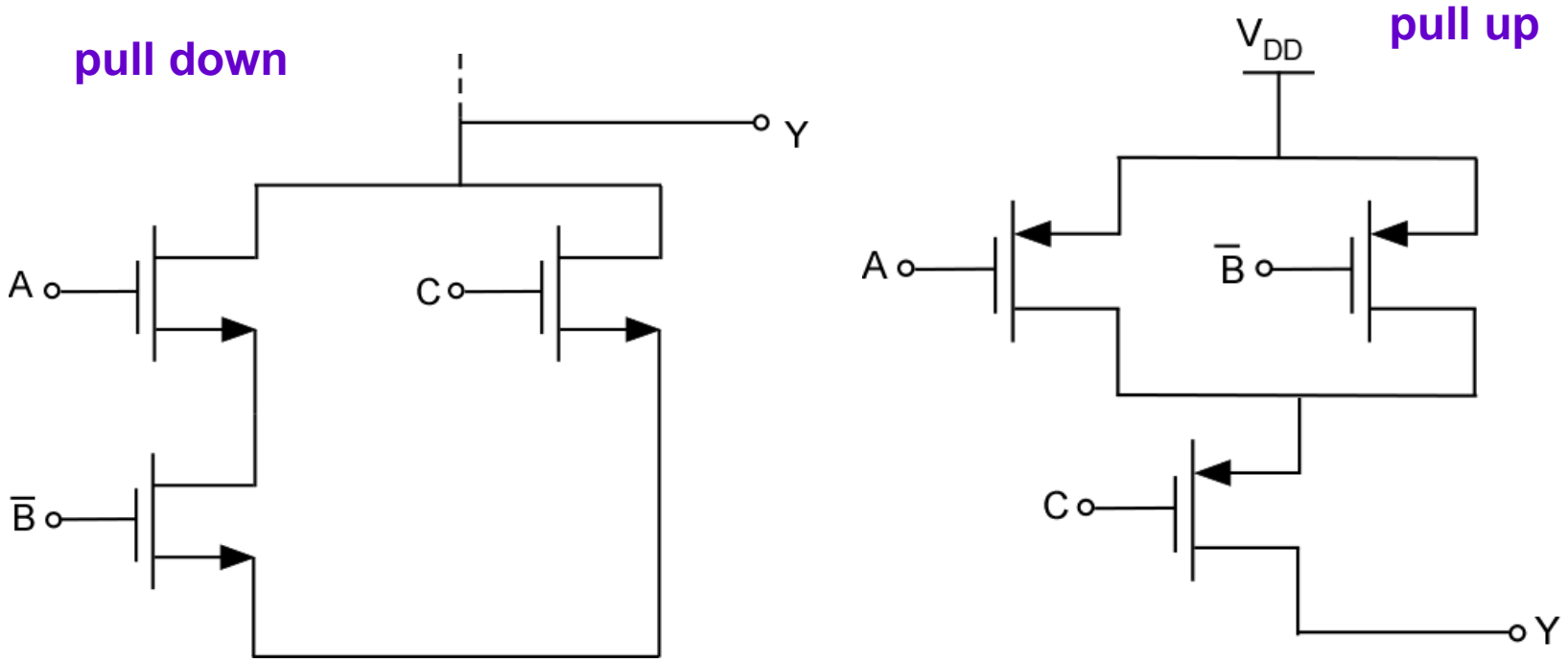
$$Y = \overline{A}B + \overline{C}$$ from pull up

$$\overline{A}B + \overline{C} = \overline{\overline{\overline{A}B} \cdot C} = \overline{(A + \overline{B})C}$$

Example 2

Implement the function

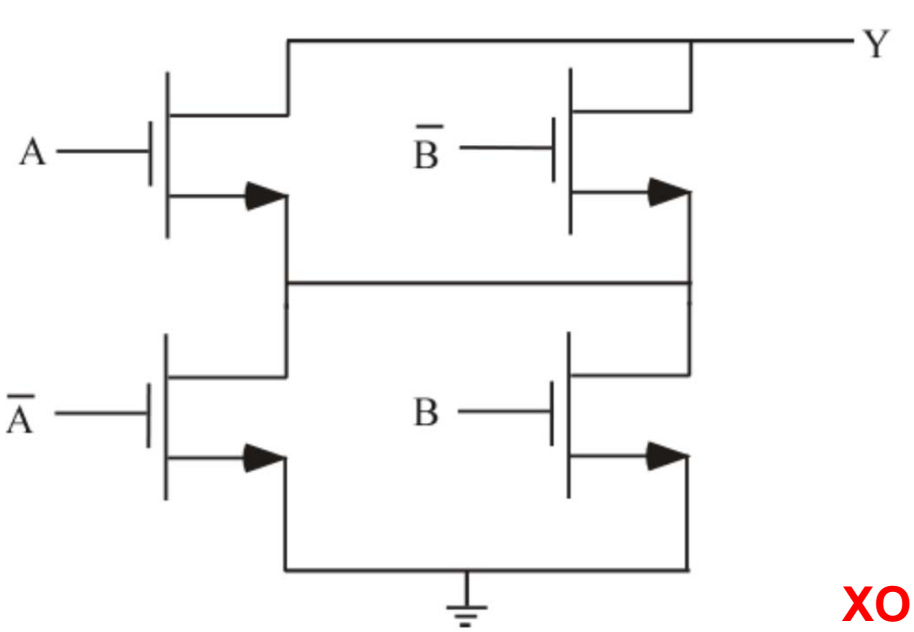
$$\overline{Y} = A\overline{B} + C$$

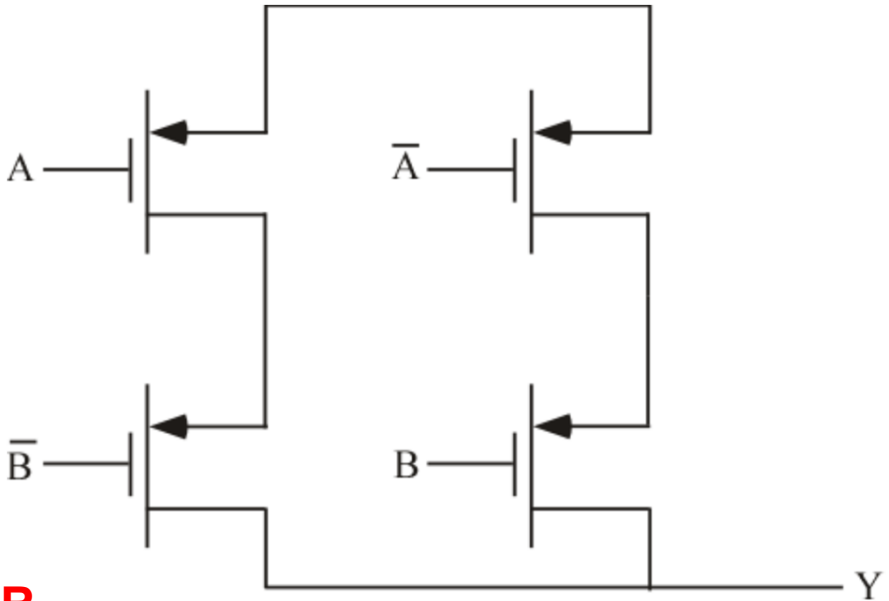


$$Y = \overline{A\overline{B} + C} = \overline{A\overline{B}} \cdot \overline{C} = (\overline{A} + B) \cdot \overline{C}$$

Exclusive-OR (XOR) Function

$$Y = A\overline{B} + \overline{A}B \qquad \overline{Y} = (\overline{A} + B)(A + \overline{B})$$





pull down

pull up

XOR

	A	B	Y
	0	0	0
	0	1	1
	1	0	1
	1	1	0

Transistor Sizing

Objectives

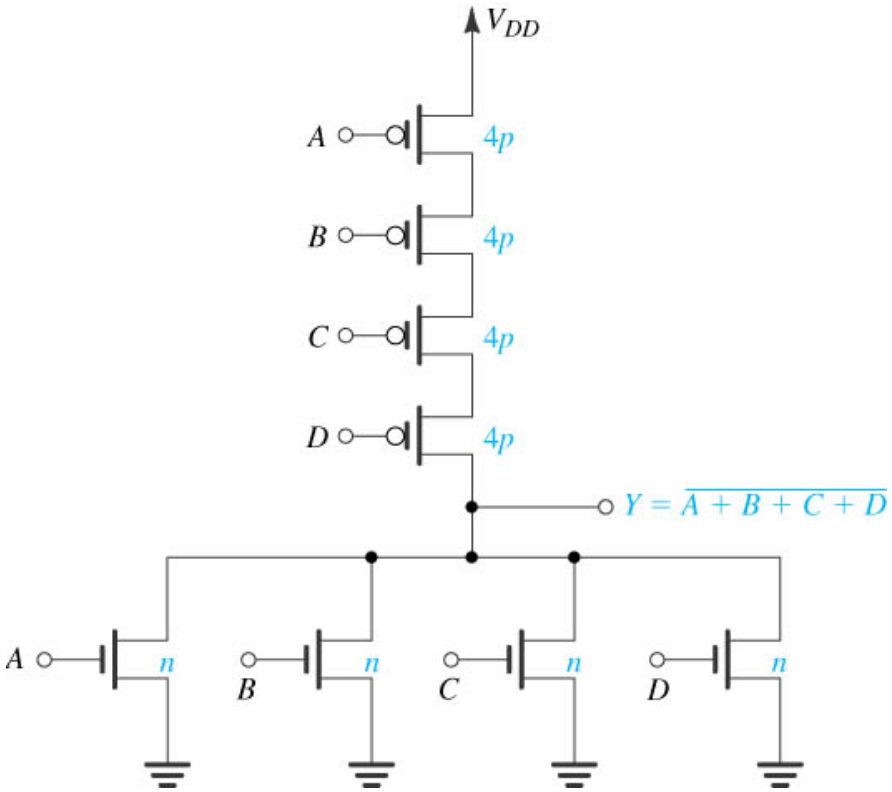
- PDN provides discharge current of at least that of an NMOS
- PUN provides charging current of at least that of a PMOS
- Worst case gate delay equal to that of basic inverter
- Find combination that results in lowest output current
- For transistors in parallel aspect ratios add
- For transistors in series, inverses of aspect ratios add

$$Series: \frac{1}{(W/L)_{eq}} = \frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \ldots + \frac{1}{(W/L)_M}$$

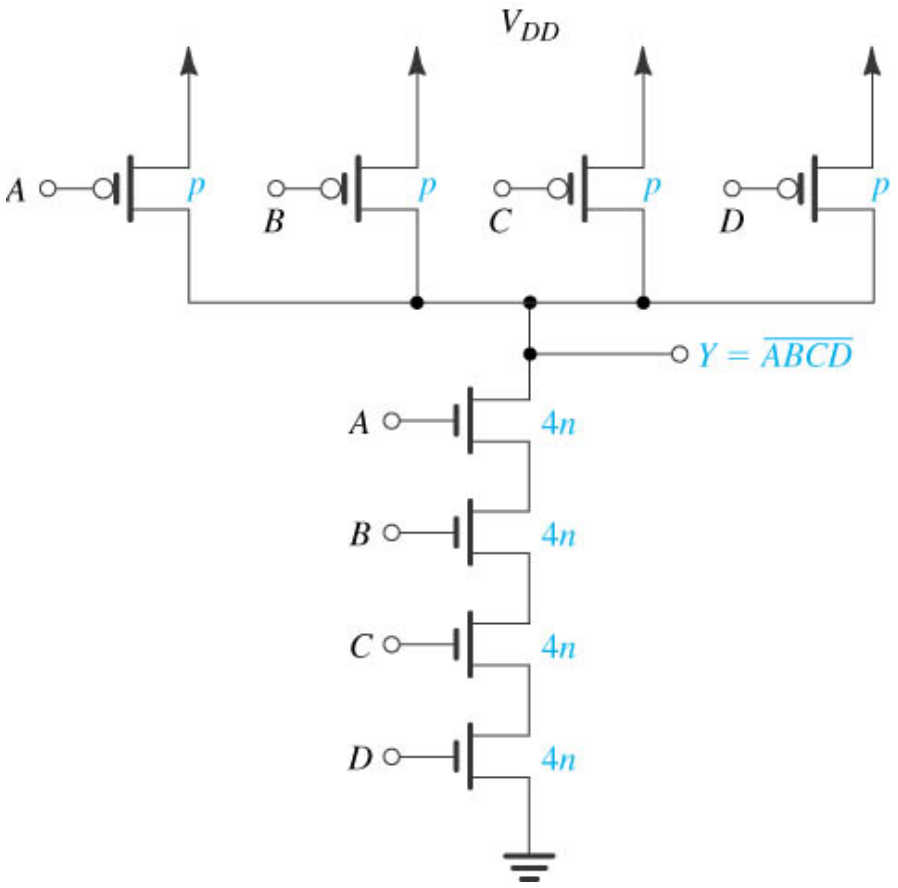
$$Parallel: (W/L)_{eq} = (W/L)_1 + (W/L)_2 + \ldots + (W/L)_M$$

$$p = (W/L)_p \qquad n = (W/L)_n$$

Transistor Sizing



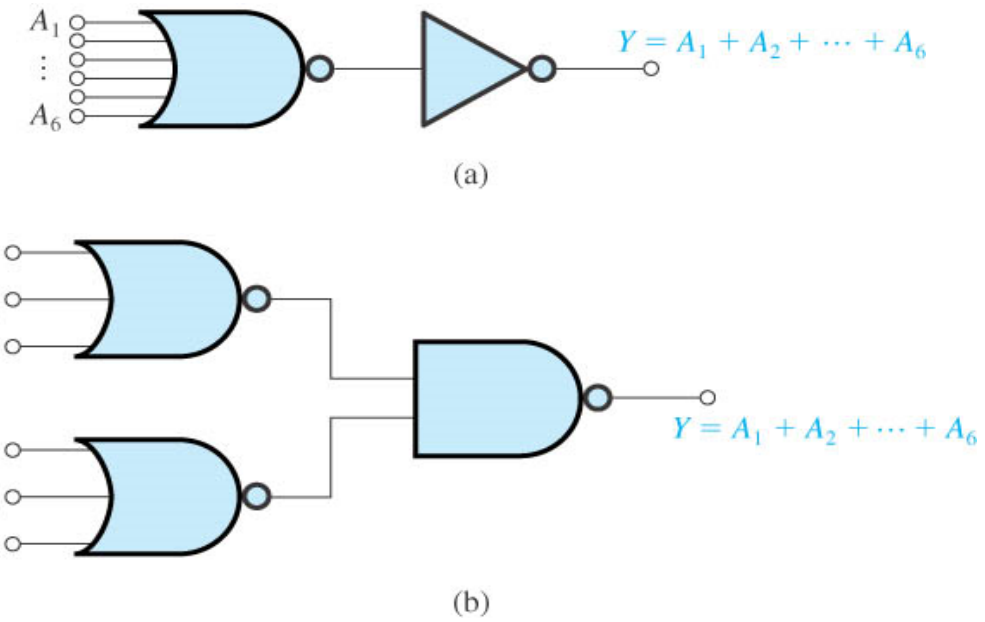
NOR



NAND

Transistor Sizing – Example 1

Two approaches to realizing the OR function of six input variables. Assuming that the transistors in both circuits are properly sized to provide each gate with a current-driving capability equal to that of the basic matched inverter, find the number of transistors and the total area of each circuit. Assume the basic inverter to have a $(W/L)_n$ ratio of 1.2 μm/0.8 μm and a $(W/L)_p$ ratio of 3.6 μm/0.8 μm.



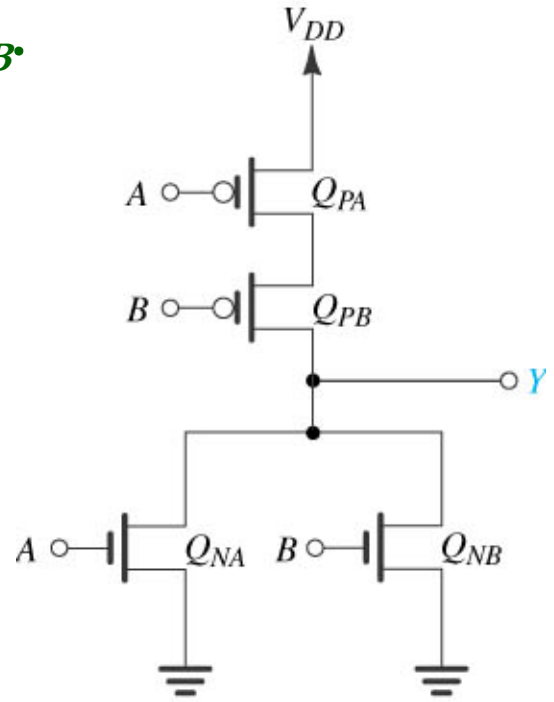
Transistor Sizing – Example 1

For design (a), there are 2(6)+2=14 transistors:
All 7 NMOS use $(W/L)_n = n$
1 PMOS uses $(W/L)_p = p$
6 PMOS use $(W/L)_p = 6p$
Total Area = 7(1.2)0.8+ 1(3.6)0.8 + 6(6)(3.6)0.8 = 113.3 μm^2

For design (b), there are 2(3)2 + 1(2)2=16 transistors:
6 NMOS use $(W/L)_n = n$
6 PMOS use $(W/L)_p = 3p$
2 PMOS use $(W/L)_p = p$
2 NMOS use $(W/L)_n = 2n$
Total Area = 70(1.2)0.8 = 67.2 μm^2, or 59% of (a)

Transistor Sizing – Example 2

Transistors in two-input NOR gate are properly sized so that the current-driving capability in each direction is equal to that of a matched inverter. For $|V_t| = 1$ V and $V_{DD} = 5$ V, find the gate threshold in the cases for which (a) input terminal A is connected to ground and (b) the two input terminals are tied together. Neglect the body effect in Q_{PB}.



$Y = \overline{A + B}$

Transistor Sizing – Example 2

Corresponding to a matched inverter characterized by n and p where $k_p = k_n = k$, the two-input NOR uses transistors n and $2p$ where $k_p = 2k_n$

a) For A grounded, V_{thB} occurs near $V_{DD}/2$, with Q_{PB} and Q_{NB} in saturation and Q_{PA} in triode. Let $V_{th} = v$, and the voltage across Q_{PA} be x

$$\text{Thus } i_D = k_p\left[(5-1)x - x^2/2\right]$$

$$\text{and } i_D = \frac{1}{2}k_p(5-x-v-1)^2$$

$$\text{and } i_D = \frac{1}{2}k_n(v-1)^2$$

Transistor Sizing – Example 2

$$\text{For } k_p = 2k_n,\ i_D = 2k_n\left(4x - x^2/2\right) = k_n\left(8x - x^2\right) \qquad (1)$$

$$\text{and} \quad i_D = k_n\left(4 - x - v\right) \qquad (2)$$

$$\text{and} \quad i_D = \frac{1}{2}k_n\left(v - 1\right)^2 \qquad (3)$$

$$\text{From 2) 3):} \quad \pm\left(v-1\right)\left(0.07\right) = 4 - x - v$$

$$\text{Thus, } 1.707v = 4.707 - x \Rightarrow x = 4.707 - 1.707v$$

$$\text{or, } \quad 0.293v = 3.293 - x \Rightarrow x = 3.293 - 0.293v$$

Transistor Sizing – Example 2

Now $x \approx 0$, in which case, $v = 4.707 / 1.707 \approx 2.38$ (ok)

or $v = 3.293 / 0.293 \approx 11.2$ (Clearly too large)

$$\text{Thus, } x = 4.707 - 1.707v \qquad (4)$$

$$\text{Now from 1) 3) : } (v-1)^2 = 2\left(8x - x^2\right)$$

$$\text{With 4), } v^2 - 2v + 1 = 16\left(4.707 - 1.707v\right) - 2\left(4.707 - 1.707\right)^2$$

$$\text{or } v^2 - 2v + 1 = 75.32 - 27.3v - 44.31 + 3213v - 5.83v^2$$

$$\text{or } 6.83v^2 + v\left(-2 + 27.32 - 32.13\right) + \left(1 - 75.32 + 44.31\right) = 0$$

$$\text{or } 6.83v^2 + 6.81v - 30.01 = 0$$

Transistor Sizing – Example 2

$$\text{whence } v = \left(--6.81 \pm \left(6.81^2 - 4(6.83)30.01 \right)^{1/2} \right) / 2(6.83) \quad (1)$$

$$= (6.81 \pm 29.43) / 13.66 = 2.65V$$

Check: $[> 2.5$ V probably ok since one PMOS is full on$]$

Thus $V_{th} = 2.65V$

b) For A and B joined, the PMOS can be approximated as a single device with twice the length, for which the width is twice that in a matched inverter. Thus, for the equivalent PMOS device, $(W/L)_{peq} = p$ and $k_p = k$. For each of the two NMOS, $(W/L)_n = n$ and $k_n = k$.

Thus, at $V_{th} = v$ with all devices in saturation:

$$i_D = 2\frac{k}{2}(v-1)^2 = \frac{k}{2}(5-v-1)^2$$

Transistor Sizing – Example 2

$$2(v-1)^2 = (4-v)^2, \; and \; \pm\sqrt{2}(v-1) = (4-v)$$

$$\text{Thus } 1.414v - 1.414 = 4 - v, \;\; 2.414v = 5.414$$

$$\text{whence } V_{th} = v = 2.24V$$

See this is reduced from the single-input value (of 2.65V)!

Note that this fact can be used to control the relative threshold of multiple gates connected to a single fan-out node, in order to guarantee operation sequence for slowly changing signals