1. Consider the classical biasing scheme shown, using a 15 V supply. For the MOSFET, $V_t = 1.2\text{V}$, $\lambda = 0$, $k_n' = 80 \, \mu\text{A/V}^2$, $W = 240 \, \mu\text{m}$, and $L = 6 \, \mu\text{m}$. Arrange that the drain current is 2 mA, with about one-third of the supply voltage across each of $R_S$ and $R_D$. Use 22 M$\Omega$ for the larger of $R_{G1}$ and $R_{G2}$. What are the values of $R_{G1}$, $R_{G2}$, $R_S$, and $R_D$ that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of saturation?

2. Given $\mu_n C_\text{ox} = 0.1\text{mA/V}^2$ and $V_t = 1\text{V}$ Determine the current $I_B$ in the circuits shown in figure below. Note that the fractions next to transistors represent $W/L$.

3. An enhancement NMOS transistor is connected in the bias circuit shown, with $V_G = 4\text{V}$ and $R_S = 1 \, \text{k}\Omega$. The transistor has $V_t = 2\text{V}$ and $k_n'(W/L) = 2 \, \text{mA/V}^2$. What bias current results? If a
transistor for which \( k_n' (W/L) \) is 50% higher is used, what is the resulting percentage increase in \( I_D \)?

4. Design the circuit shown below so that the transistor operates in saturation with \( V_D \) biased 1 V from the edge of the triode region, with \( I_D = 1 \) mA and \( V_D = 3 \) V for each of the following two devices (use a 10-\( \mu \)A current in the voltage divider):

(a) \(|V_t| = 1 \) V and \( k_p' W/L = 0.5 \) mA/V^2

(b) \(|V_t| = 2 \) V and \( k_p' W/L = 1.25 \) mA/V^2

For each case, specify the values of \( V_G, V_D, V_S, R_1, R_2, R_S \) and \( R_D \).
5. In the circuit below, find the unknown node voltages $V_1$ and $V_2$, given $V_{tp} = -1 \text{V}$, $k' W/L = 1 \text{mA/V}^2$, and $\lambda = 0$ for all transistors.