1. Using incremental model, derive the expression for equivalent impedance of the configurations shown below. You may assume all transistors are biased in saturation region and $r_{ds} \neq \infty$.

(a) \[ \frac{R_G}{R_{eq}} \]
(b) \[ V_B \]
(c) \[ R_G \]
(d) \[ R_{eq} \]
(e) \[ V_B \]
(f) \[ R_D \]
(g) \[ R_S \]

2. Using the results from Problem 1, determine the equivalent impedance for the configurations shown below. You may assume all transistors are biased in saturation region and $r_{ds} \neq \infty$.

(a) \[ I_B \]
(b) \[ R_{eq} \]
(c) \[ R \]
(d) \[ R_{eq} \]
(e) \[ M_1 \]