Common-source Amplifier

Consider an NMOS in SAT. The DC voltages, DC current, and bias circuitry is not shown.

This figure represents the core concept of a CS amplifier. Only small-signal quantities are shown. Real (complete) CS amplifier circuit will include DC bias circuitry, coupling and bypass capacitors, external load, signal input source. These will all strive to ensure that:

1) transistor is in SAT over the entire range of operation.

2) the input \( \nu_{gs} \) "sees" as much of the input signal source \( \nu_i \).

3) the output \( \nu_o \) "sees" as much of the \( \nu_{ds} \) signal.
The small-signal current \( i_d \) is given by:

\[
l_d = g_m v_{gs} + \frac{v_{ds}}{r_{ds}} = g_m v_i + \frac{v_o}{r_{ds}} \tag{1}
\]

Also,

\[
v_o = -R_D \cdot l_d \tag{2}
\]

Substituting (1) into (2)

\[
v_o = -R_D \left[ g_m v_i + \frac{v_o}{r_{ds}} \right] \]

\[
\Rightarrow v_o \left[ 1 + \frac{R_D}{r_{ds}} \right] = -g_m R_D v_i
\]

\[
v_o = -g_m \left[ \frac{R_D r_{ds}}{R_D + r_{ds}} \right] v_i = -g_m \left( R_D || r_{ds} \right) v_i
\]

\[
\frac{v_o}{v_i} = A_v = -g_m \left( R_D || r_{ds} \right)
\]

\( A_v \) is the voltage gain of this CS amplifier. Proper choice of DC bias ensures \( A_v > 1.0 \) or \( >> 1.0 \).
Example: For $A_{ny} = -10$, let $R_D = 5 \, \text{k}\Omega$ and $g_m = 2 \, \text{mA} / \text{V}$.

One option: choose $V_{OV} = 0.2 \, \text{V}$ and $I_D = 200 \, \mu A / \text{V}$.

Then use

$$I_D = \frac{\mu_n C_{ox} (\frac{w}{L})^2 V_{OV}^2}{2}$$

to find $\left(\frac{w}{L}\right)$.

Assume: $k_n' = \frac{200 \, \mu A}{V^2}$

then

$$200 \times 10^{-6} = 200 \times 10^{-6} \left(\frac{w}{L}\right)^2 \left(0.2\right)^2$$

$$\Rightarrow \left(\frac{w}{L}\right) = 50$$

This is a geometric design parameter.

Note: $R_D$ will affect the DC bias as well.

Meaning of negative sign in $A_{ny} = -g_m \left(\frac{R_D}{s_{ds}}\right)$
Using SSM to obtain $A_v$:

\[ R_D \]

\[ i_d \]

\[ v_i = v_{gs} \]

\[ v_{ds} = v_o \]

\[ g_m v_{gs} \]

\[ R_D \parallel r_{ds} \]

**Note:** $R_D$ appears in parallel with $r_{ds}$

\[ i_d \text{ flows through } R_D \parallel r_{ds} \]

\[ v_{ds} = v_o = 0 - g_m (R_D \parallel r_{ds}) v_{gs} \]

\[ = -g_m (R_D \parallel r_{ds}) v_i \]

\[ A_v = \frac{v_o}{v_i} = -g_m (R_D \parallel r_{ds}) \]

**Note:** As $R_D \rightarrow \infty$, $A_v \rightarrow -g_m r_{ds}$

This value of $A_v$ is the maximum achievable gain → intrinsic gain of the transistor.
A more practical CS amplifier circuit

\[ V_0 = V_O + V_o \]

**DC circuit/model**

**AC (SSM) circuit/model**

Here \( V_{ds} = V_o \) &

\[ V_{gs} = V_i \]
DC model sets the DC bias point. $V_{DD}$, $R_D$, $V_I$, $(\frac{u}{L})$ are chosen to ensure NMOS in SAT.

DC analysis provides $(I_D, V_{GS}, V_{DS}) = 0$.

AC model provides gain $A_{v2}$.

\[ \text{R}_i : \text{input resistance} \]
\[ \text{R}_o : \text{output} \]

As $R_{sig}$ has no impact:

\[ A_{v2} = -g_m (R_D || R_{ds}) \]

\[ R_i = \infty \]: Thevenin resistance between the input port.

$\text{I}_t = 0 = \text{I}_e$

$V_t = V_t = \pm \text{V}_T$

\[ \text{R}_i = \frac{V_t}{\text{I}_t} = \infty \]
$R_0$: output resistance. Thevenin resistance between output ports.

$$\frac{R_{srg}}{V_{gs}} = 0$$

$$I_t = V_t$$

$$R_o = \frac{V_t}{I_t} = R_D || R_{ds}$$

As the CS amplifier is a voltage amplifier, its input resistance is the ideal value of $\infty$. The output resistance's ideal value $R_o = 0$ should be 0 but it is not.
Interpreting CS-amplifier using I-V curves and load line:

Here: \( V_{gs} = V_I \); \( I_{gs} = I_i \); \( I_{ds} = I_i \)

\[ V_{DS} = V_o = V_{DD} - I_D R_D \]
CS Amplifier with coupling & bypass capacitances:

- Source (input) → CS amplifier → Load →

- $V_{DD}$
- $R_1$
- $R_D$
- $C_{c2}$
- $V_D$
- $R_O$
- $R_L$

$C_{c1}, C_{c2}$: coupling (DC-block) capacitors

- These ensure that the signal source ($V_I$) & load ($R_D$) do not affect the bias point $\Theta = (I_D, V_{GS}, V_{DS})$

$C_S$: bypass capacitance

- Ensures the source node is at AC ground, even though the current source provides the bias current $I = I_D$.

Recall: $V_g = V_G + \nu_g$; $V_s = V_G + (\nu_s = 0) C_s$

$V_D = V_D + \nu_d$; $I_d = I_D + i_d$
DC circuit: open all capacitors → ckt. containing the NMOS between the dotted lines is isolated from the input source and the load.

\[ V_G = \frac{R_2}{R_1 + R_2} V_{DD} \rightarrow \text{choose } R_1 \& R_2 \text{ to be large to minimize current} \]

\[ I_R = \frac{V_{DD}}{R_1 + R_2} \]

\[ V_D = V_{DD} - I_D R_D ; \quad I_D = I \]

\[ V_S \text{ is set as the solution to:} \]

\[ I_D = I = \frac{k_D}{2} (V_G - V_S - V_{th})^2 \]

Assumes: \( V_{DS} > V_{GS} - V_{th} \) (should check this always)
AC or SSM:

\[ v_{ds} = v_o \]

\[ u_{gs} = \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_{sig}} \cdot u_i \quad \text{(want } u_{gs} = u_i \text{ ideally)} \]

\[ u_o = -g_m \left( \frac{R_{ds} \parallel R_D \parallel R_L}{R_1 \parallel R_2} \right) u_{gs} \]

\[ = -g_m \left( \frac{R_{ds} \parallel R_D \parallel R_L}{R_1 \parallel R_2} \right) \left( \frac{R_1 \parallel R_2}{(R_1 \parallel R_2) + R_{sig}} \right) u_i \]

\[ A_{\text{gs}} = -g_m \left( \frac{R_{ds} \parallel R_D \parallel R_L}{(R_1 \parallel R_2) + R_{sig}} \right) \left( \frac{R_1 \parallel R_2}{(R_1 \parallel R_2) + R_{sig}} \right)(\gg 1) \]

\[ \text{(but close to 1.0)} \]

\[ R_i = R_1 \parallel R_2 \]

\[ R_o = R_{ds} \parallel R_D \]

\( R_i \) and \( R_o \) do not include circuitry to the left and right of the dotted line.
Choosing capacitor values: these should be sufficiently large so that they become shorts in the AC model.

e.g. Choosing $C_{c1}$:

\[ \frac{R_{sig}}{sC_{c1}} \quad \Rightarrow \quad \frac{R_{sig}}{sC_{c1}} \quad \Rightarrow \quad \frac{R_{sig}}{sC_{c1}} \quad \Rightarrow \quad \frac{R_{sig}}{sC_{c1}} \]

\[ \frac{R_{1||R_2}}{R_{sig} + (R_{1||R_2} + \frac{1}{sC_{c1}})} \quad \Rightarrow \quad \frac{R_{1||R_2}}{R_{sig} + (R_{1||R_2})} \]

\[ \text{want} \left| \frac{1}{sC_{c1}} \right| \ll R_{sig} + (R_{1||R_2}) \text{ at frequencies of interest} \]

\[ v_i(t) = v_i \sin(\omega t) \]

\[ C_{c1} \gg \frac{1}{\omega_i (R_{sig} + (R_{1||R_2})) \text{ minimum input frequency}} \]

Similarly, for $C_{c2}$ and $C_s$.

For simplicity, we assume $C_{c1} = \infty$, $C_{c2} = \infty$, $C_s = \infty$.

These are shorts in the AC model.