ECE 342
Electronic Circuits

Lecture 6
MOS Transistors

Jose E. Schutt-Aine
Electrical & Computer Engineering
University of Illinois
jesa@Illinois.edu
Typically $L = 0.1 \text{ to } 3 \, \mu\text{m}$, $W = 0.2 \text{ to } 100 \, \mu\text{m}$, and the thickness of the oxide layer ($t_{\text{ox}}$) is in the range of 2 to 50 nm.
• NMOS Transistor
  – N-Channel MOSFET
  – Built on p-type substrate
  – MOS devices are smaller than BJTs
  – MOS devices consume less power than BJTs
NMOS Transistor - Layout

Top View

Cross Section
MOS Regions of Operation

- **Resistive**
  - $V_{GS} > V_T$
  - $V_{DS} \text{ small}$

- **Triode**
  - $V_{GS} > V_T$
  - $V_{DS} < (V_{GS} - V_T)$

- **Nonlinear**
  - $V_{GS} > V_T$
  - $V_{DS} < (V_{GS} - V_T)$

- **Active**
  - $V_{GS} > V_T$
  - $V_{DS} \geq V_{GS} - V_T$
MOS Transistor Operation

• As $V_G$ increases from zero
  – Holes in the p substrate are repelled from the gate area leaving negative ions behind
  – A depletion region is created
  – No current flows since no carriers are available

• As $V_G$ increases
  – The width of the depletion region and the potential at the oxide-silicon interface also increase
  – When the interface potential reaches a sufficiently positive value, electrons flow in the “channel”. The transistor is turned on

• As $V_G$ rises further
  – The charge in the depletion region remains relatively constant
  – The channel current continues to increase
MOS – Triode Region - 1

\[ I_D = \mu \frac{W}{L} C_{ox} \left[ (V_{GS} - V_T) V_{DS} \right] \]

\[ V_{DS} \ll \left( V_{GS} - V_T \right) \]

\[ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \varepsilon_o}{t_{ox}} \]

- \( C_{ox} \): gate oxide capacitance
- \( \mu \): electron mobility
- \( L \): channel length
- \( W \): channel width
- \( V_T \): threshold voltage
FET is like a linear resistor with

\[ r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)} \]
MOS – Triode Region - 2

\[ \frac{V_{GS}}{V_T} > \frac{V_{DS}}{(V_{GS} - V_T)} \]

- Charge distribution is nonuniform across channel
- Less charge induced in proximity of drain

\[ I_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]
MOS – Active (Saturation) Region

Saturation occurs at pinch off when

\[ V_{DS} = (V_{GS} - V_T) = V_{DSS} \]

\[ V_{GS} > V_T \]

\[ V_{DS} > (V_{GS} - V_T) \]  
(saturation)

\[ I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \]
NMOS – Circuit Symbols

(a)  
(b)  
(c)  

D
G
B
S

D
G
B
S

D
G
S

NMOS – Regions of Operation

**Cut off**

\[ V_{GS} < V_T \]

\[ I_D = 0 \]

**Triode**

\[ V_{GS} > V_T \]

\[ V_{DS} < (V_{GS} - V_T) \]

\[ I_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

**Saturation**

\[ V_{GS} > V_T \]

\[ V_{DS} > (V_{GS} - V_T) \]

\[ I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \]
NMOS – Drain Current

The diagram illustrates the drain current $i_D$ as a function of $v_{DS}$. The curve bends because the channel resistance increases with $v_{DS}$.

- **Triode Region**: $v_{DS} < v_{GS} - V_t$
  - Current increases linearly with $v_{DS}$, proportional to $(v_{GS} - V_t)$.

- **Saturation Region**: $v_{DS} \geq v_{GS} - V_t$
  - Current saturates because the channel is pinched off at the drain end, and $v_{DS}$ no longer affects the channel.

The equation $v_{DS_{sat}} = v_{GS} - V_t$ defines the saturation region, where the drain-source voltage equals the threshold voltage plus the gate-source voltage.
characteristics for a device with $k'_n \ (W/L) = 1.0 \ mA/V^2$. 
MOS Threshold Voltage

The value of $V_G$ for which the channel is “inverted” is called the threshold voltage $V_T$ (or $V_t$).

- **Characteristics of the threshold voltage**
  - Depends on equilibrium potential
  - Controlled by inversion in channel
  - Adjusted by implantation of dopants into the channel
  - Can be positive or negative
  - Influenced by the body effect
nMOS Device Types

• **Enhancement Mode**
  – Normally off & requires positive potential on gate
  – Good at passing low voltages
  – Cannot pass full $V_{DD}$ (pinch off)

• **Depletion Mode**
  – Normally on (negative threshold voltage)
  – Channel is implanted with positive ions ($\rightarrow V_T$)
  – Provides inverter with full output swings
Types of MOSFETS
PMOS Transistor

- All polarities are reversed from nMOS
- $v_{GS}$, $v_{DS}$ and $V_t$ are negative
- Current $i_D$ enters source and leaves through drain
- Hole mobility is lower $\Rightarrow$ low transconductance
- nMOS favored over pMOS
PMOS – Regions of Operation

**Cut off**

\[ V_{GS} > V_{TP} \]

\[ I_D = 0 \]

**Triode**

\[ V_{GS} < V_{TP} \]

\[ V_{DS} > (V_{GS} - V_{TP}) \]

\[ I_D = -\mu_p C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{TP})V_{DS} - \frac{1}{2}V_{DS}^2 \right] \]

**Saturation**

\[ V_{GS} < V_{TP} \]

\[ V_{DS} < (V_{GS} - V_{TP}) \]

\[ I_D = -\mu_p C_{ox} \frac{W}{2L} \left( V_{GS} - V_{TP} \right)^2 \]
PMOS – Alternative Equations

In positive quantities \((V_{SG}, V_{SD}, |V_{TP}|)\)

**Cut off**

\[
V_{SG} < |V_{TP}|
\]

\[
I_D = 0
\]

**Triode**

\[
V_{SG} > |V_{TP}|
\]

\[
V_{SD} < (V_{SG} - |V_{TP}|)
\]

\[
I_D = \mu_p C_{ox} \frac{W}{L} \left[ (V_{SG} - |V_{TP}|) V_{SD} - \frac{1}{2} V_{SD}^2 \right]
\]

**Saturation**

\[
V_{SG} > |V_{TP}|
\]

\[
V_{SD} > (V_{SG} - |V_{TP}|)
\]

\[
I_D = \mu_p C_{ox} \frac{W}{2L} \left( V_{SG} - |V_{TP}| \right)^2
\]