ECE 342
Electronic Circuits

Lecture 6
MOS Transistors

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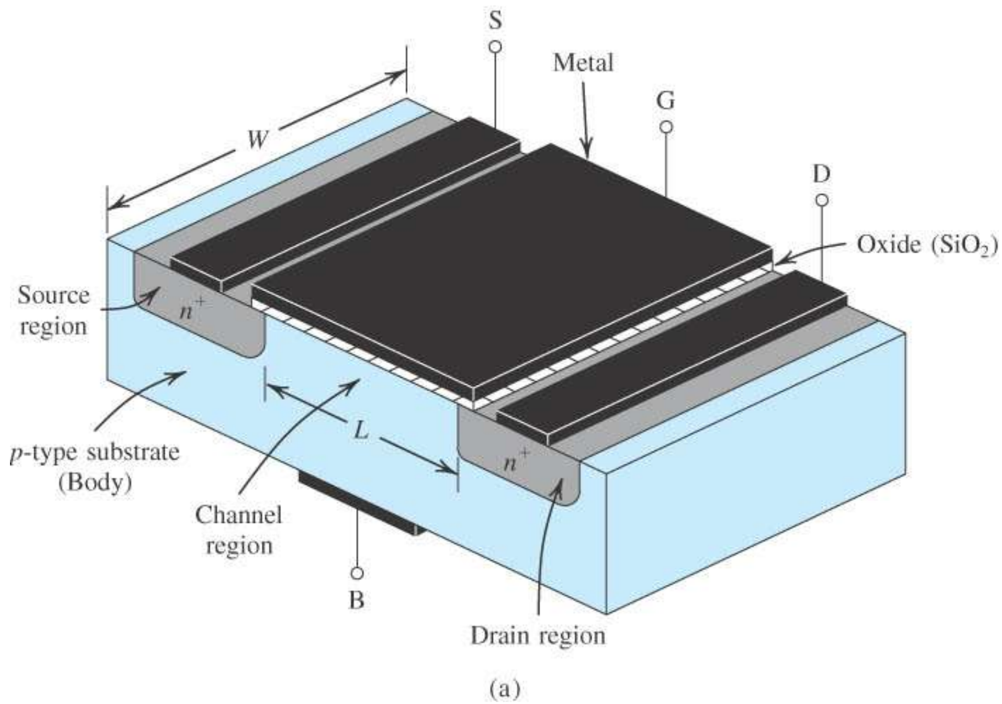
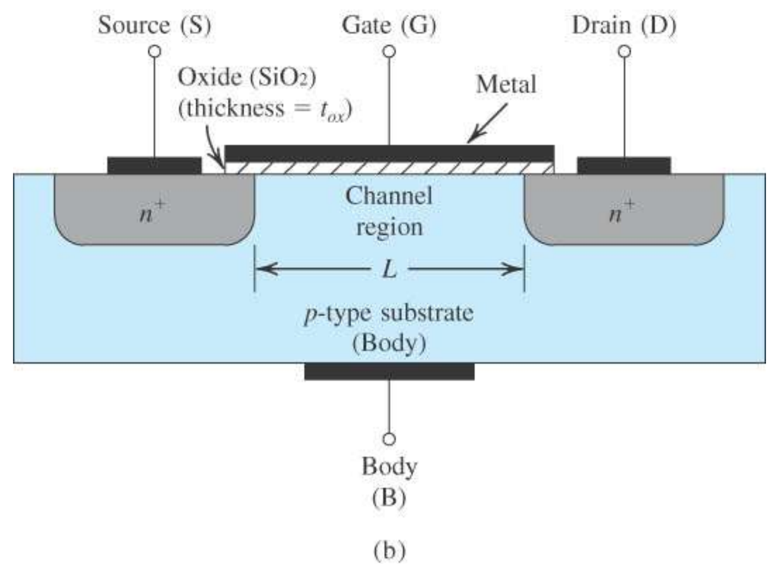
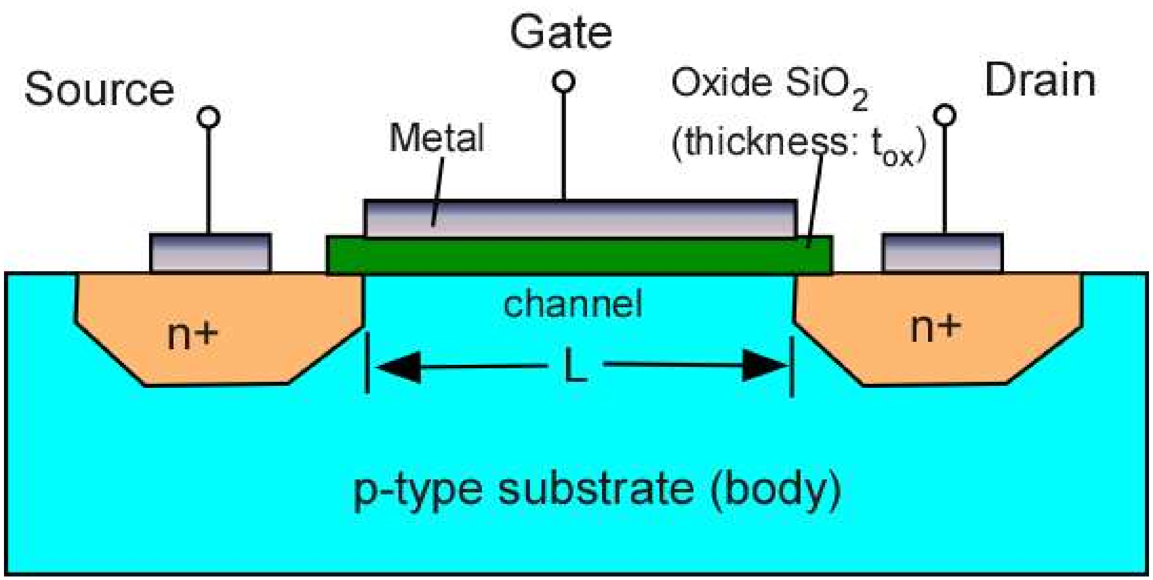
NMOS Transistor





Typically L = 0.1 to 3 μm, W = 0.2 to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

NMOS Transistor

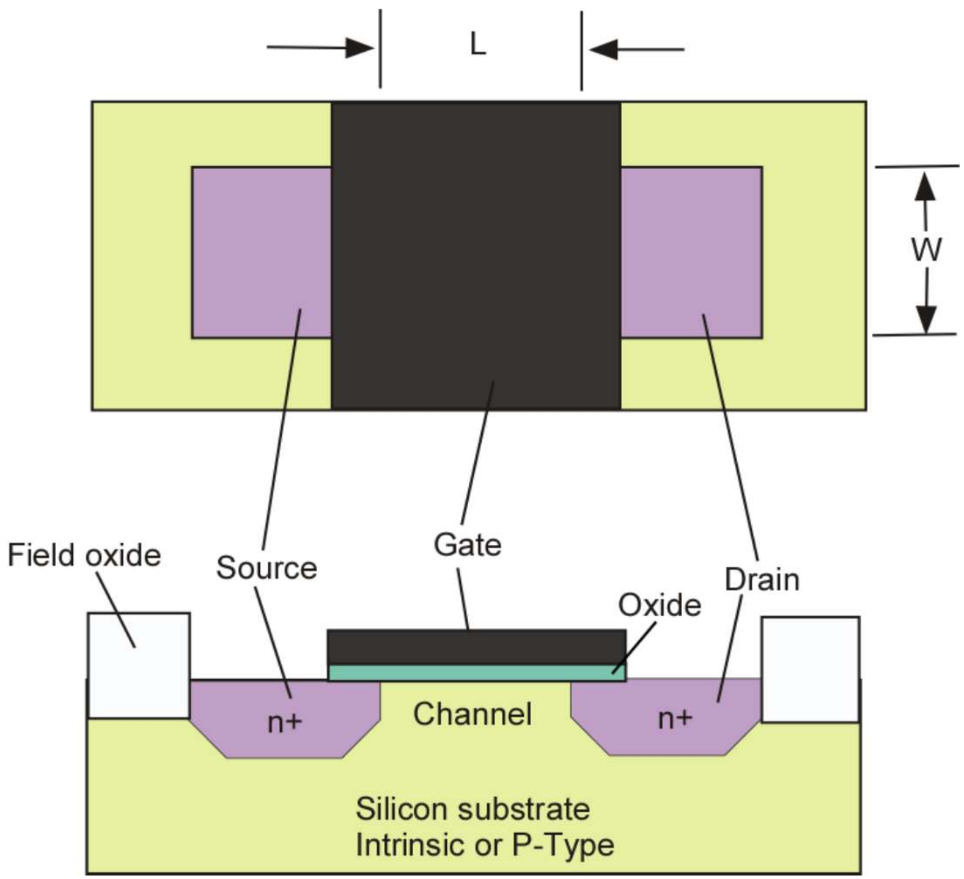


- **NMOS Transistor**
  - N-Channel MOSFET
  - Built on p-type substrate
  - MOS devices are smaller than BJTs
  - MOS devices consume less power than BJTs

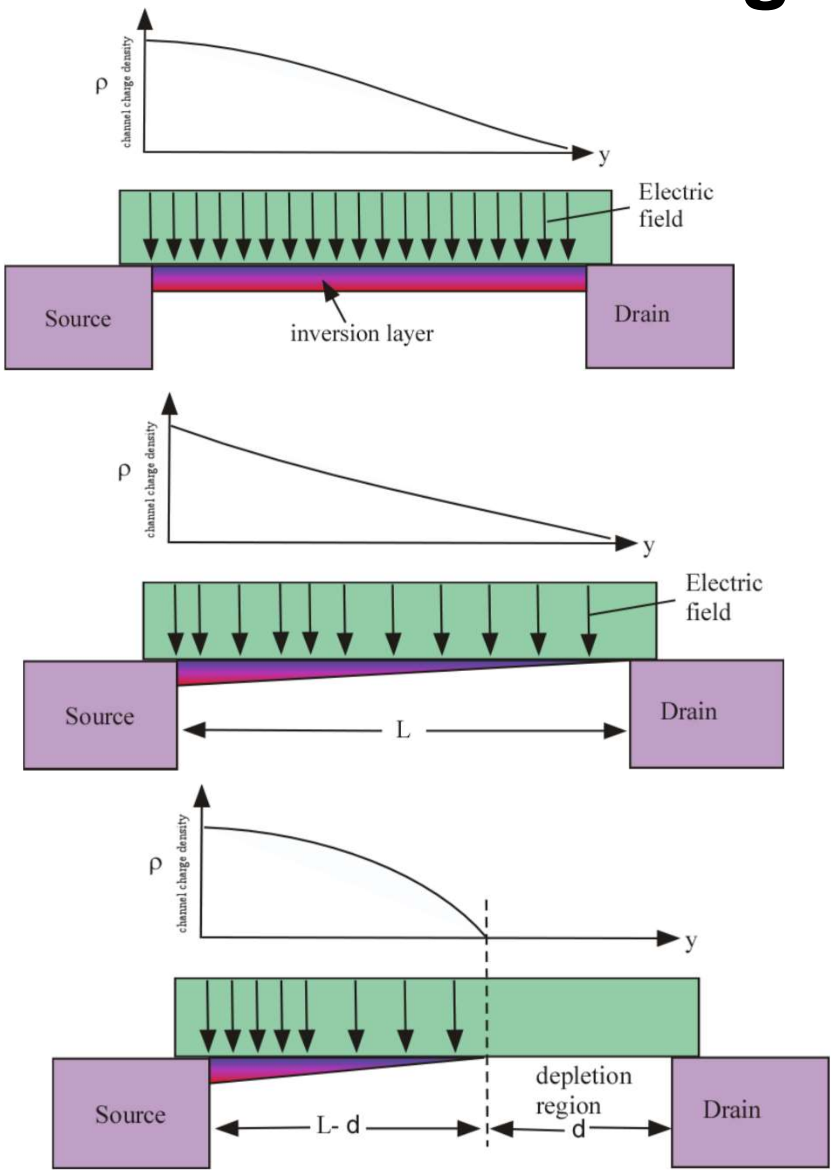
NMOS Transistor - Layout

Top View

Cross Section



MOS Regions of Operation



Triode

Resistive

$$V_{GS} > V_T$$

$$V_{DS} \ small$$

Nonlinear

$$V_{GS} > V_T$$

$$V_{DS} < (V_{GS} - V_T)$$

Active

Saturation

$$V_{GS} > V_T$$

$$V_{DS} \geq V_{GS} - V_T$$

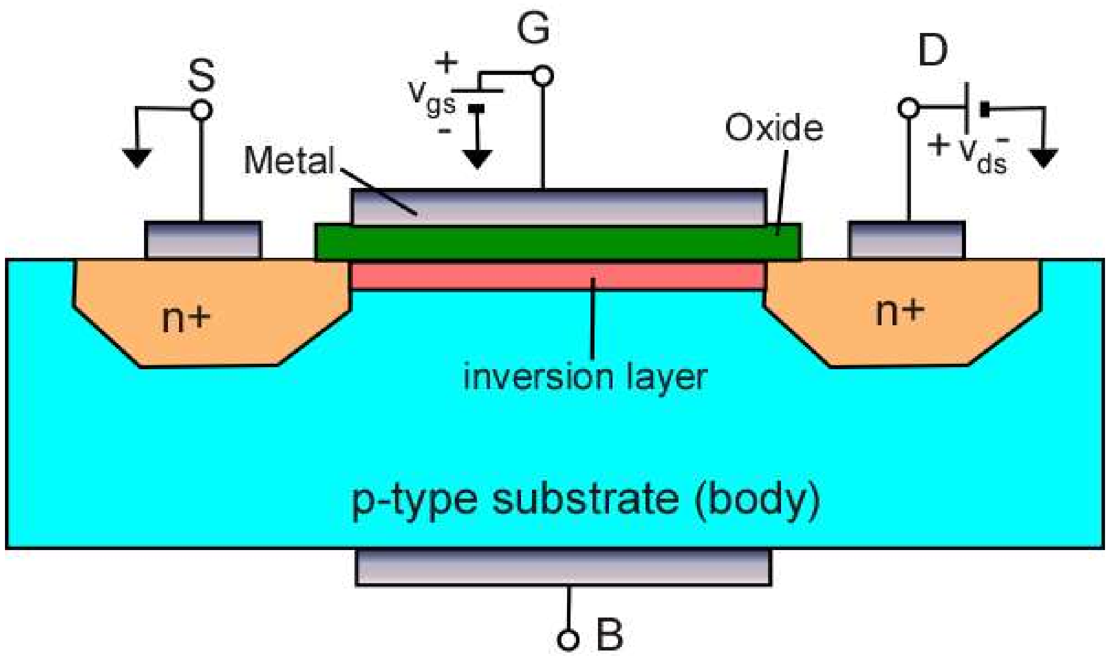
MOS Transistor Operation

- **As V_G increases from zero**
  - Holes in the p substrate are repelled from the gate area leaving negative ions behind
  - A depletion region is created
  - No current flows since no carriers are available

- **As V_G increases**
  - The width of the depletion region and the potential at the oxide-silicon interface also increase
  - When the interface potential reaches a sufficiently positive value, electrons flow in the "*channel*". The transistor is turned on

- **As V_G rises further**
  - The charge in the depletion region remains relatively constant
  - The channel current continues to increase

MOS – Triode Region - 1



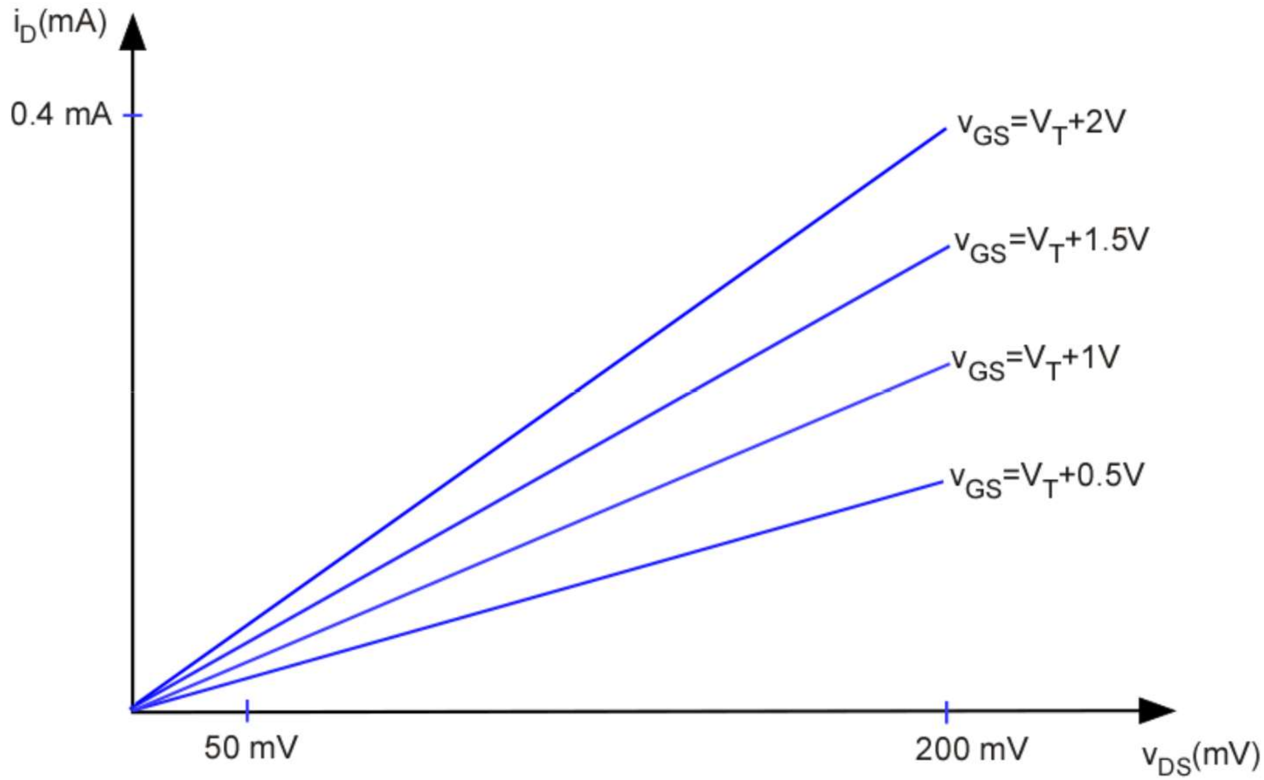
$$I_D = \mu \frac{W}{L} C_{ox} \left[\left(V_{GS} - V_T \right) V_{DS} \right]$$

$$V_{DS} << \left(V_{GS} - V_T \right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\varepsilon_o}{t_{ox}}$$

C_{ox}: gate oxide capacitance
μ: electron mobility
L: channel length
W: channel width
V_T: threshold voltage

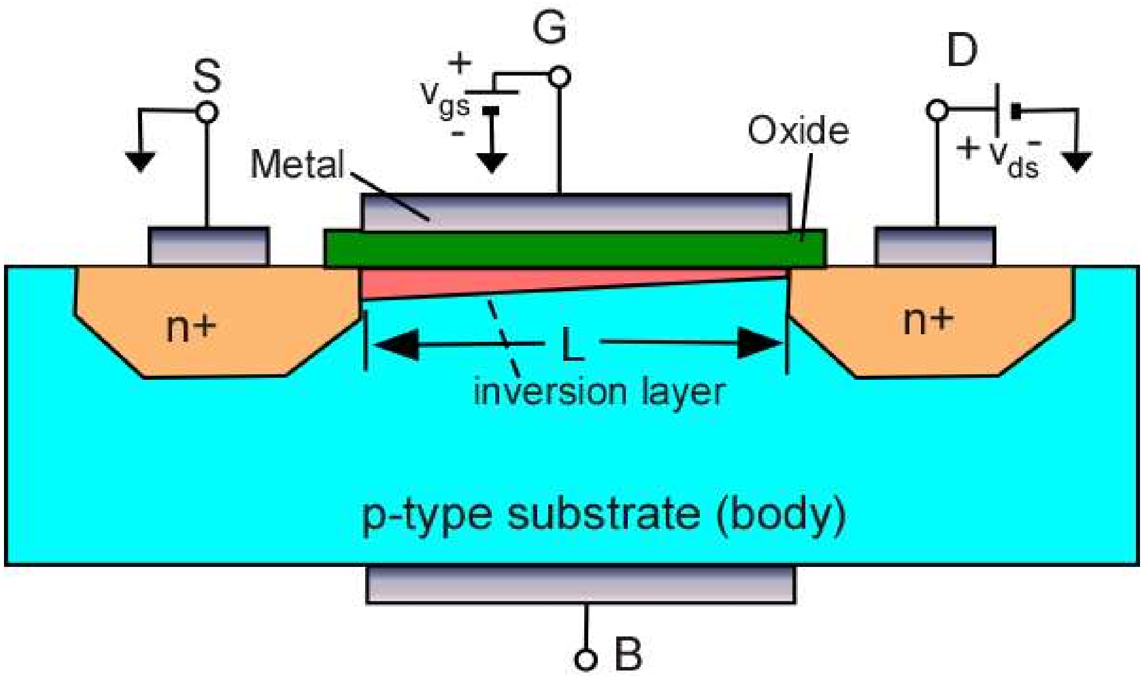
MOS – Triode Region - 1



FET is like a linear resistor with

$$r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_T\right)}$$

MOS – Triode Region - 2



$$V_{GS} > V_T$$

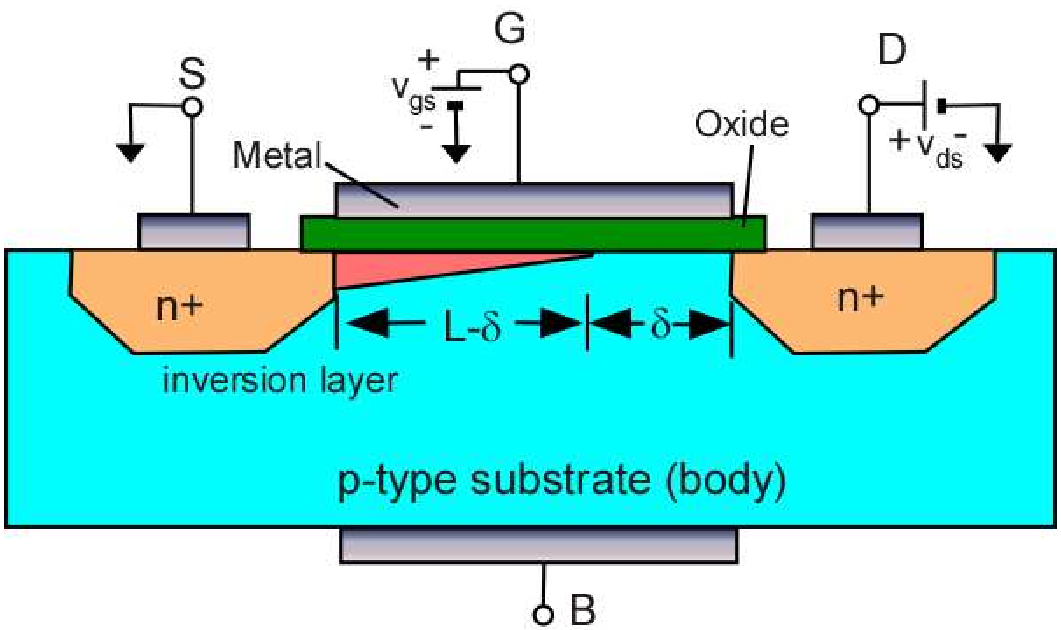
$$V_{DS} < (V_{GS} - V_T)$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

– Charge distribution is nonuniform across channel
– Less charge induced in proximity of drain

MOS – Active (Saturation) Region

Saturation occurs at pinch off when $V_{DS} = (V_{GS} - V_T) = V_{DSP}$



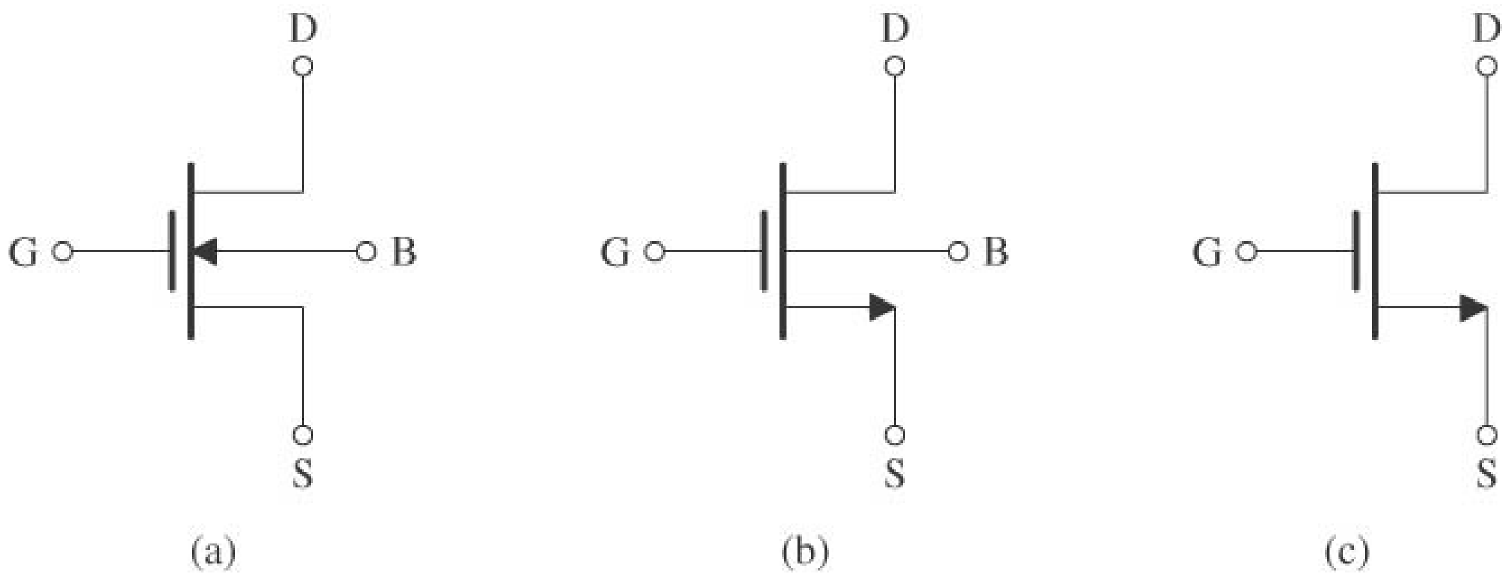
$$V_{GS} > V_T$$

$$V_{DS} > (V_{GS} - V_T)$$

(saturation)

$$I_D = \mu_n C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2$$

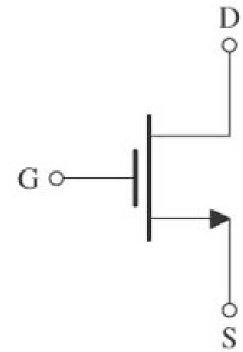
NMOS – Circuit Symbols



NMOS – Regions of Operation

Cut off

$$V_{GS} < V_T \qquad I_D = 0$$



Triode

$$V_{GS} > V_T$$

$$V_{DS} < (V_{GS} - V_T)$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

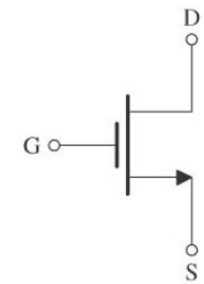
Saturation

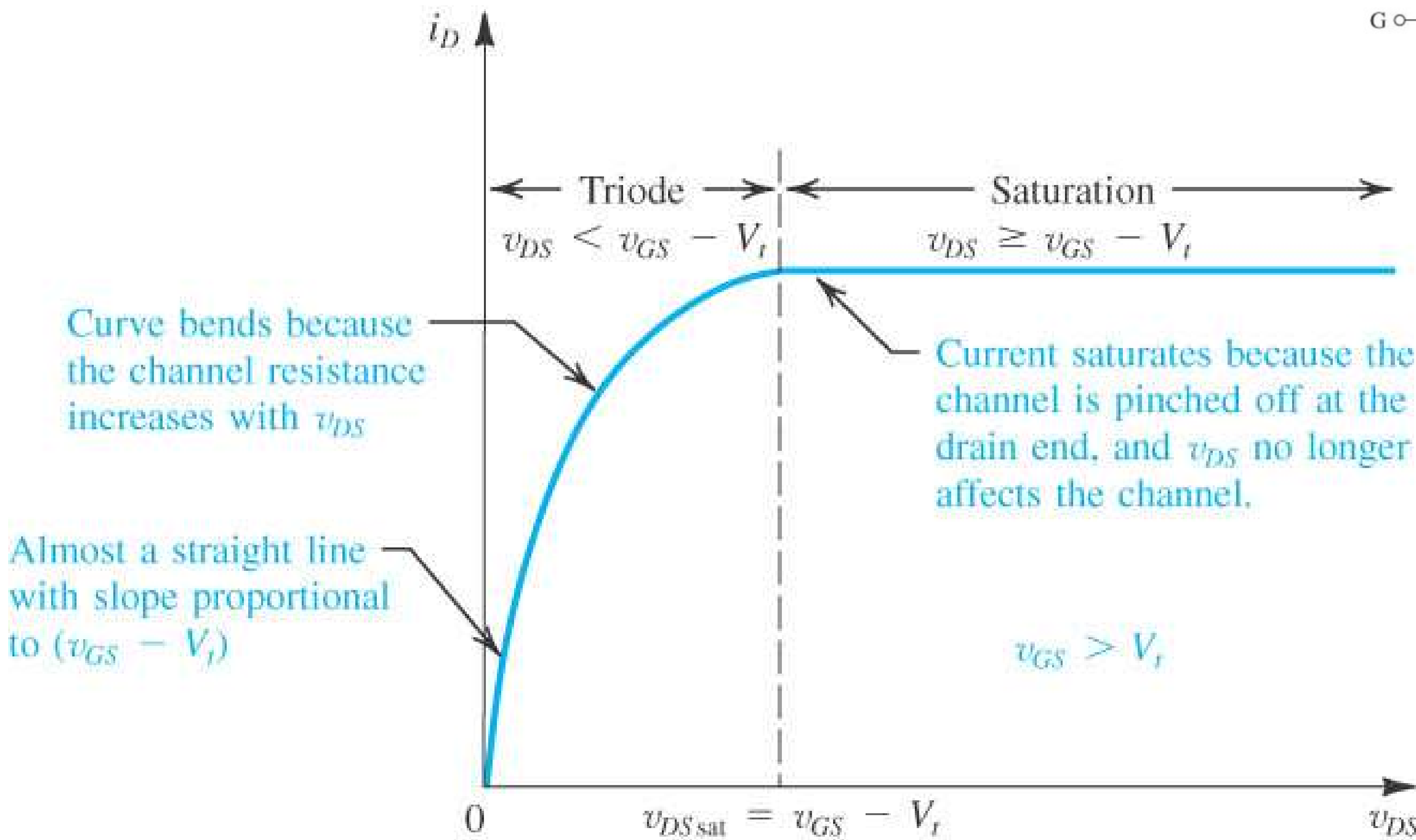
$$V_{GS} > V_T$$

$$V_{DS} > (V_{GS} - V_T)$$

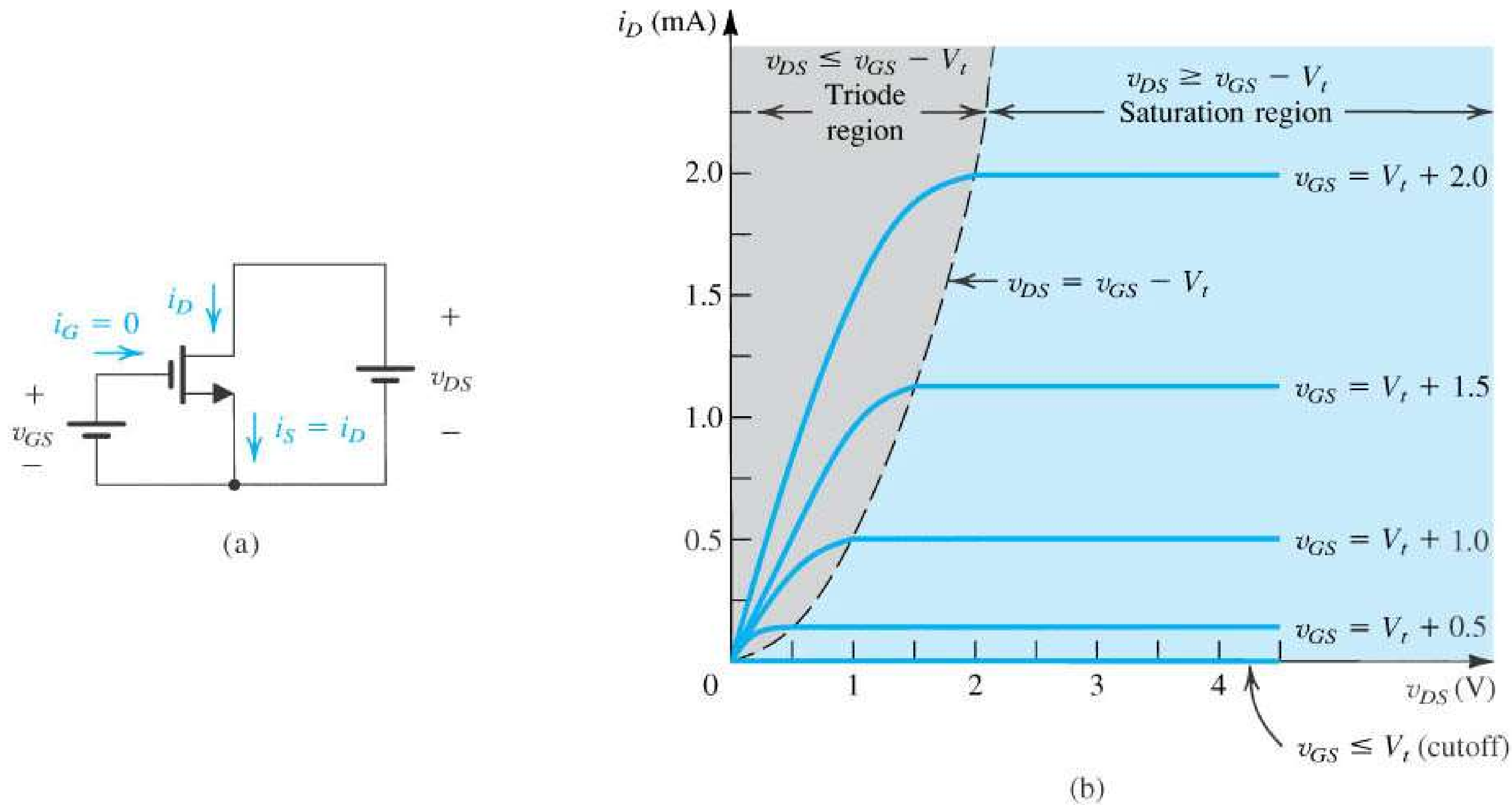
$$I_D = \mu_n C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2$$

NMOS – Drain Current





NMOS – IV Characteristics



characteristics for a device with $k'_n (W/L) = 1.0$ mA/V^2.

MOS Threshold Voltage

The value of V_G for which the channel is *"inverted"* is called the threshold voltage V_T (or V_t).

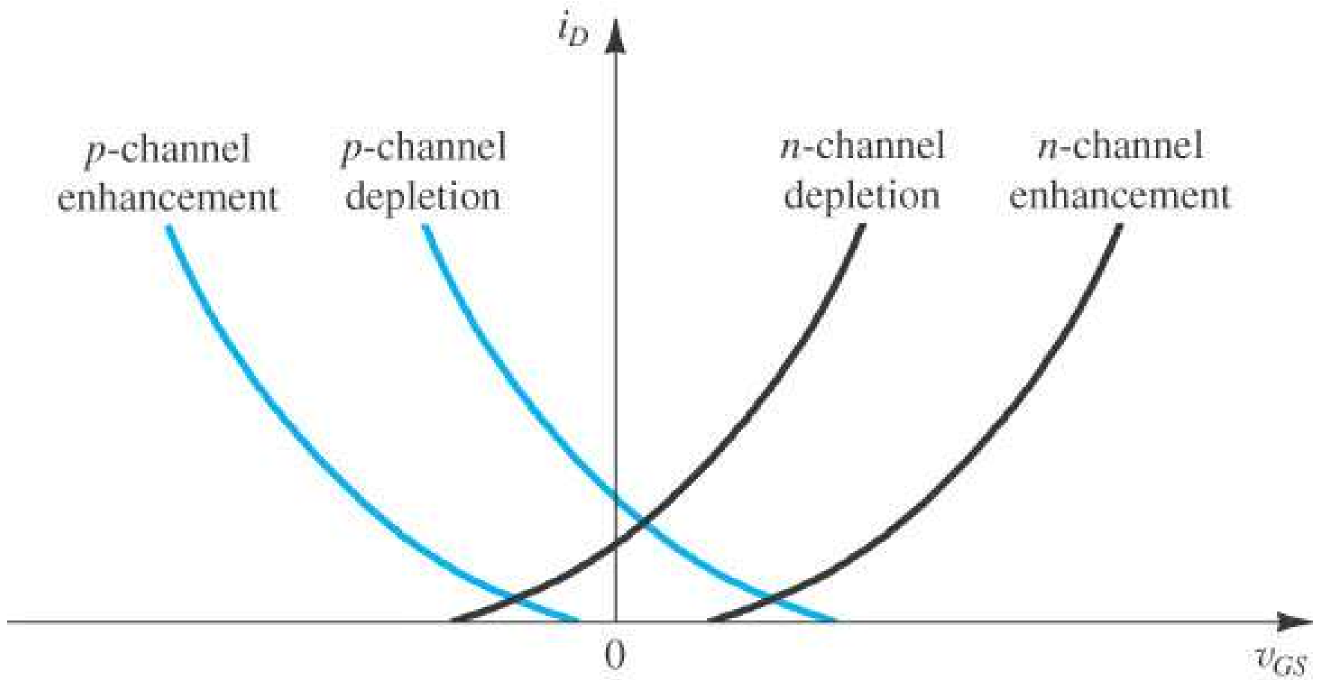
- **Characteristics of the threshold voltage**
  - Depends on equilibrium potential
  - Controlled by inversion in channel
  - Adjusted by implantation of dopants into the channel
  - Can be positive or negative
  - Influenced by the body effect

nMOS Device Types

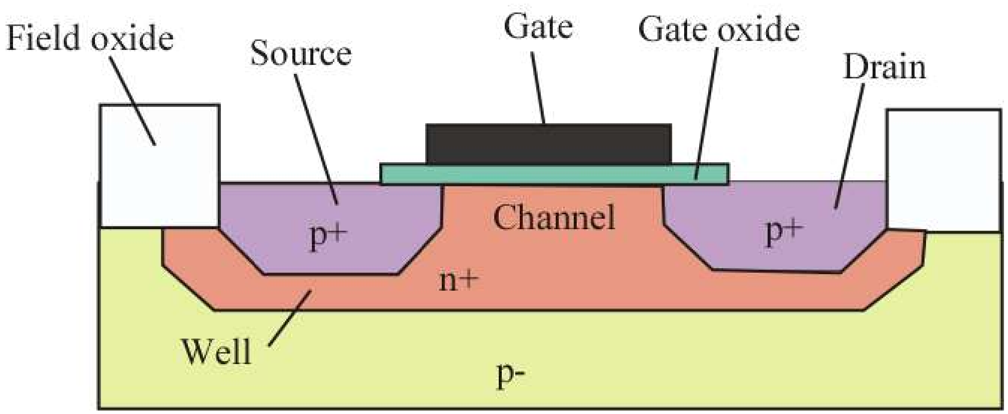
- **Enhancement Mode**
  - Normally off & requires positive potential on gate
  - Good at passing low voltages
  - Cannot pass full V_{DD} (pinch off)

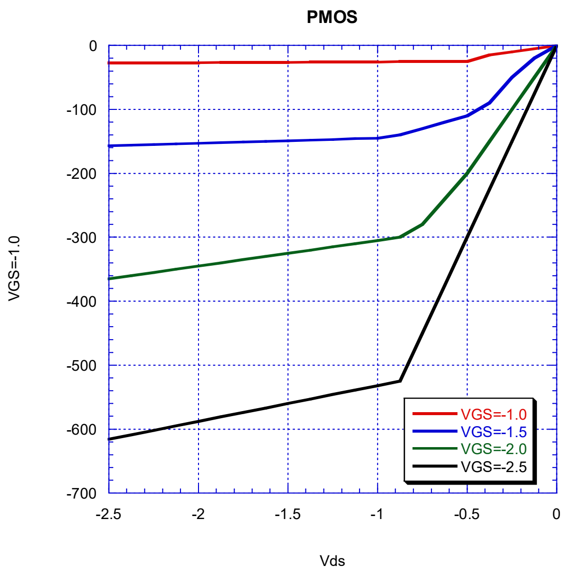
- **Depletion Mode**
  - Normally on (negative threshold voltage)
  - Channel is implanted with positive ions ($\rightarrow V_T$)
  - Provides inverter with full output swings

Types of MOSFETS



PMOS Transistor





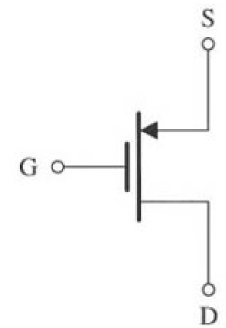
- All polarities are reversed from nMOS
- v_{GS}, v_{DS} and V_t are negative
- Current i_D enters source and leaves through drain
- Hole mobility is lower $\Rightarrow$ low transconductance
- nMOS favored over pMOS

PMOS – Regions of Operation

I_D : drain current flowing from drain to source

Cut off

$$V_{GS} > V_{TP} \qquad I_D = 0$$



Triode

$$V_{GS} < V_{TP}$$

$$V_{DS} > \left(V_{GS} - V_{TP}\right)$$

$$I_D = -\mu_p C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_{TP}\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Saturation

$$V_{GS} < V_{TP}$$

$$V_{DS} < \left(V_{GS} - V_{TP}\right)$$

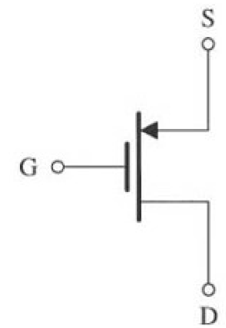
$$I_D = -\mu_p C_{ox} \frac{W}{2L}\left(V_{GS} - V_{TP}\right)^2$$

PMOS – Alternative Equations

In positive quantities (V_{SG}, V_{SD}, $|V_{TP}|$)

Cut off

$$V_{SG} < |V_{TP}| \qquad I_D = 0$$



Triode

$$V_{SG} > |V_{TP}|$$

$$V_{SD} < \left(V_{SG} - |V_{TP}|\right)$$

$$I_D = \mu_p C_{ox} \frac{W}{L}\left[\left(V_{SG} - |V_{TP}|\right)V_{SD} - \frac{1}{2}V_{SD}^2\right]$$

Saturation

$$V_{SG} > |V_{TP}|$$

$$V_{SD} > \left(V_{SG} - |V_{TP}|\right)$$

$$I_D = \mu_p C_{ox} \frac{W}{2L}\left(V_{SG} - |V_{TP}|\right)^2$$