ECE 342
Electronic Circuits

Lecture 32
CMOS

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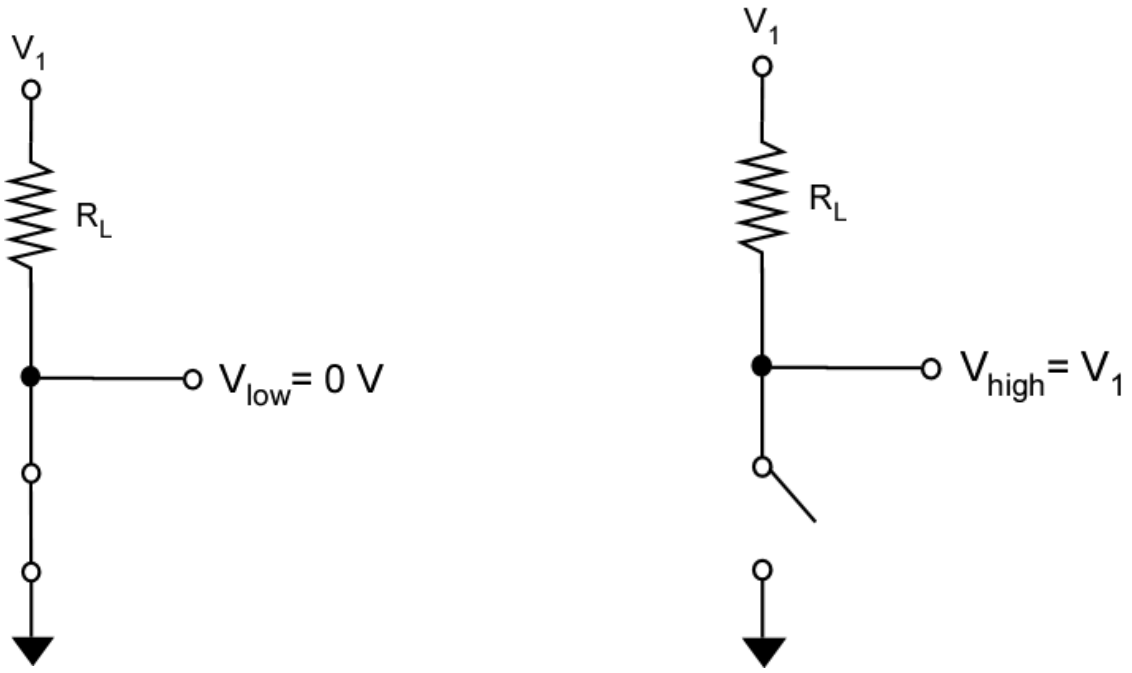
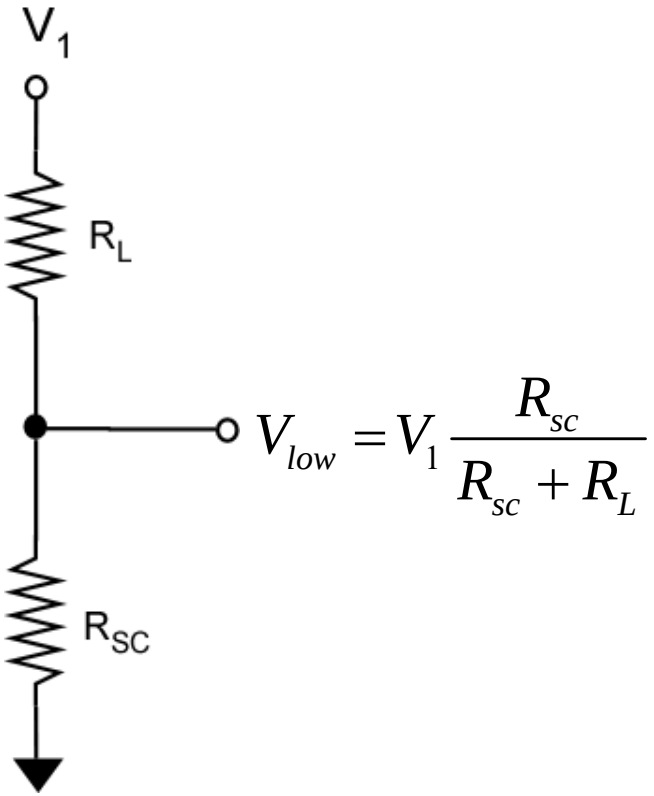
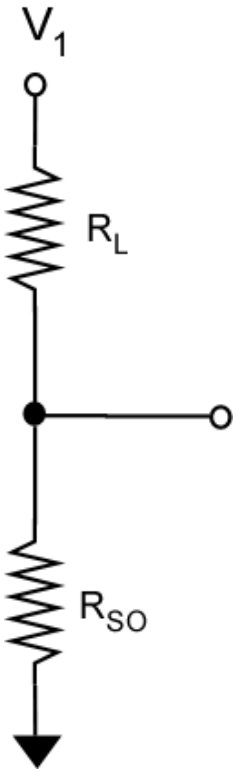
Switching Circuit



Nonideal Switch

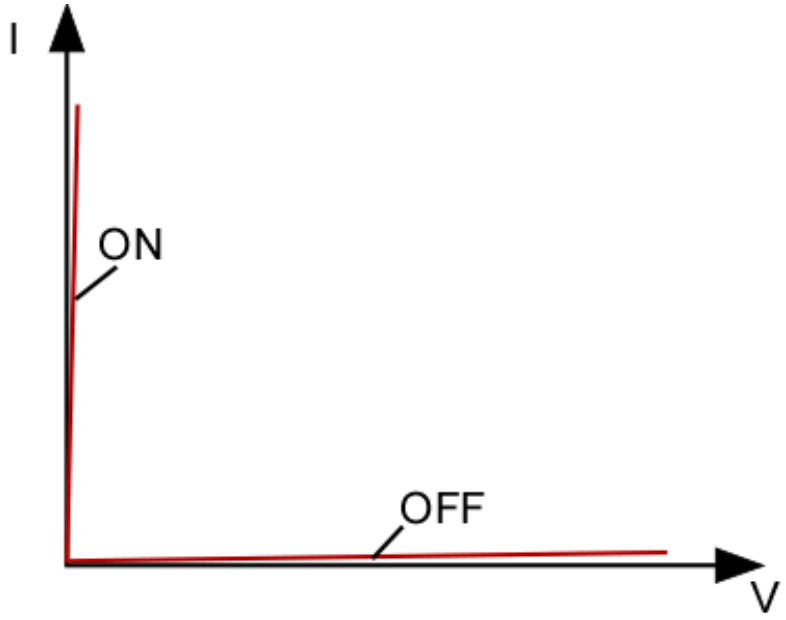


$$V_{low} = V_1 \frac{R_{sc}}{R_{sc} + R_L}$$

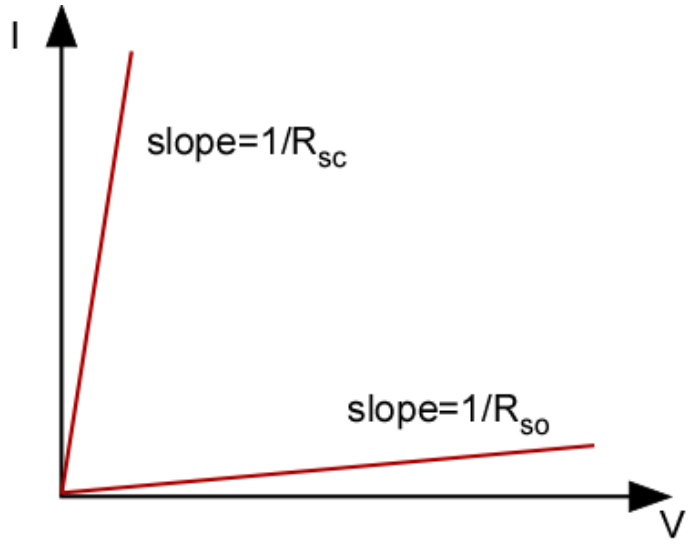


$$V_{high} = V_1 \frac{R_{so}}{R_{so} + R_L}$$

IV Characteristics of Switches

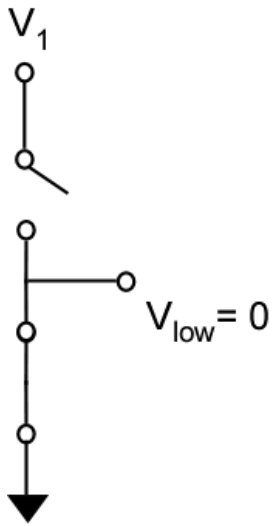


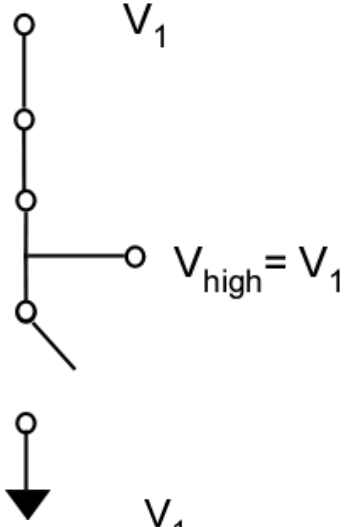
Ideal switch

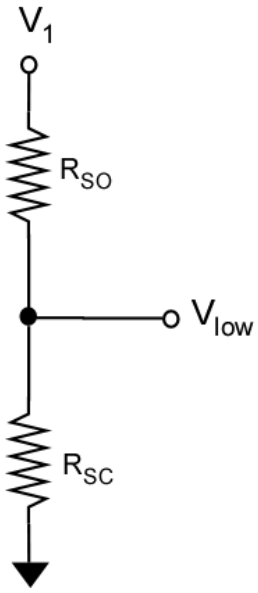


Non-ideal switch

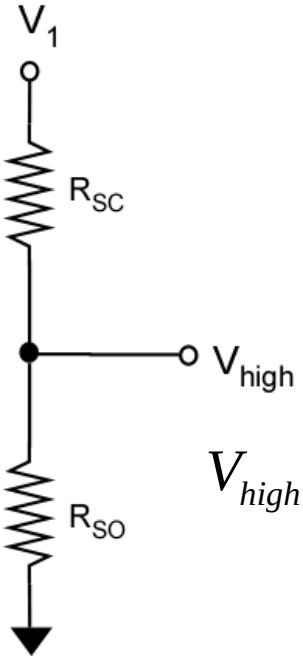
Complementary Switches







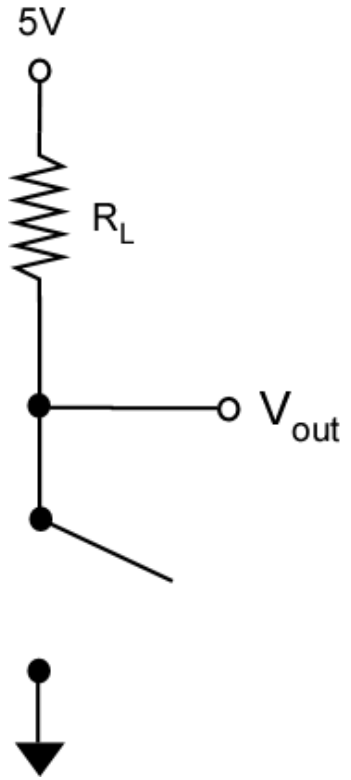
$$V_{low} = V_1 \frac{R_{sc}}{R_{sc} + R_{so}}$$



$$V_{high} = V_1 \frac{R_{so}}{R_{so} + R_{sc}}$$

Problem

A switch has an open (off) resistance of 10MΩ and close (on) resistance of 100 Ω.
Calculate the two voltage levels of V_{out} for the circuit shown. Assume R_L=5 kΩ



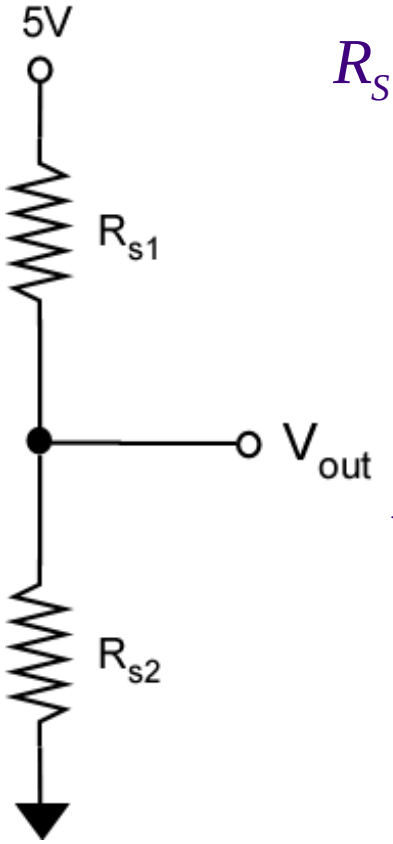
$$V_{out} = \frac{V_{CC} R_S}{R_L + R_S}$$

$$Open: \; R_S = 10 \times 10^6 \, \Omega \Rightarrow V_{out} \approx 5V$$

$$Short: \; R_S = 10^2 \, \Omega \Rightarrow V_{out} = \frac{5 \cdot 10^2}{5000 + 100} = 0.098V$$

Problem

If two switches are used as shown, calculate the two output voltage levels. Assume switches are complementary



$$R_S \ \ on = 100\,\Omega\,,\ \ R_S \ \ off = 10\,M\Omega$$

$$V_{out} = \frac{V_{CC} R_{S2}}{R_{S1} + R_{S2}}$$

State 1: S_1 off, S_2 on

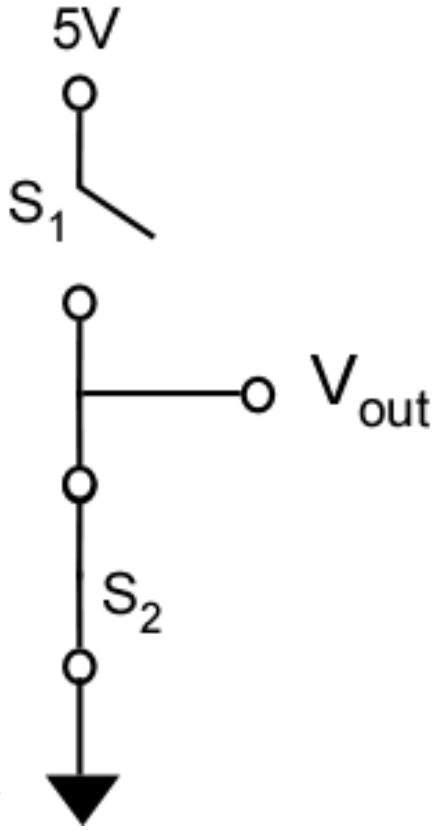
➔R_{S1}=10 MΩ, R_{S2}=100 Ω

$$V_{out} = \frac{5 \times 100}{10 \times 10^6 + 100} = 5\mu V \approx 0V$$

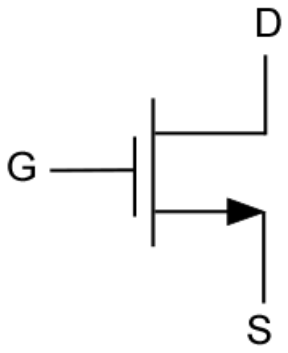
State 2: S_1 on, S_2 off

➔R_{S1}=100 Ω, R_{S2}=10 MΩ

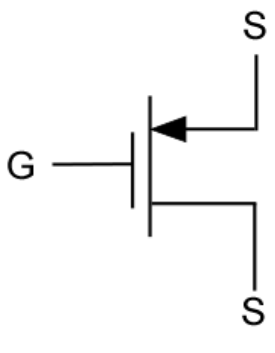
$$V_{out} = \frac{5 \times 10 \times 10^6}{10 \times 10^6 + 100} = \frac{5 \times 10^7}{10^7 + 100} \simeq 5V$$



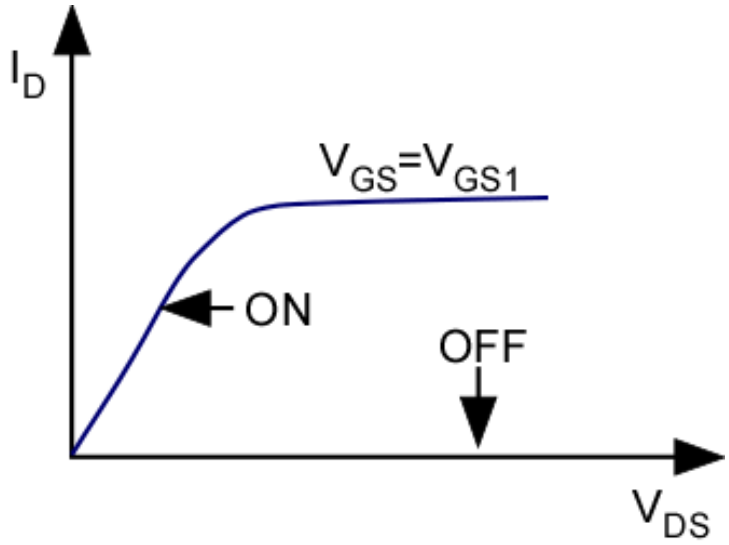
MOSFET Switch



NMOS

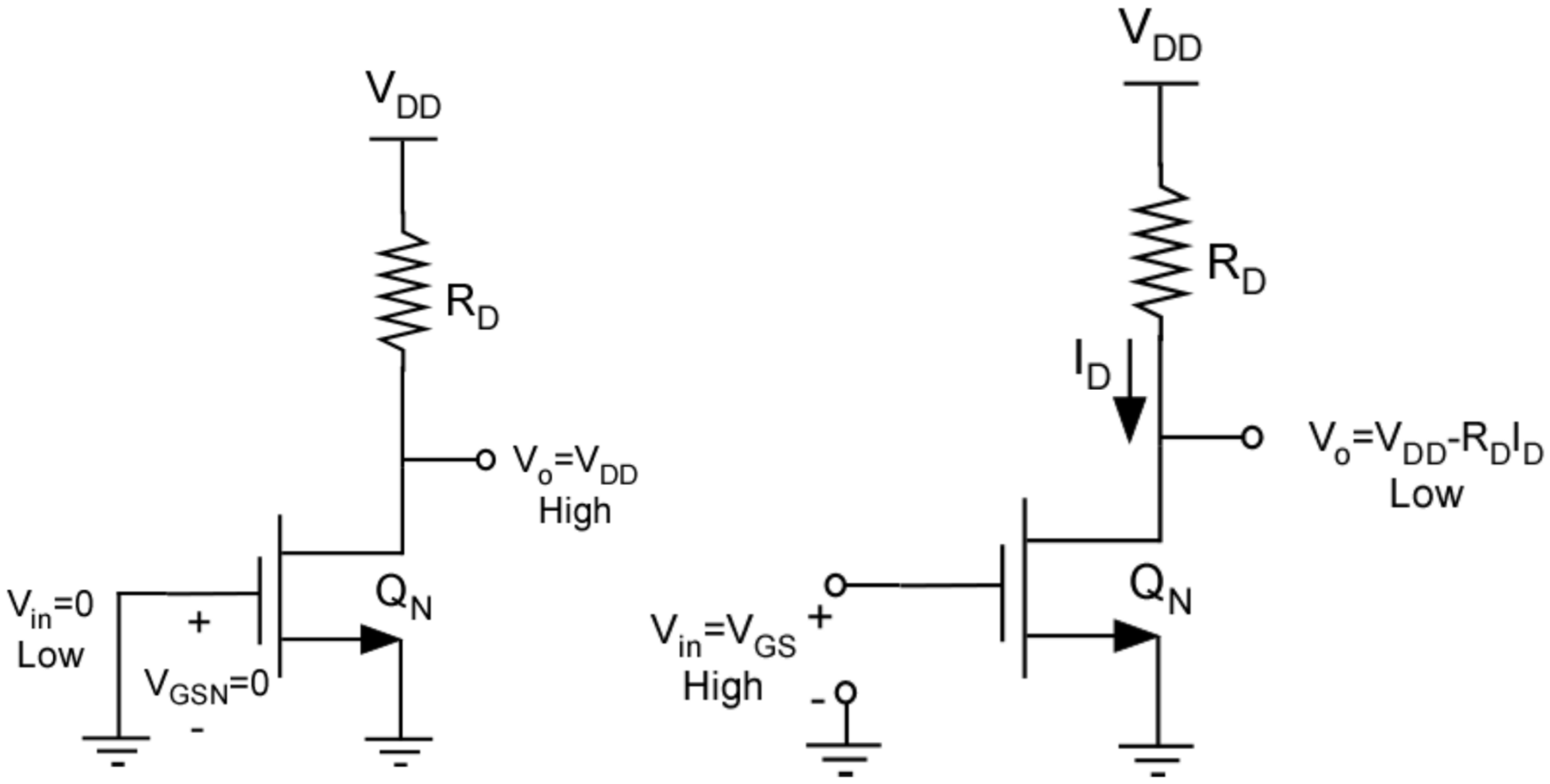


PMOS

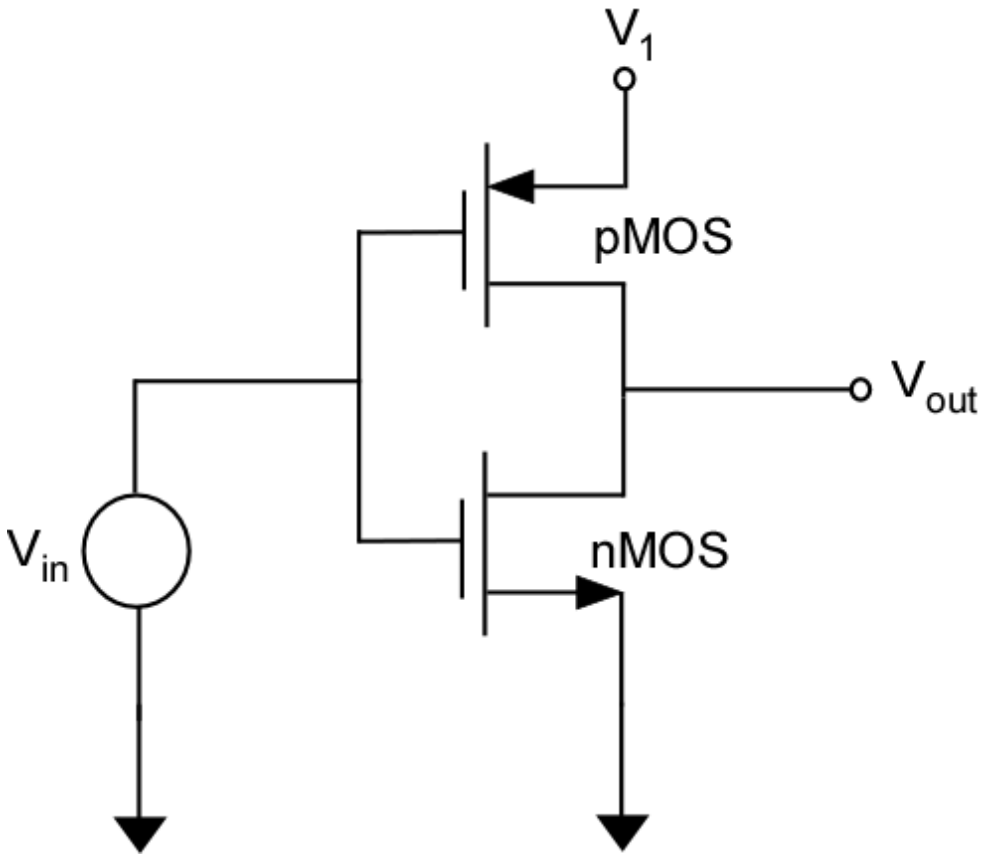


- **Characteristics of MOS Switch**
  - MOS approximates switch better than BJT in off state
  - Resistance in on state can vary from 100 Ω to 1 kΩ

NMOS Switch


V_{DD}
R_D
$V_o=V_{DD}$
High
$V_{in}=0$
Low
+
$V_{GSN}=0$
-
Q_N
V_{DD}
R_D
I_D
$V_o=V_{DD}-R_DI_D$
Low
$V_{in}=V_{GS}$
High
+
-
Q_N

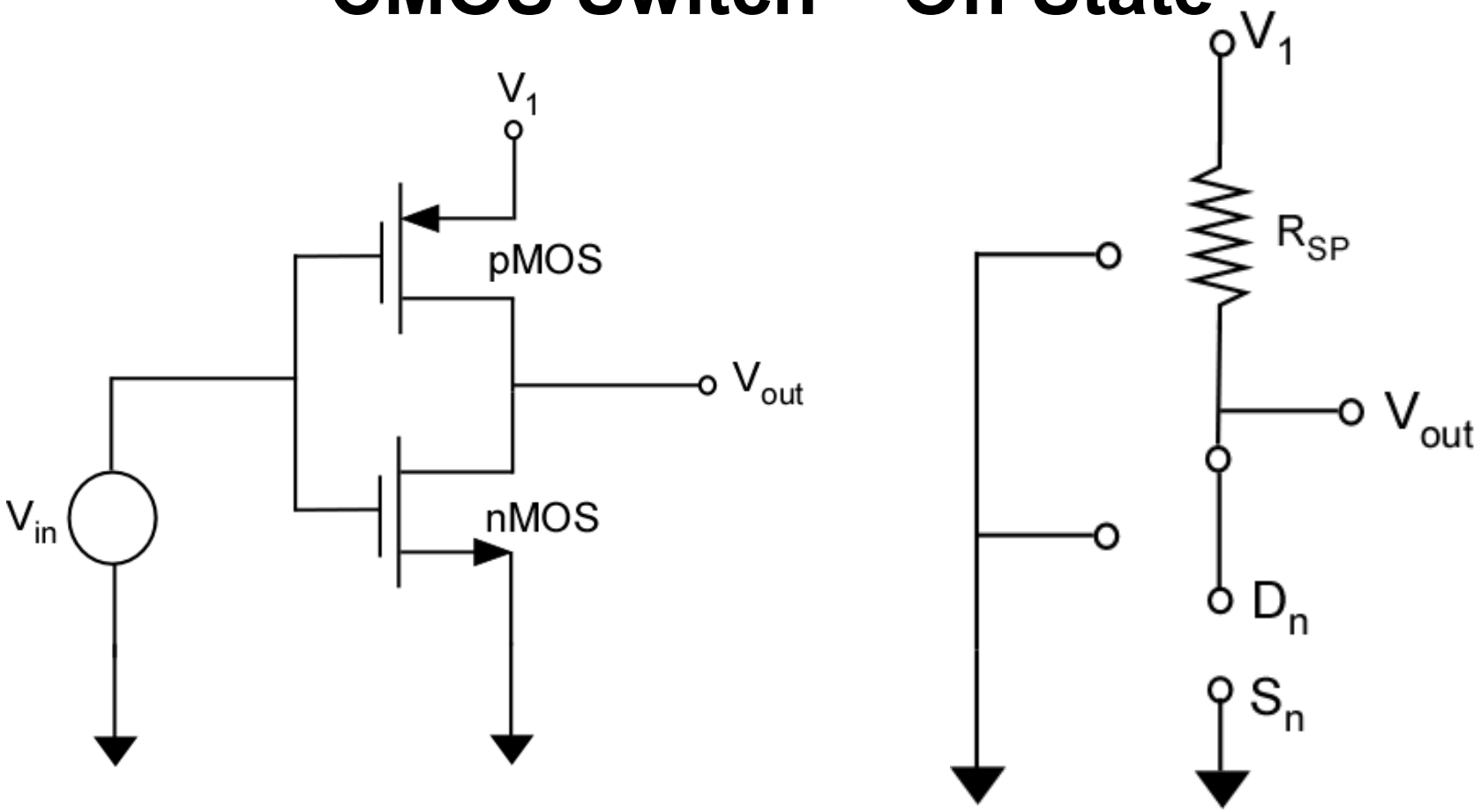
CMOS Switch



CMOS switch is called an inverter

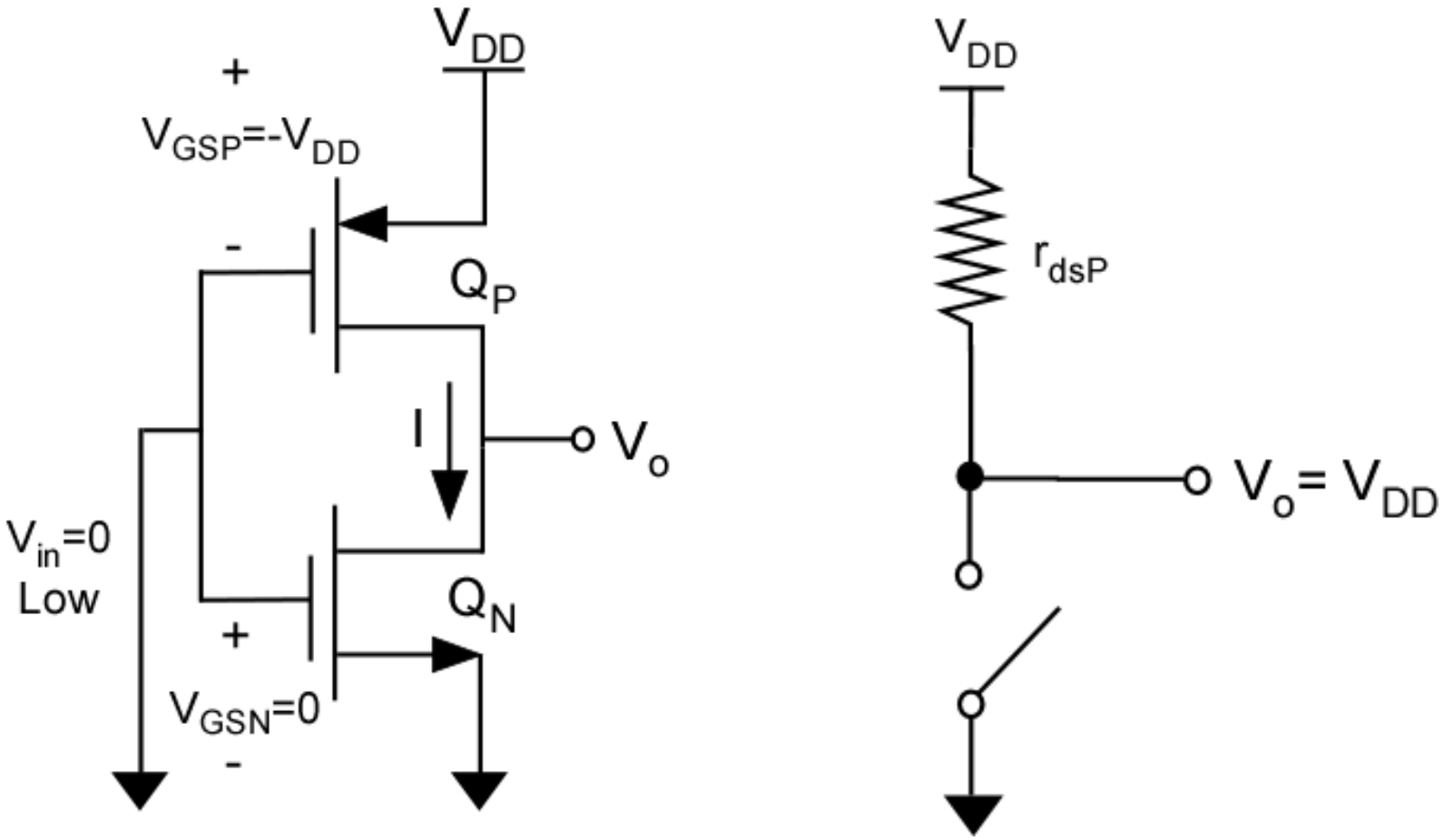
The body of each device is connected to its source ➔ NO BODY EFFECT

CMOS Switch – Off State

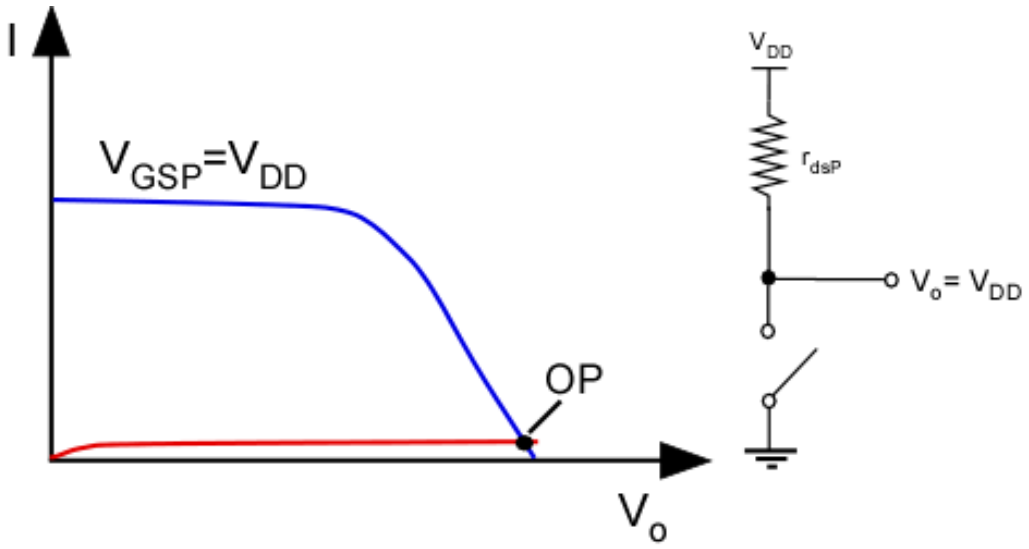


- **OFF State (V_{in}: low)**
  - nMOS transistor is off
  - Path from V_{out} to V_1 is through PMOS ➔V_{out}: high

CMOS Switch – Input Low



CMOS Switch – Input Low



NMOS

$$V_{GSN} < V_{TN} \Rightarrow OFF$$

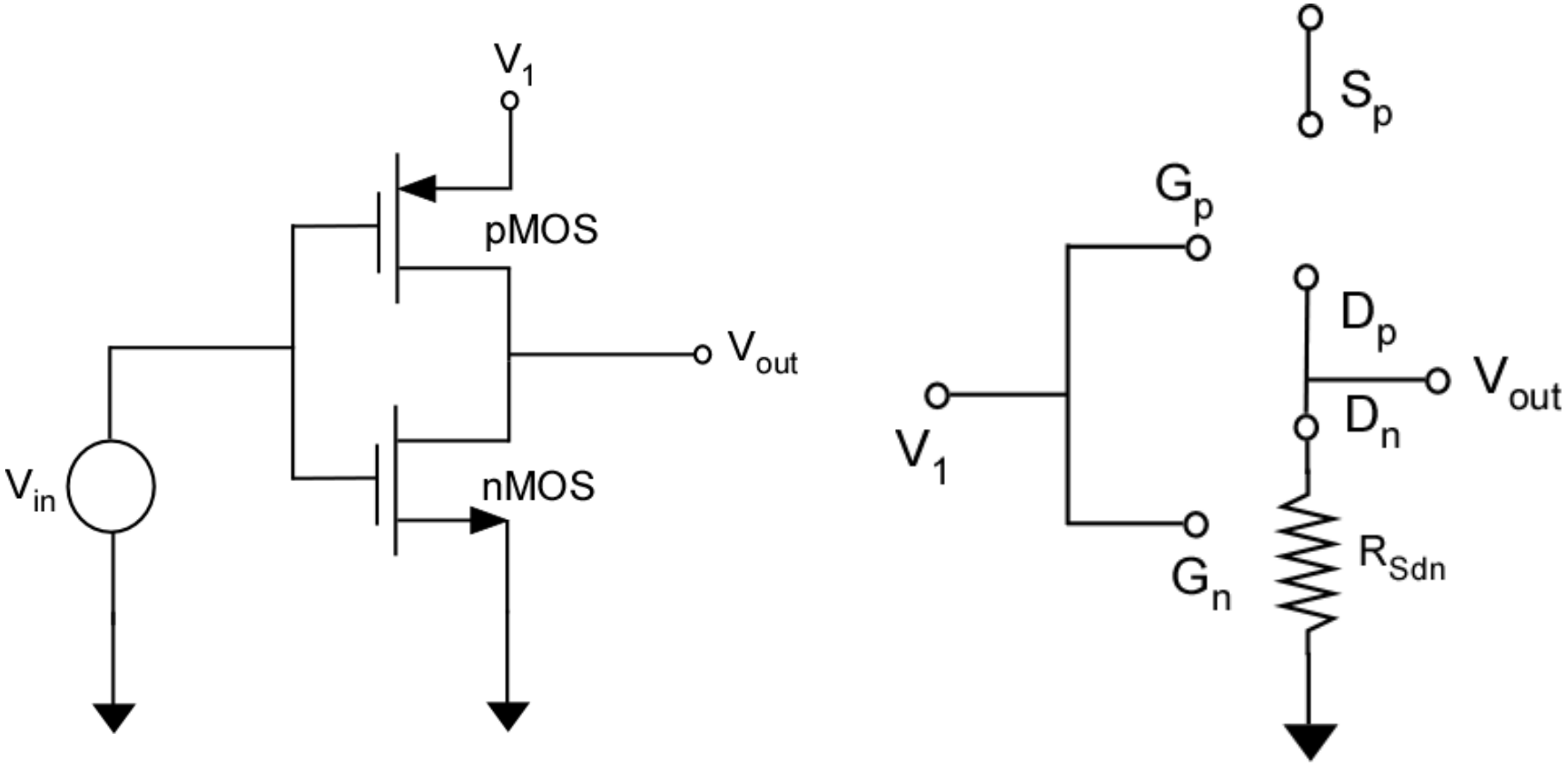
r_{dsn} high

PMOS

$$r_{dsp} = \frac{1}{k_p'\left(\frac{W}{L}\right)_p\left(V_{DD} - |V_{TP}|\right)}$$

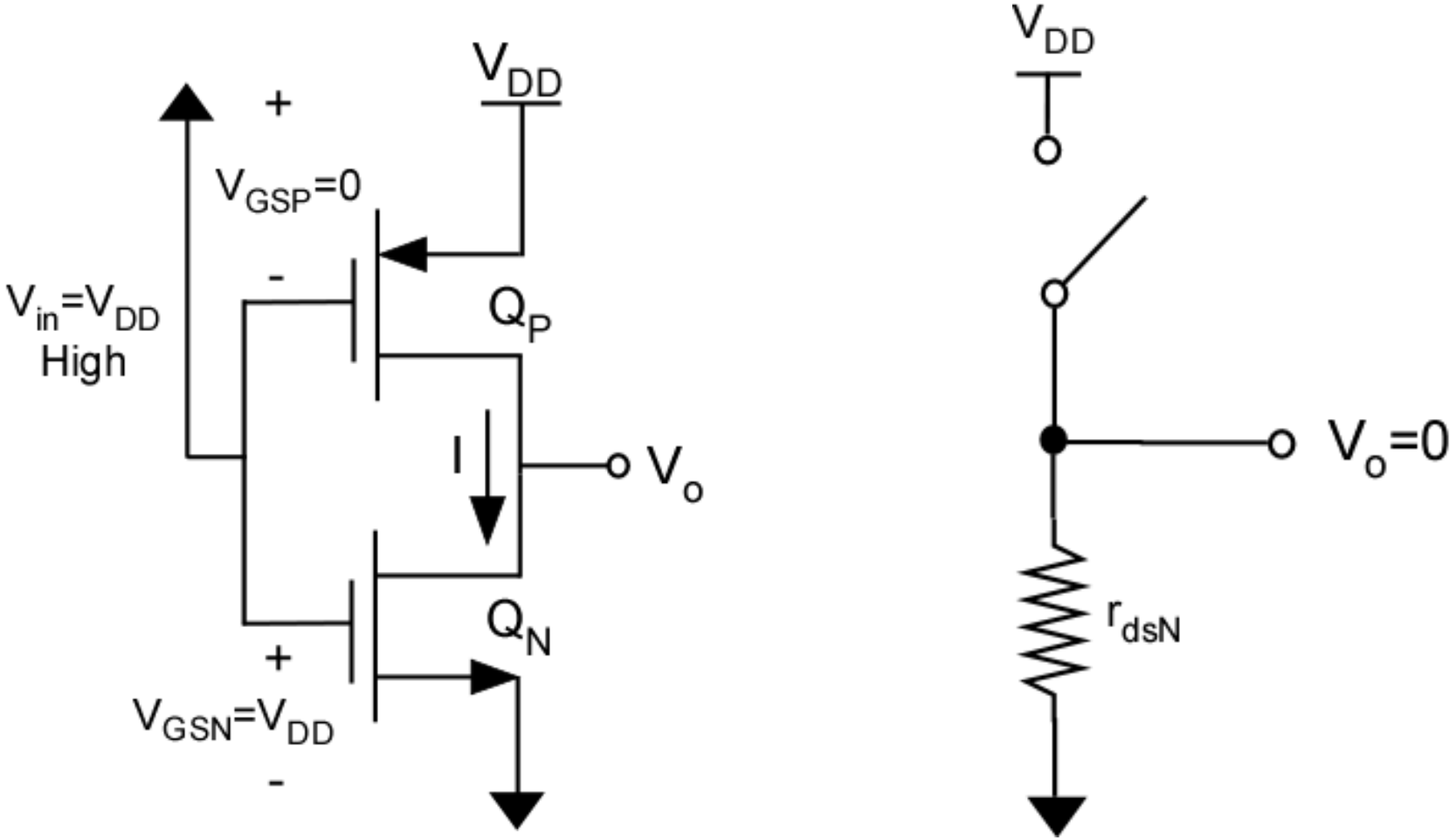
r_{dsp} is low

CMOS Switch – On State



- **ON State (V_{in}: high)**
  - pMOS transistor is off
  - Path from V_{out} to ground is through nMOS ➔V_{out}: low

CMOS Switch – Input High

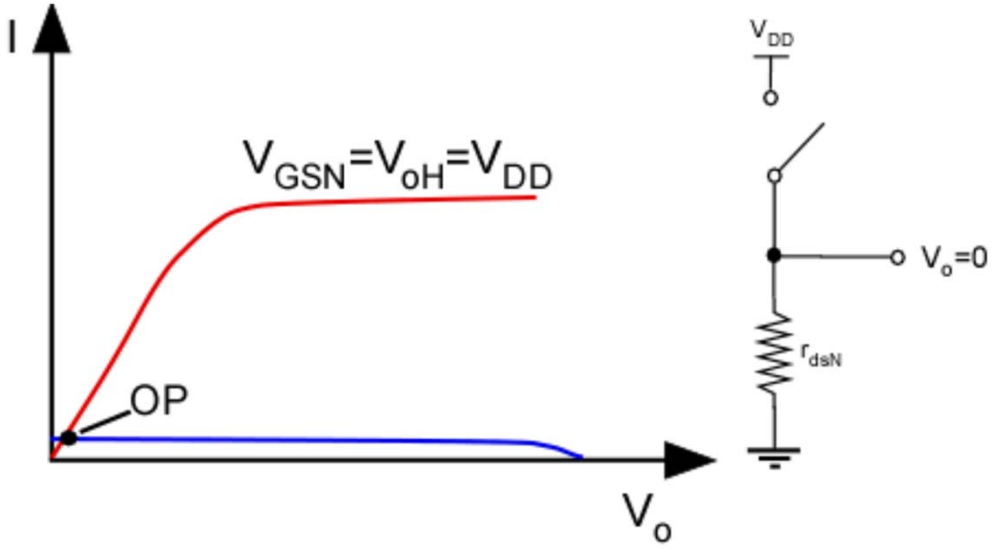


CMOS Switch – Input High

NMOS

$$r_{dsn} = \frac{1}{k_n'\left(\frac{W}{L}\right)_n \left(V_{DD} - V_{TN}\right)}$$

r_{dsn} is low

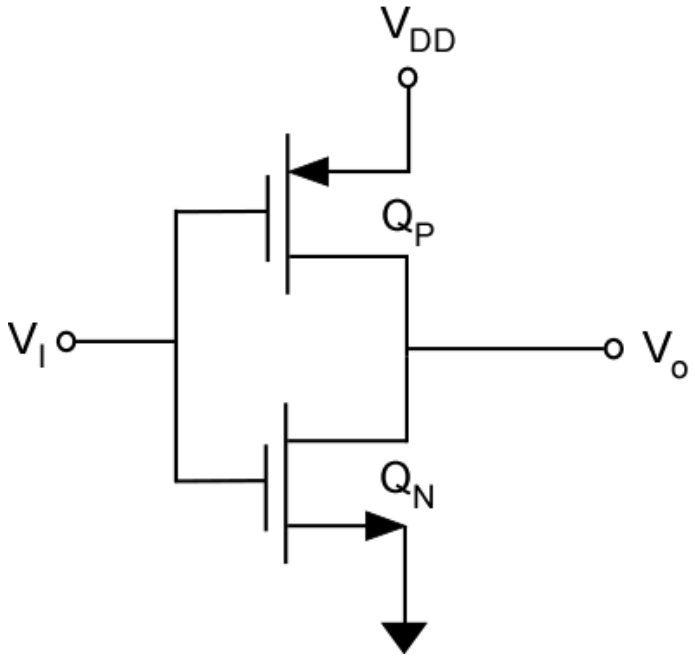


PMOS

$$V_{GSP} > V_{TP} \Rightarrow OFF$$

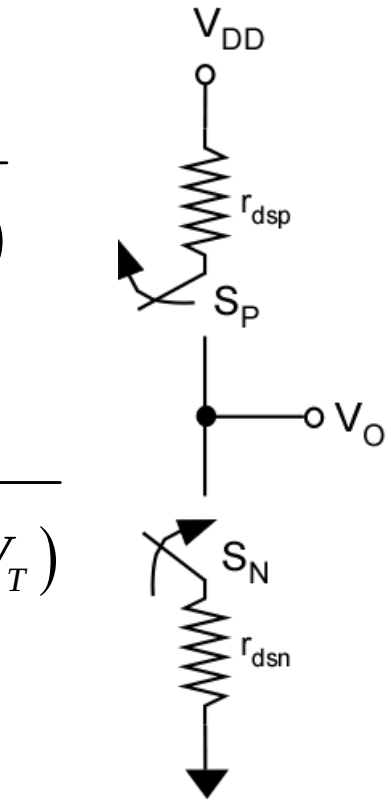
r_{dsp} high

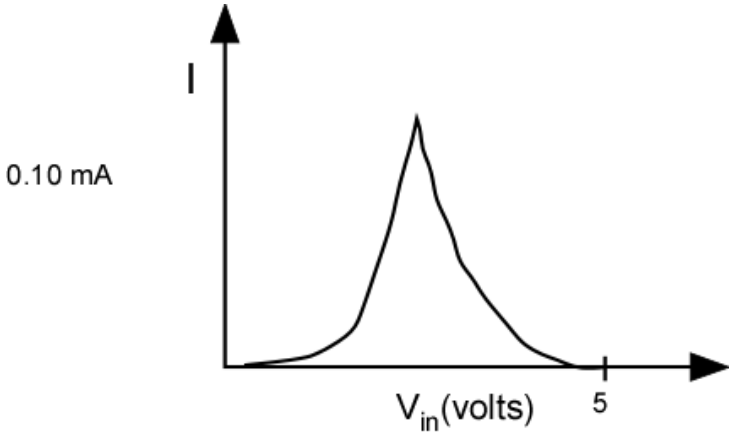
CMOS Inverter



$$r_{dsn} = \frac{1}{k_N' \left(\frac{W}{L}\right)_n \left(V_{DD} - V_T\right)}$$

$$r_{dsp} = \frac{1}{k_P' \left(\frac{W}{L}\right)_p \left(V_{DD} - V_T\right)}$$





Short switching transient current ➔ low power

CMOS Inverter

Advantages of CMOS inverter

- Output voltage levels are 0 and V_{DD} ➔ signal swing is maximum possible
- Static power dissipation is zero
- Low resistance paths to V_{DD} and ground when needed
- High output driving capability ➔ increased speed
- Input resistance is infinite ➔ high fan-out

Load driving capability of CMOS is high. Transistors can sink or source large load currents that can be used to charge and discharge load capacitances.