ECE 342
Electronic Circuits

Lecture 33
CMOS Characteristics

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Digital Circuits

V_{IH}: Input voltage at high state ➔ V_{IHmin}
V_{IL}: Input voltage at low state ➔ V_{ILmax}
V_{OH}: Output voltage at high state ➔ V_{OHmin}
V_{OL}: Output voltage at low state ➔ V_{OLmin}

Likewise for current we can define

Currents into input

I_{IH} ➔ I_{IHmax}
I_{IL} ➔ I_{ILmax}

Currents into output

I_{OH} ➔ I_{OHmax}
I_{OL} ➔ I_{OLmax}

Voltage Transfer Characteristics (VTC)

The static operation of a logic circuit is determined by its VTC

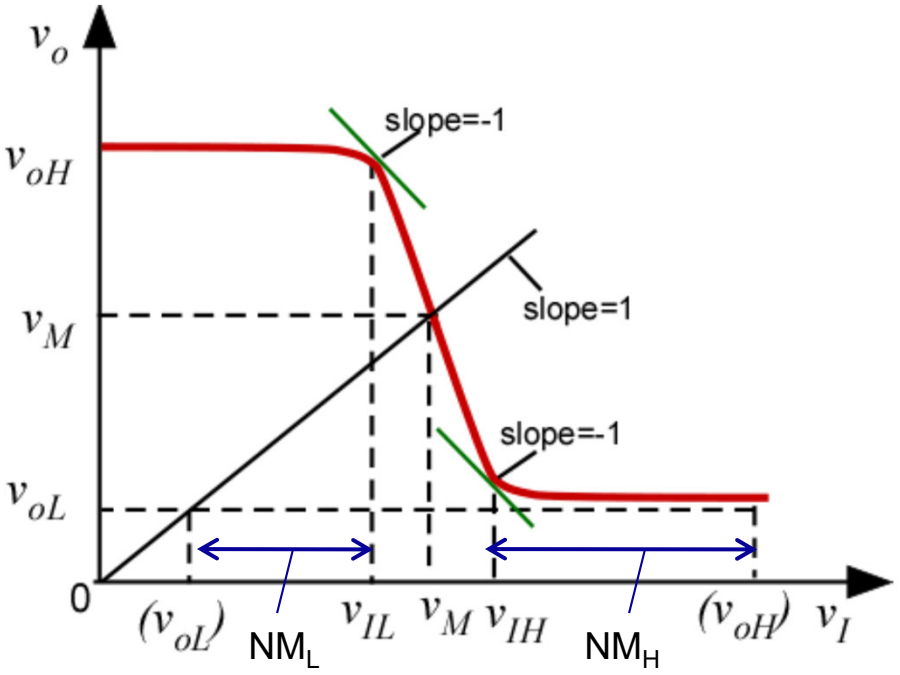
- **In low state: noise margin is *NM_L***

$$NM_L = V_{IL} - V_{OL}$$

- **In high state: noise margin is *NM_H***

$$NM_H = V_{OH} - V_{IH}$$

- **An ideal VTC will maximize noise margins**



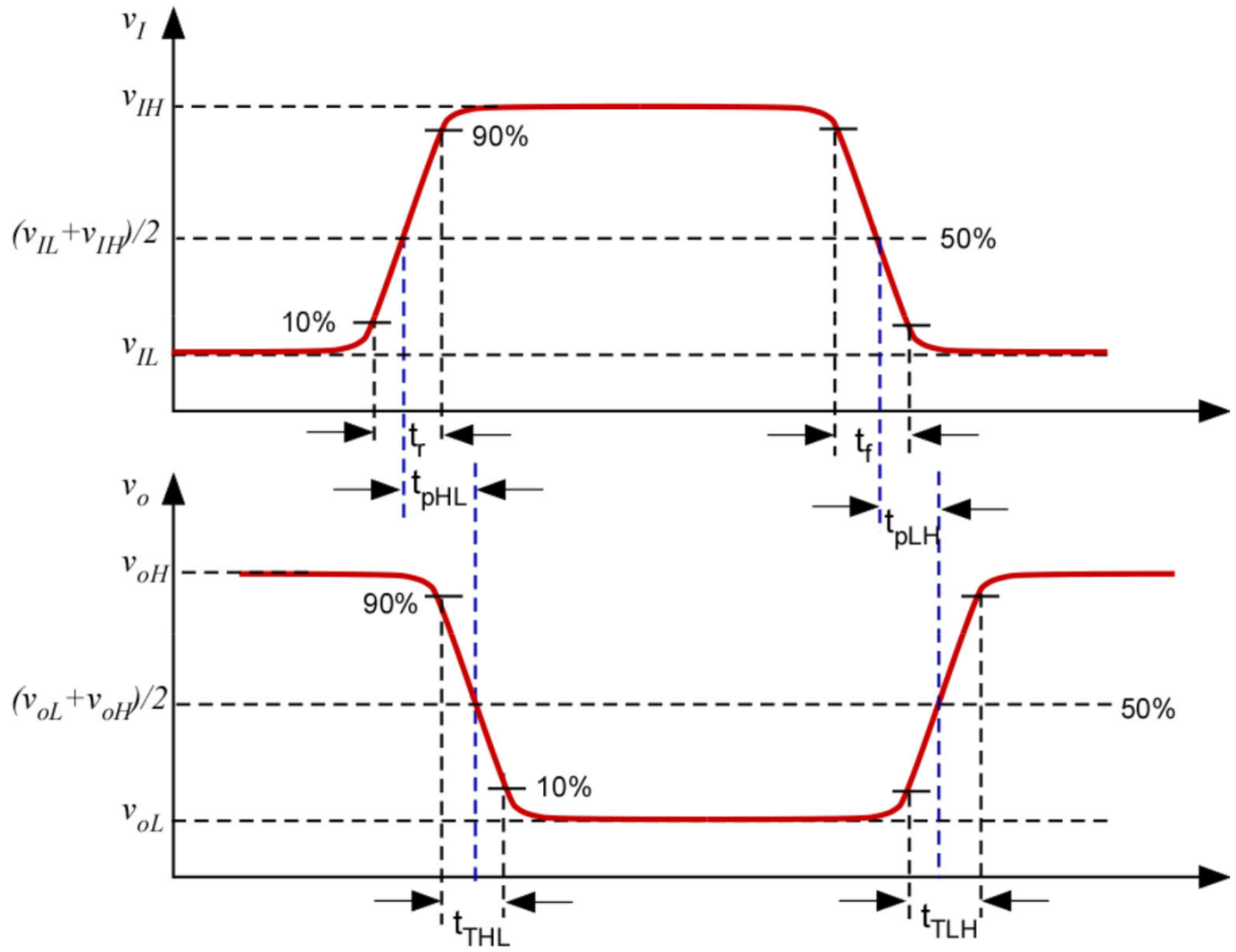
V_{IL} and V_{IH} are the points where the slope of the VTC=-1

Optimum: $NM_L = NM_H = V_{DD}/2$

Switching Time & Propagation Delay

input

output



Switching Time & Propagation Delay

t_r=rise time (from 10% to 90%)
t_f=fall time (from 90% to 10%)
t_{pLH}=low-to-high propagation delay
t_{pHL}=high-to-low propagation delay

Inverter propagation delay:

$$t_p = \frac{1}{2}\left(t_{pLH} + t_{pHL}\right)$$

VTC and Noise Margins

For a logic-circuit family employing a 3-V supply, suggest an ideal set of values for V_{th}, V_{IL}, V_{IH}, V_{OH}, NM_L, NM_H. Also, sketch the VTC. What value of voltage gain in the transition region does your ideal specification imply?

Ideal 3V logic implies:

$$V_{OH} = V_{DD} = 3.0V; \qquad V_{OL} = 0.0V$$

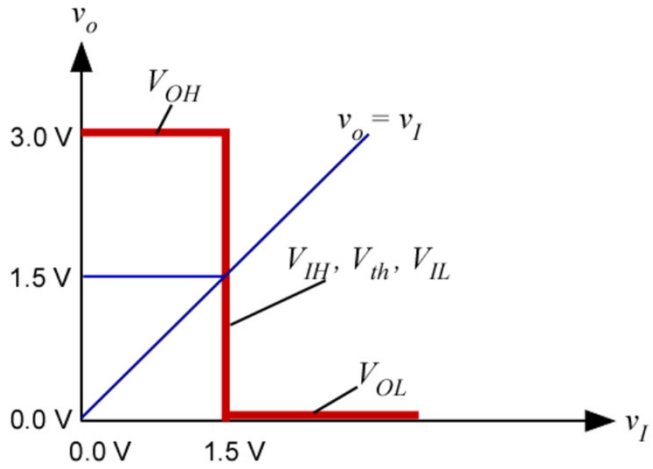
$$V_{th} = V_{DD} / 2 = 3.0 / 2 = 1.5V;$$

$$V_{IL} = V_{DD} / 2 = 1.5V; \quad V_{IH} = V_{DD} / 2 = 1.5V$$

VTC and Noise Margins

$$NM_H = V_{OH} - V_{IH} = 3.0 - 1.5 = 1.5V$$

$$NM_L = V_{IL} - V_{OL} = 1.5 - 0.0 = 1.5V$$



Inverting transfer characteristics

The gain in the transition region is:

$$\left(V_{OH} - V_{OL}\right) / \left(V_{IH} - V_{IL}\right) = \left(3.0 - 0.0\right) / \left(1.5 - 1.5\right)$$

$$= 3 / 0 = \infty\, V / V$$

CMOS Noise Margins

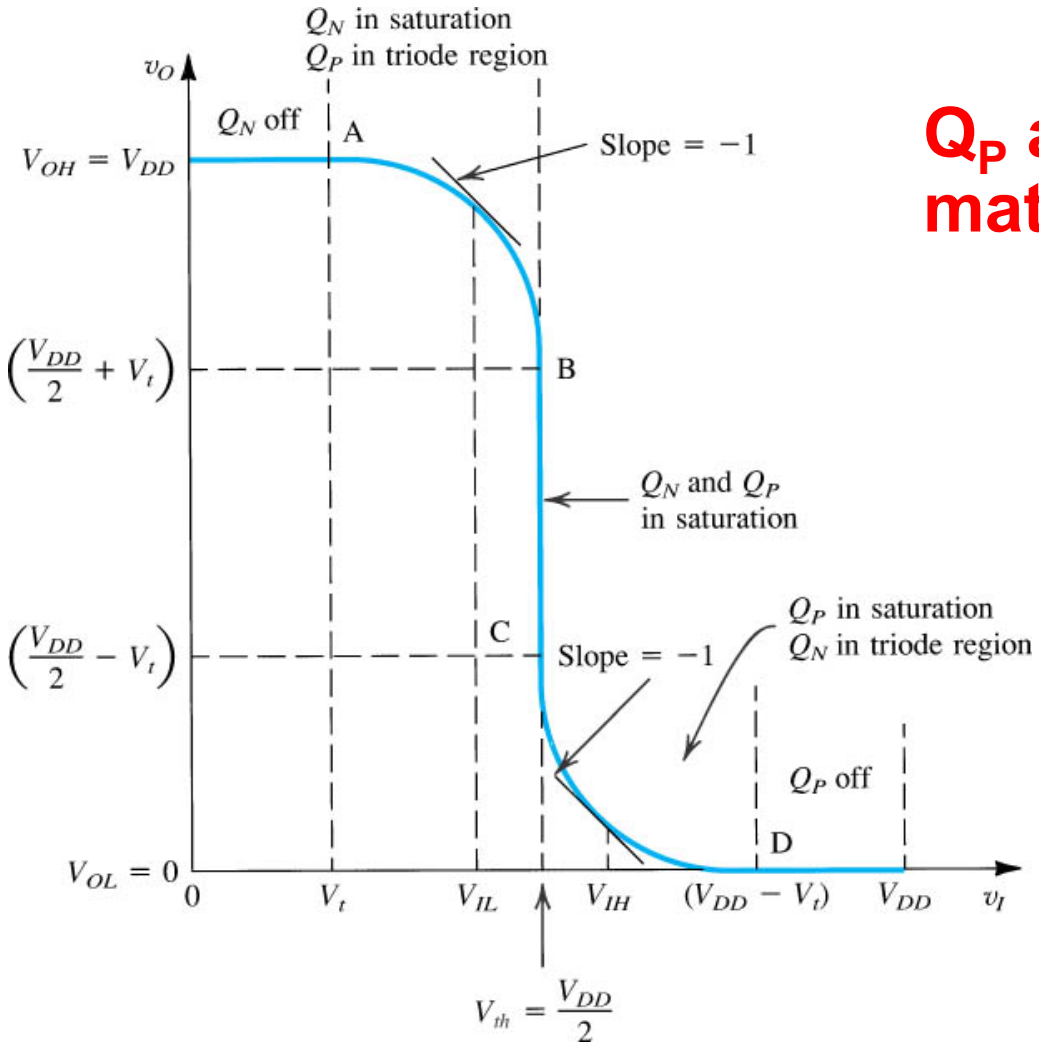
When inverter threshold is at $V_{DD}/2$, the noise margin NM_H and NM_L are equalized

$$NM_H = NM_L = \frac{3}{8}\left(V_{DD} + \frac{2}{3}V_{th}\right)$$

NM_H: noise margin for high input
NM_L: noise margin for low input
V_{th}: threshold voltage

Noise margins are typically around 0.4 V_{DD}; close to half power-supply voltage ➔ CMOS ideal from noise-immunity standpoint

CMOS Inverter VTC



Q_P and Q_N are matched

CMOS Inverter VTC

Derivation

- Assume that transistors are matched
- Vertical segment of VTC is when both Q_N and Q_P are saturated
- No channel length modulation effect ➔ $\lambda = 0$
- Vertical segment occurs at $v_i = V_{DD}/2$
- V_{IL}: maximum permitted logic-0 level of input (slope=-1)
- V_{IH}: minimum permitted logic-1 level of input (slope=-1)

To determine V_{IH}, assume Q_N in triode region and Q_P in saturation region

$$\left(v_I - V_t\right)v_o - \frac{1}{2}v_o^2 = \frac{1}{2}\left(V_{DD} - v_I - V_t\right)^2$$

Next, we differentiate both sides relative to v_i

$$\left(v_I - V_t\right)\frac{dv_o}{dv_I} + v_o - v_o\frac{dv_o}{dv_I} = -\left(V_{DD} - v_I - V_t\right)$$

CMOS Inverter VTC

Substitute $v_i = V_{IH}$ and $dv_o/dv_i = -1$

$$v_o = V_{IH} - \frac{V_{DD}}{2}$$

After substitutions, we get

$$V_{IH} = \frac{1}{8}\left(5V_{DD} - 2V_t\right)$$

Same analysis can be repeated for V_{IL} to get

$$V_{IL} = \frac{1}{8}\left(3V_{DD} + 2V_t\right)$$

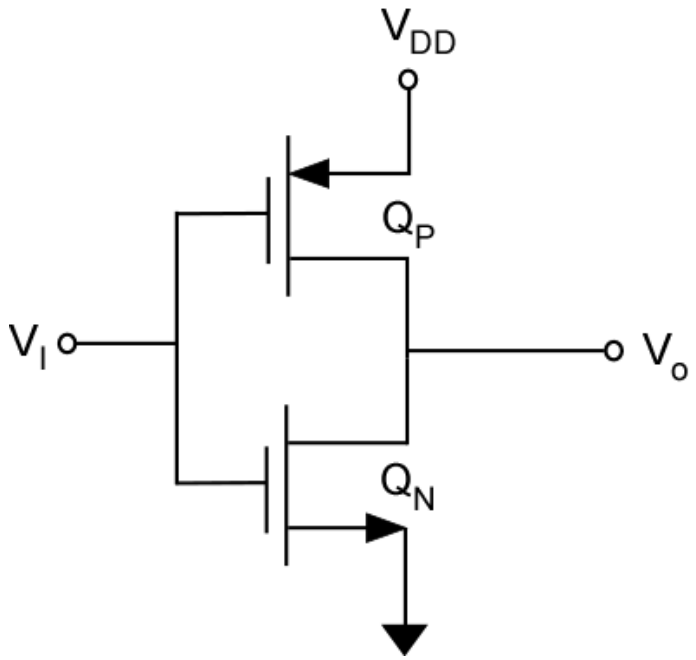
CMOS Inverter Noise Margins

$$V_{IH} = \frac{1}{8}\left(5V_{DD} - 2V_t\right)$$

$$V_{IL} = \frac{1}{8}\left(3V_{DD} + 2V_t\right)$$

$$NM_H = \frac{1}{8}\left(3V_{DD} + 2V_t\right)$$

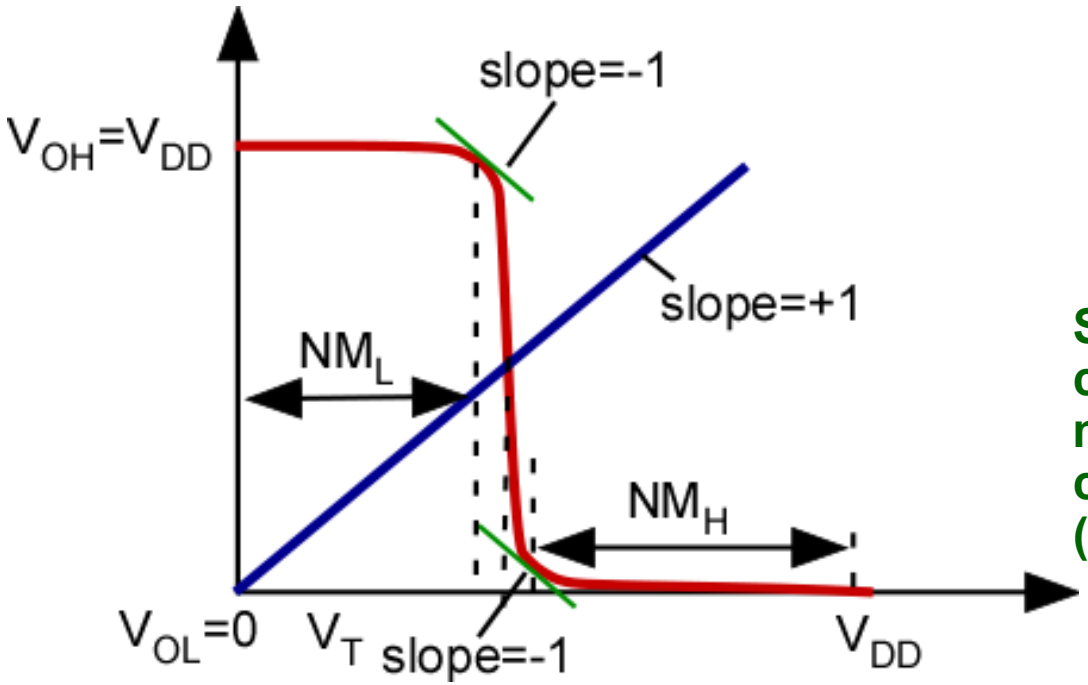
$$NM_L = \frac{1}{8}\left(3V_{DD} + 2V_t\right)$$



Symmetry in VTC ➔ equal noise margins

Matched CMOS Inverter VTC

CMOS inverter can be made to switch at specific threshold voltage by appropriately sizing the transistors



$$\left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_n$$

Symmetrical transfer characteristics is obtained via matching ➔ equal current driving capabilities in both directions (pull-up and pull-down)

VTC and Noise Margins - Problem

An inverter is designed with equal-sized NMOS and PMOS transistors and fabricated in a 0.8-micron CMOS technology for which k_n' = 120 μA/V², k_p' = 60 μA/V², V_{tn} =|V_{tp}|=0.7 V, V_{DD} = 3V, L_n=L_p = 0.8 μm, W_n = W_p = 1.2 μm, find V_{IL}, V_{IH} and the noise margins.

Equal sizes NMOS and PMOS, but $k_n'=2k_p'$

V_t = 0.7V

For V_{IH}: Q_N in triode and Q_P in saturation

$$k_n'\left(\frac{W}{L}\right)_n\left[(V_I-V_t)V_o-\frac{1}{2}V_o^2\right]=\frac{1}{2}k_p'\left(\frac{W}{L}\right)_p(V_{DD}-V_I-V_t)^2$$

VTC and Noise Margins – Problem (cont')

$$4\left(V_I - V_t\right)V_o - 2V_o^2 = \left(V_{DD} - V_I - V_t\right)^2 \qquad (1)$$

Differentiating both sides relative to V_I results in:

$$\frac{\partial}{\partial V_I}: \; 4\left(V_I - V_t\right)\frac{\partial V_o}{\partial V_I} + 4V_o - 4V_o\frac{\partial V_o}{\partial V_I} = 2\left(V_{DD} - V_I - V_t\right)(-1)$$

Substitute the values together with:

$$V_I = V_{IH} \quad \text{and} \quad \frac{\partial V_o}{\partial V_I} = -1$$

VTC and Noise Margins – Problem (cont')

$$4\left(V_{IH}-0.7\right)\left(-1\right)+4V_o+4V_o=2\left(V_{IH}-3+0.7\right)$$

$$V_{IH}=\frac{8V_o+7.4}{6}=1.33V_o+1.23 \qquad (2)$$

$$\text{From (1):}\ 4\left(V_{IH}-0.7\right)V_o-2V_o^2=\left(3-V_{IH}-0.7\right)^2$$

$$4\left(V_{IH}-0.7\right)V_o-2V_o^2=\left(2.3-V_{IH}\right)^2 \qquad (3)$$

$$\text{solving (2) \& (3):}\ 1.55V_o^2+4.97V_o-1.14=0$$

$$\Rightarrow V_o=0.22\,V \qquad V_{IH}=1.52\,V$$

VTC and Noise Margins – Problem (cont')

For V_{IL}: Q_N is in saturation and Q_P in triode

$$\frac{1}{2}k_n'\left(\frac{W}{L}\right)_n\left(V_I-V_t\right)^2=k_p'\left(\frac{W}{L}\right)_p\left[\left(V_{DD}-V_I-V_t\right)\left(V_{DD}-V_o\right)-\frac{1}{2}\left(V_{DD}-V_o\right)^2\right]$$

$$\left(V_I-0.7\right)^2=\left(3-V_I-0.7\right)\left(3-V_o\right)-\frac{1}{2}\left(3-V_o\right)^2 \qquad (1)$$

$$\left(V_I-0.7\right)^2=\left(2.3-V_I\right)\left(3-V_o\right)-\frac{1}{2}\left(3-V_o\right)^2$$

$$\frac{\partial}{\partial V_I}\Rightarrow 2\left(V_I-0.7\right)=\left(2.3-V_I\right)\left(-\frac{\partial V_o}{\partial V_I}\right)-\left(3-V_o\right)+\left(3-V_o\right)\frac{\partial V_o}{\partial V_I}$$

VTC and Noise Margins – Problem (cont')

$$V_I = V_{IL} \text{ and } \frac{\partial V_o}{\partial V_I} = -1$$

$$2V_{IL} - 1.4 = 2.3 - V_{IL} - 3 + V_o + 3 + V_o$$

$$V_{IL} = \frac{2}{3}V_o - 1.15$$

$$\text{From (1)}: \left(V_{IL} - 0.7\right)^2 = \left(2.3 - V_{IL}\right)\left(3 - V_o\right) - \frac{1}{2}\left(3 - V_o\right)^2$$

$$\left(0.66V_o - 1.85\right)^2 = \left(3.45 - 0.66V_o\right)\left(3 - V_o\right) - \frac{1}{2}\left(3 - V_o\right)^2$$

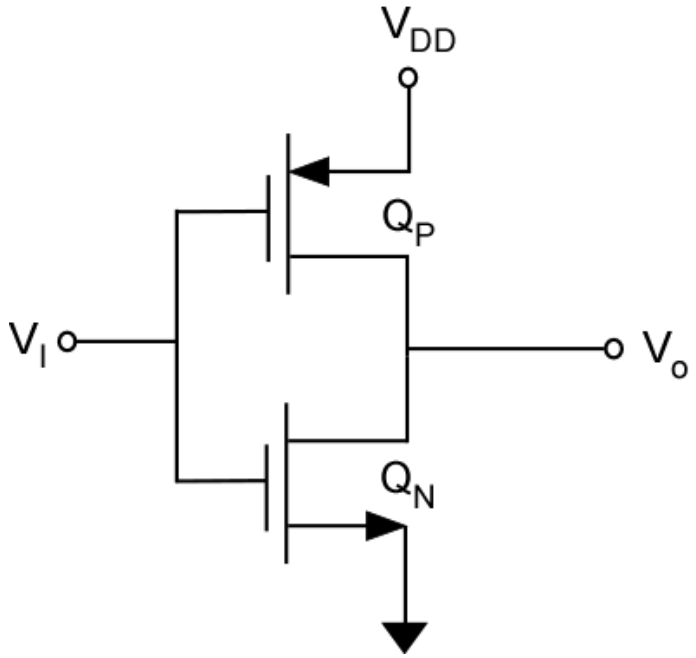
VTC and Noise Margins – Problem (cont')

$$V_o = 2.96\,V \qquad V_{IL} = 0.81\,V$$

Noise Margins:

$$NM_H = 3 - 1.52 = 1.48\,V$$

$$NM_L = 0.81 - 0 = 0.81\,V$$



Since Q_N and Q_P are not matched, the VTC is not symmetric