ECE 342
Electronic Circuits

Lecture 34
CMOS Delay Model

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Digital Circuits

V_{IH}: Input voltage at high state ➔ V_{IHmin}
V_{IL}: Input voltage at low state ➔ V_{ILmax}
V_{OH}: Output voltage at high state ➔ V_{OHmin}
V_{OL}: Output voltage at low state ➔ V_{OLmin}

Likewise for current we can define

Currents into input

I_{IH} ⬌ I_{IHmax}
I_{IL} ⬌ I_{ILmax}

Currents into output

I_{OH} ⬌ I_{OHmax}
I_{OL} ⬌ I_{OLmax}

Voltage Transfer Characteristics (VTC)

The static operation of a logic circuit is determined by its VTC
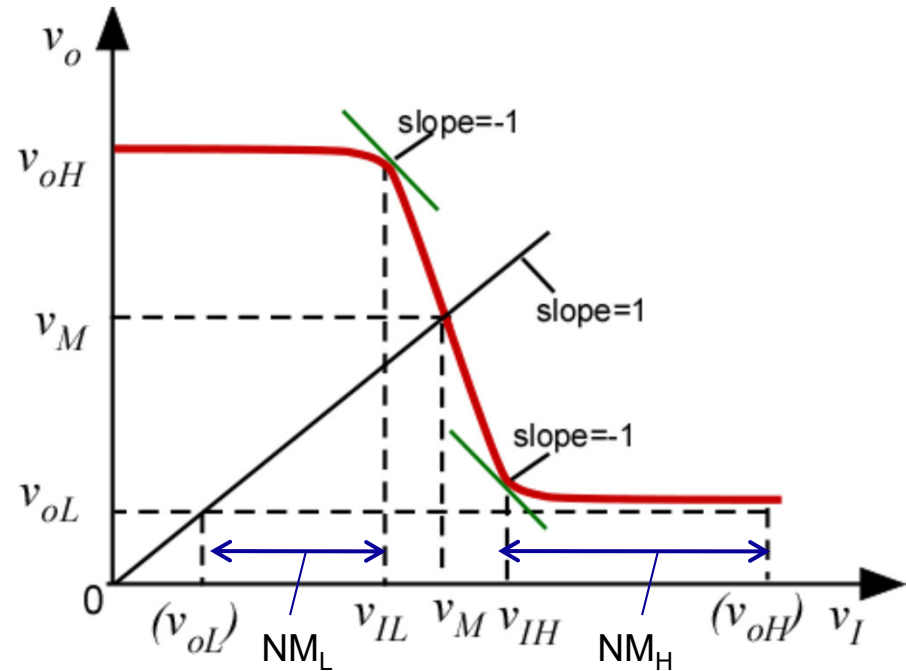
- **In low state: noise margin is NM_L**

$$NM_L = V_{IL} - V_{OL}$$

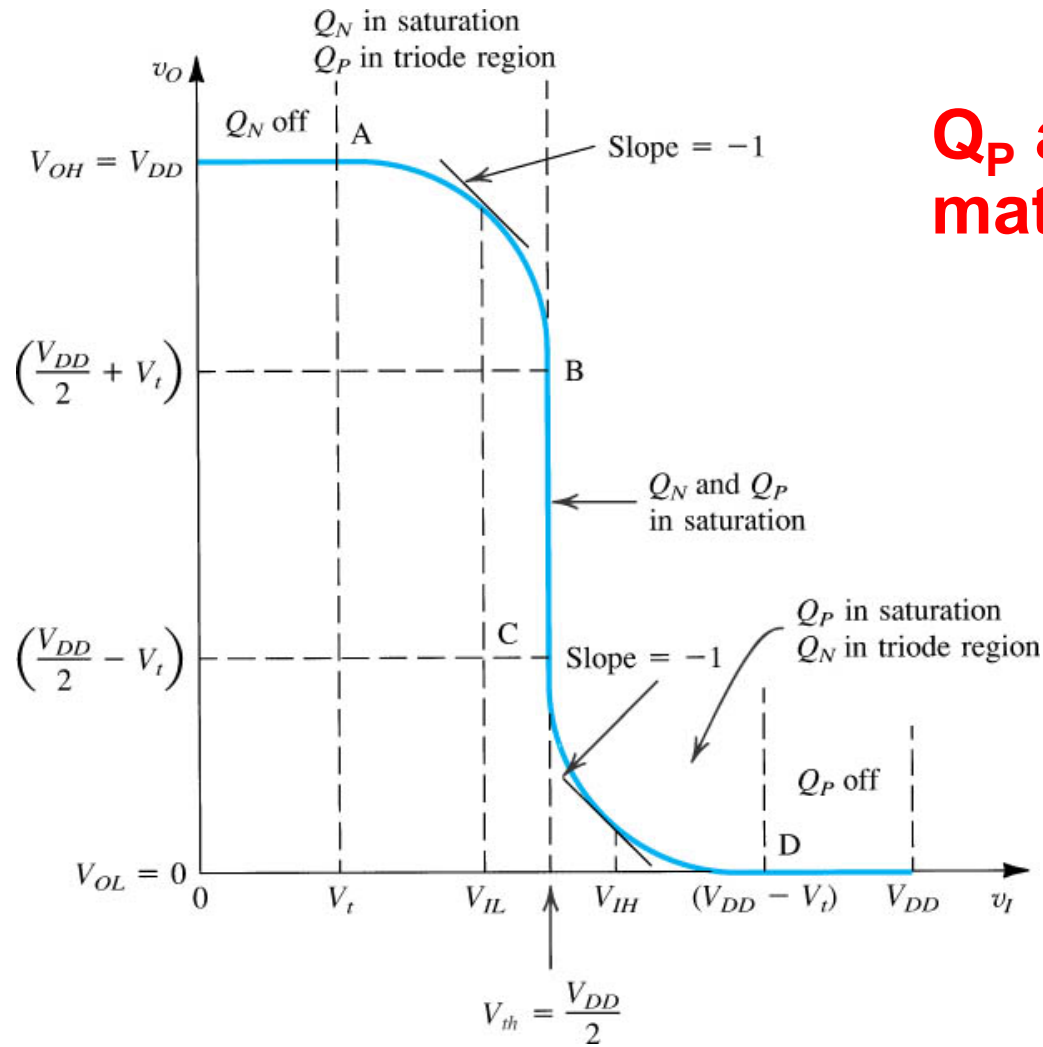- **In high state: noise margin is NM_H**

$$NM_H = V_{OH} - V_{IH}$$

- **An ideal VTC will maximize noise margins**

V_{IL} and V_{IH} are the points where the slope of the VTC=-1

Optimum: $\quad NM_L = NM_H = V_{DD}/2$

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CMOS Inverter VTC

Q_P and Q_N are matched

CMOS Inverter VTC

Derivation

- ➢ **Assume that transistors are matched**
- ➢ **Vertical segment of VTC is when both Q_N and Q_P are saturated**
- ➢ **No channel length modulation effect ➔ $\lambda = 0$**
- ➢ **Vertical segment occurs at $v_i = V_{DD}/2$**
- ➢ **V_{IL}: maximum permitted logic-0 level of input (slope=-1)**
- ➢ **V_{IH}: minimum permitted logic-1 level of input (slope=-1)**

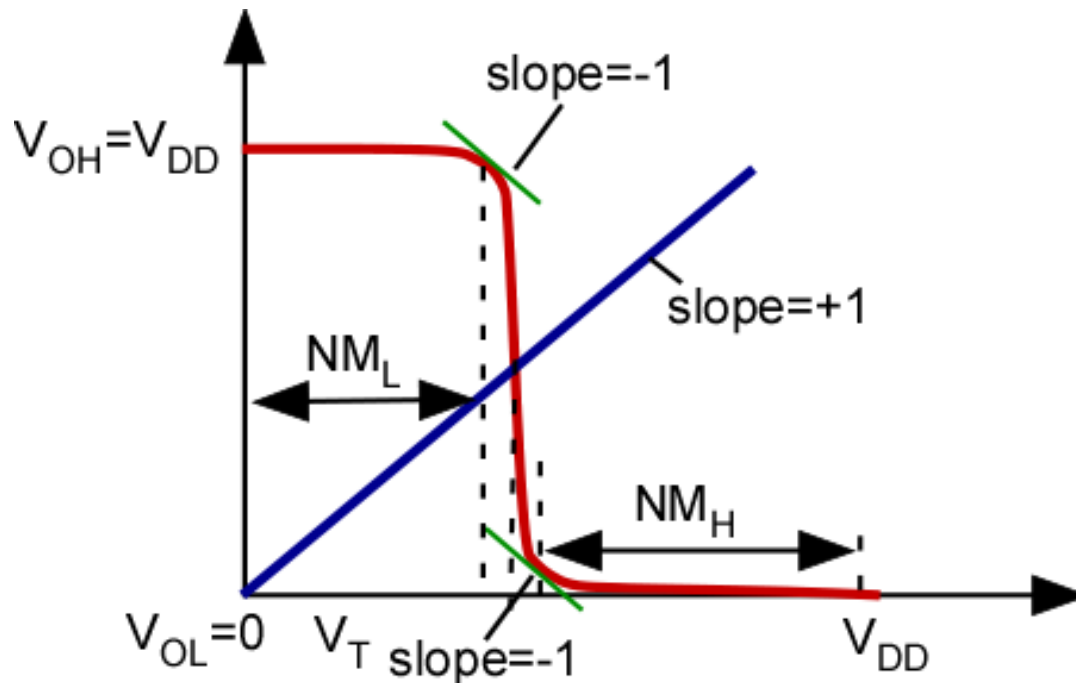**CMOS inverter can be made to switch at $V_{DD}/2$ by appropriate sizing**

LOGIC Threshold:
$$V_M = V_{th} = \frac{V_{DD} - |V_{tp}| + \sqrt{k_n / k_p} V_{tn}}{1 + \sqrt{k_n / k_p}}$$

where $\quad k_n = k_n^{'}\left(W/L\right)_n \; and \; k_p = k_p^{'}\left(W/L\right)_p$
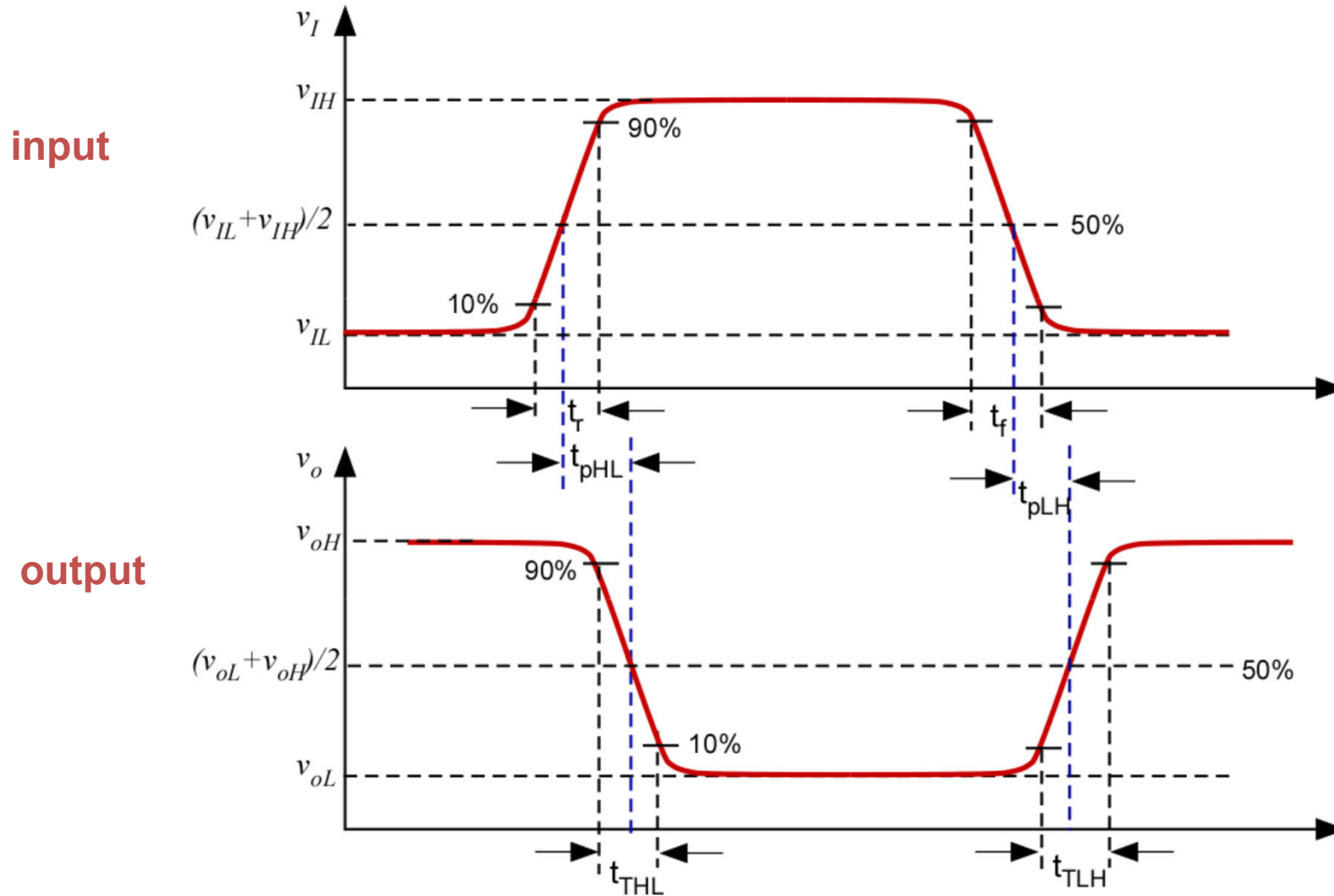
Matched CMOS Inverter VTC

CMOS inverter can be made to switch at specific threshold voltage by appropriately sizing the transistors

$$\left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_n$$

Symmetrical transfer characteristics is obtained via matching ➔ equal current driving capabilities in both directions (pull-up and pull-down)

Switching Time & Propagation Delay

Switching Time & Propagation Delay
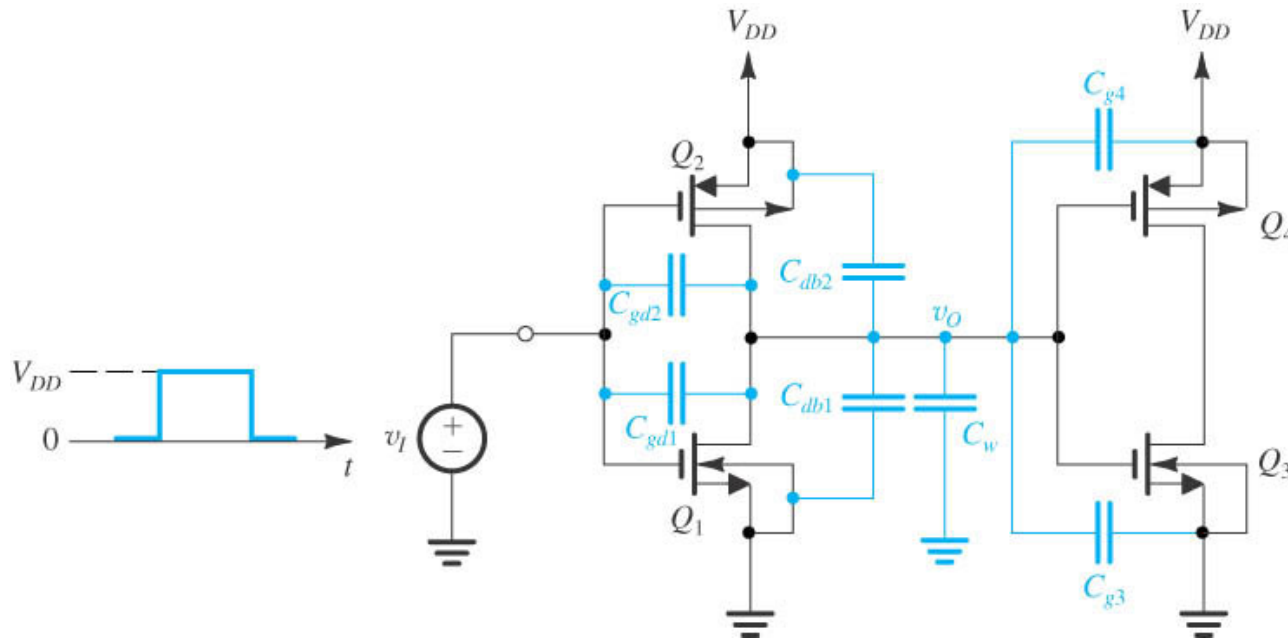
t_r=rise time (from 10% to 90%)
t_f=fall time (from 90% to 10%)
t_{pLH}=low-to-high propagation delay
t_{pHL}=high-to-low propagation delay

Inverter propagation delay:

$$t_p = \frac{1}{2}\left(t_{pLH} + t_{pHL}\right)$$
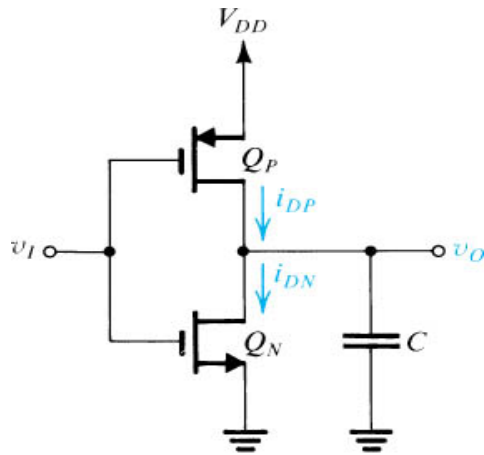
CMOS Dynamic Operation

- ➤ **Exact analysis is too tedious**
- ➤ **Replace all the capacitances in the circuit by a single equivalent capacitance C connected between the output node of the inverter and ground**
- ➤ **Analyze capacitively loaded inverter to determine propagation delay**

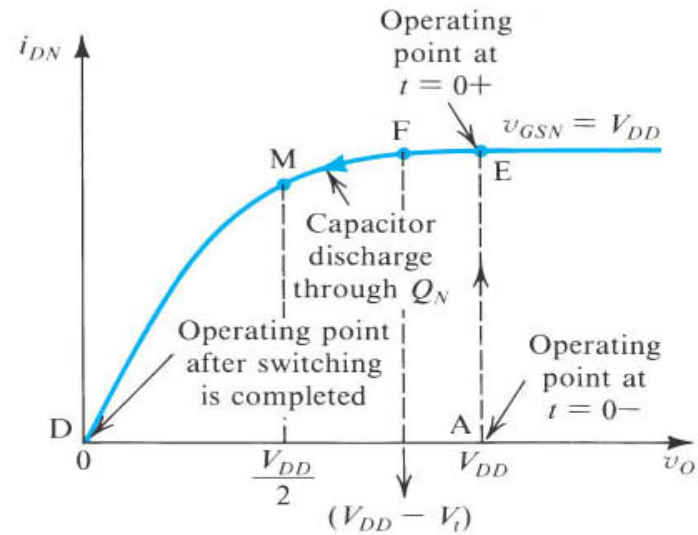# CMOS – Dynamic Operation
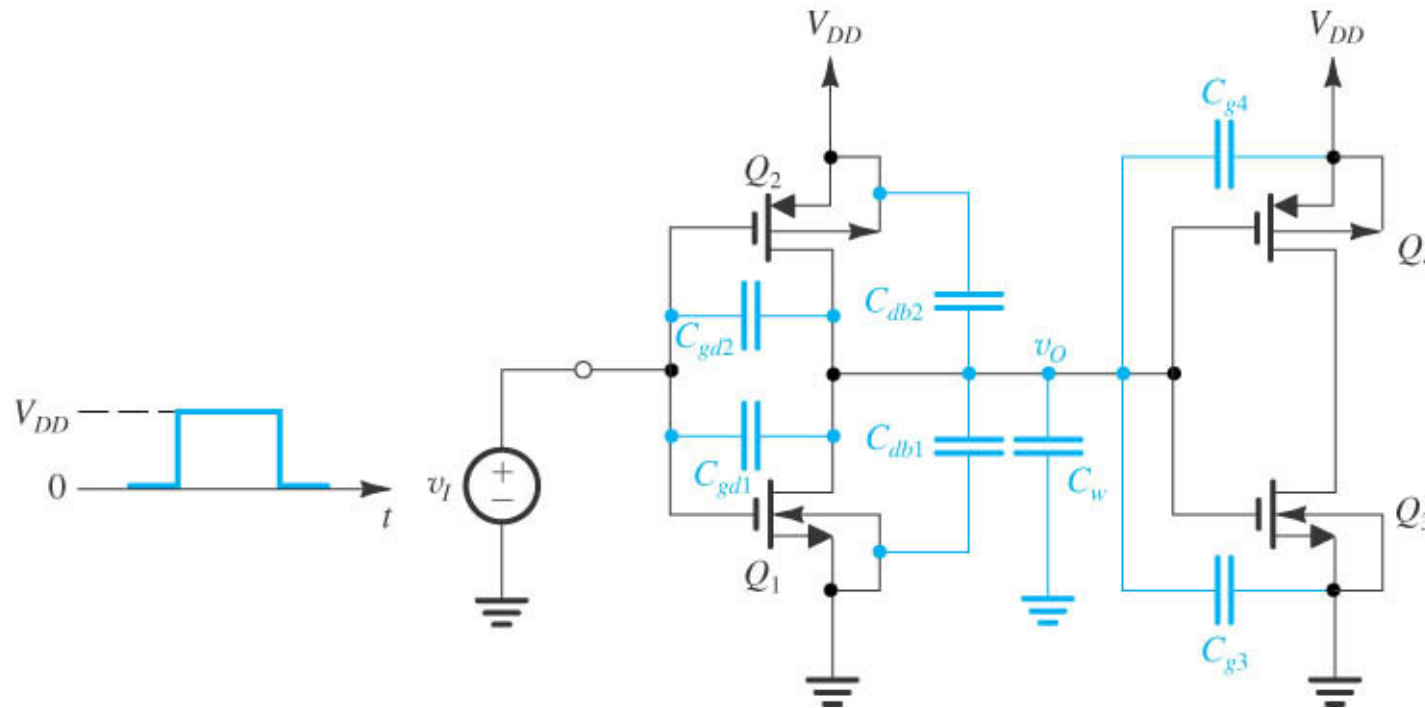
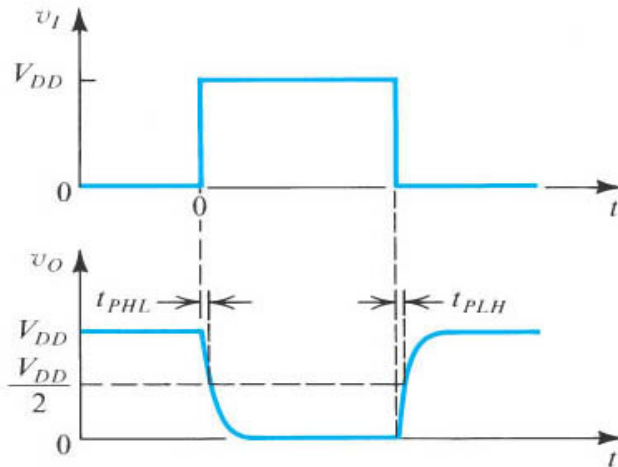$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$$
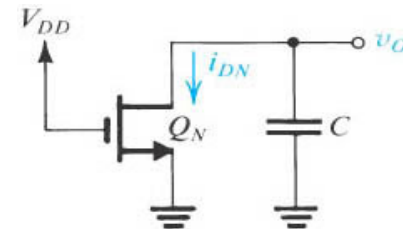
CMOS – Dynamic Operation

(a)

(b)

(c)

(d)

CMOS Dynamic Operation

Need interval t_{PHL} during which v_o reduces from V_{DD} to $V_{DD}/2$

$$I_{av} t_{PHL} = C\left[V_{DD} - \left(V_{DD}/2\right)\right]$$

Which gives

$$t_{PHL} = \frac{C V_{DD}}{2 I_{av}}$$

I_{av} is given by

$$I_{av} = \frac{1}{2}\left[i_{DN}\left(E\right) + i_{DN}\left(M\right)\right]$$

CMOS Dynamic Operation

where

$$i_{DN}(E) = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})^2$$

and

$$i_{DN}(M) = k_n'\left(\frac{W}{L}\right)_n\left[(V_{DD} - V_{tn})\left(\frac{V_{DD}}{2}\right) - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

this gives

$$t_{PHL} = \frac{\alpha_n C}{k_n'(W/L)_n V_{DD}}$$

CMOS Dynamic Operation

Where α_n is given by

$$\alpha_n = \frac{2}{\left[\dfrac{7}{4} - \dfrac{3V_{tn}}{V_{DD}} + \left(\dfrac{V_{tn}}{V_{DD}} \right)^2 \right]}$$

Likewise, t_{PLH} is given by

$$t_{PLH} = \frac{\alpha_p C}{k'_p \left(W/L \right)_p V_{DD}} \quad \textbf{with} \quad \alpha_p = \frac{2}{\left[\dfrac{7}{4} - \dfrac{3\left| V_{tp} \right|}{V_{DD}} + \left| \dfrac{V_{tp}}{V_{DD}} \right|^2 \right]}$$
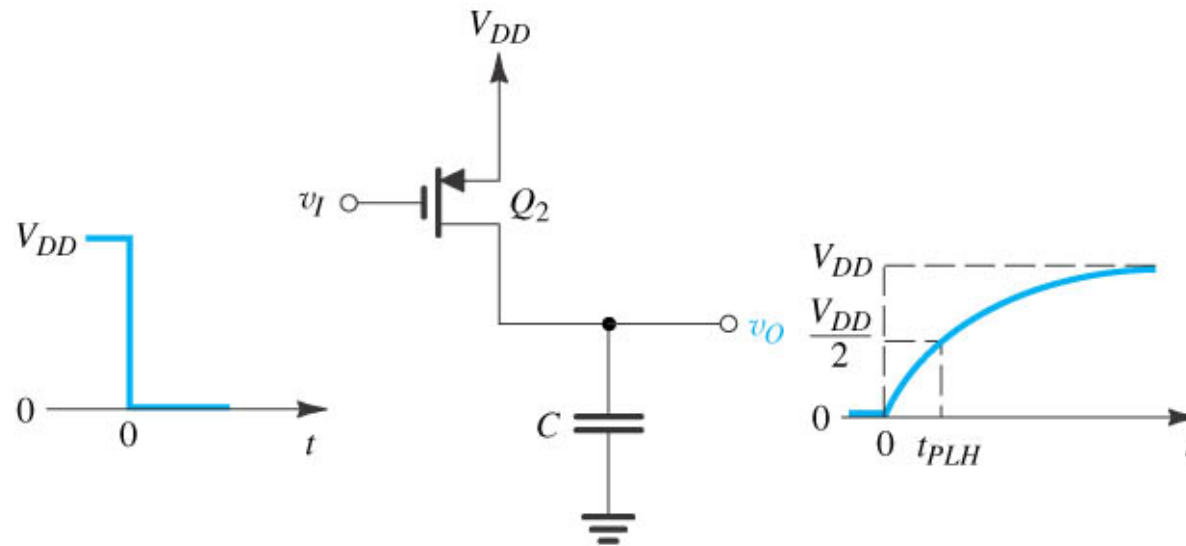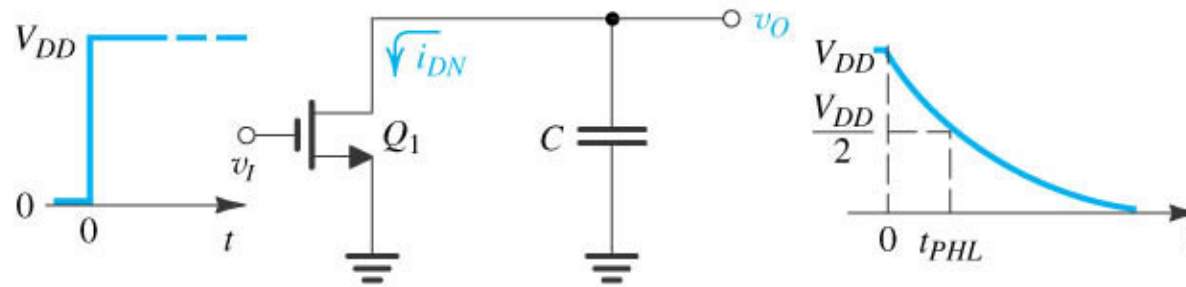
CMOS Dynamic Operation

Propagation delay, t_p is given by

$$t_P = \frac{1}{2}\left(t_{PHL} + t_{PLH}\right)$$

➢ **Components can be equalized by matching transistors**
➢ t_P **is proportional to** C➜ **reduce capacitance**
➢ **Larger** V_{DD} **means lower** t_p
➢ **Conflicting requirements exist**

CMOS – Propagation Delay
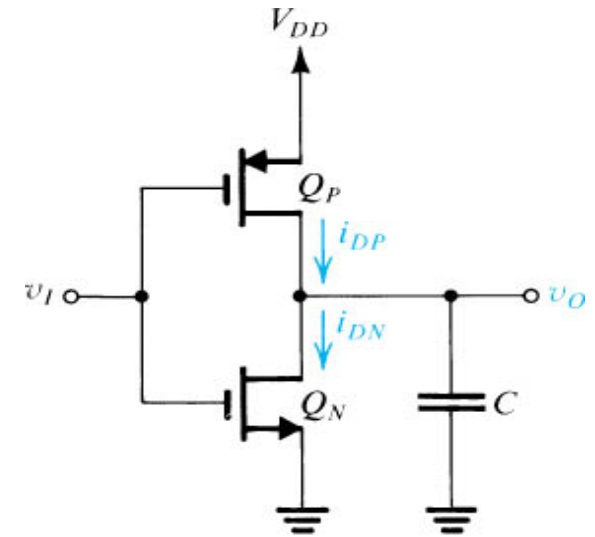
CMOS – Propagation Delay

Capacitance C is the sum of:

- Internal capacitances of Q_N and Q_P
- Interconnect wire capacitance
- Input of the other logic gate

$$t_{PHL} = \frac{1.6C}{k_n^{'}\left(W/L\right)_n V_{DD}}$$

To lower propagation delay

- Minimize C
- Increase process transconductance k'
- Increase W/L
- Increase V_{DD}

Propagation Delay - Example

Find the propagation delay for a minimum-size inverter for which $k_n' = 3k_p' = 180$ μA/V^2 and $(W/L)_n = (W/L)_p = 0.75$ μm/0.5 μm, $V_{DD} = 3.3$ V, $V_{tn} = -V_{tp} = 0.7$ V, and the capacitance is roughly 2fF/mm of device width plus 1 fF/device. What does t_p become if the design is changed to a matched one? Use the method of average current.

Solution

$$\alpha_n = 2 \Bigg/ \left[\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}} \right)^2 \right] = 2 \Bigg/ \left[\frac{7}{4} - \frac{3 \times 0.7}{3.3} + \left(\frac{0.7}{3.3} \right)^2 \right] = 1.73$$

$$t_{PHL} = \frac{\alpha_n C}{k_n' (W/L)_n V_{DD}} = \frac{1.73 \times (2 fF \times 0.75 + 1 fF)}{180 \times 10^{-6} \times \dfrac{0.75}{0.5} \times 3.3}$$

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Propagation Delay - Example

$$t_{PHL} = 4.85 \; ps$$

Since $V_{tn} = \left| V_{tp} \right|$, then $\alpha_n = \alpha_p = 1.73$

We also have $\left(\dfrac{W}{L} \right)_n = \left(\dfrac{W}{L} \right)_p$, hence

$$t_{PLH} = t_{PHL} \times \frac{k_n'}{k_p'} = 4.85 \times 3 = 14.55 \; ps$$

$$t_p = \frac{1}{2}\left(t_{PHL} + t_{PLH} \right) = \frac{1}{2}\left(4.85 + 14.55 \right) = 9.7 \; ps$$

Propagation Delay - Example

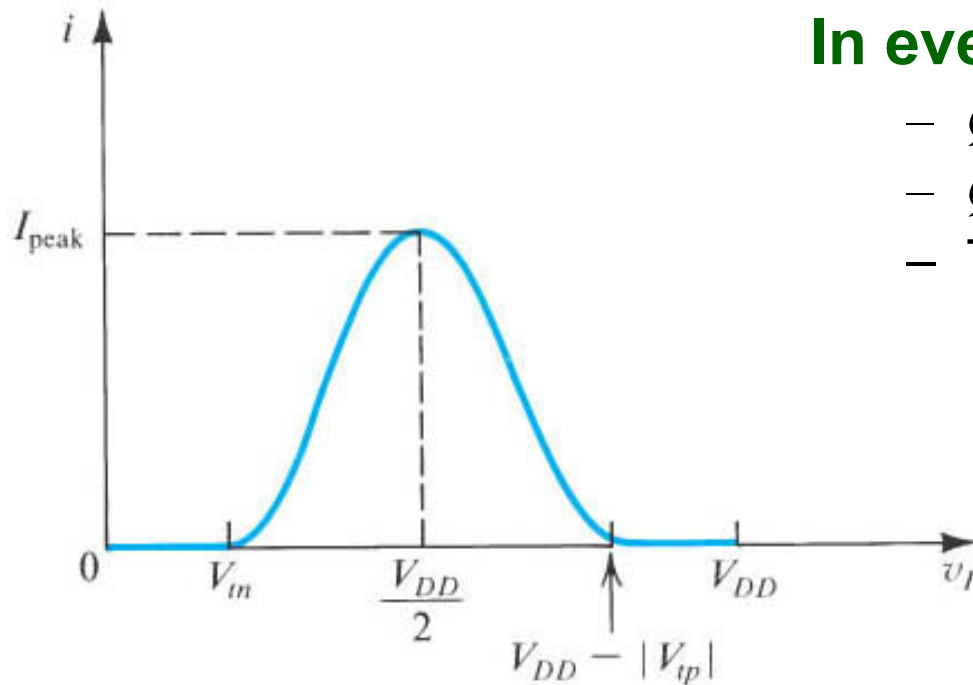**If both devices are matched, then**
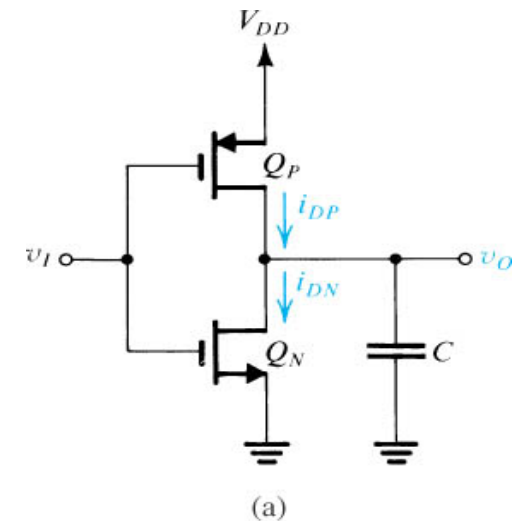
$$k'_p = k'_n$$

$$t_{PLH} = t_{PHL}$$

and

$$t_p = \frac{1}{2}\left(t_{PHL} + t_{PLH}\right) = t_{PHL} = 4.85 \; ps$$
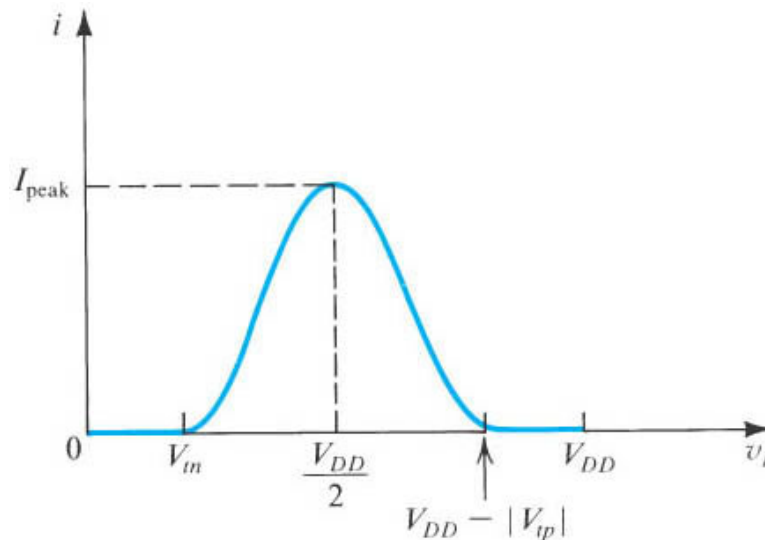
CMOS – Dynamic Power Dissipation

In every cycle

- Q_N dissipate ½ CV_{DD}^2 of energy
- Q_P dissipate ½ CV_{DD}^2 of energy
- Total energy dissipation is CV_{DD}^2

If inverter is switched at f cycles per second, dynamic power dissipation is: $\quad P_D = fCV_{DD}^2$

Power Dissipation - Example

In this problem, we estimate the inverter power dissipation resulting from the current pulse that flows in Q_N and Q_P when the input pulse has finite rise and fall times. Let $V_{tn}=-V_{tp}=0.5$ V, $V_{DD} = 1.8$V, and $k_n=k_p=450\mu$A/V^2. Let the input rising and falling edges be linear ramps with the 0-to-V_{DD} and V_{DD}-to-0 transitions taking 1 ns each. Find I_{peak}.

13.44

Power Dissipation - Example
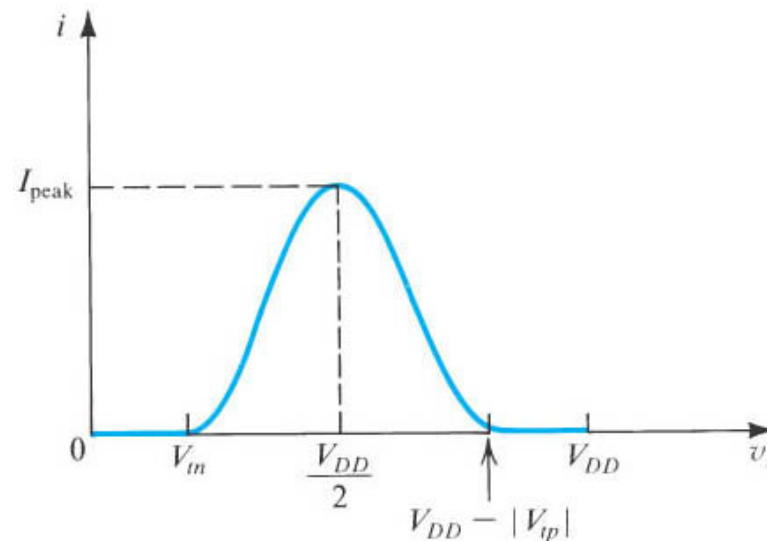
To determine the energy drawn from the supply per transition, assume that the current pulse can be approximated by a triangle with a base corresponding to the time for the rising or falling edge to go from V_t to $V_{DD}-V_t$, and the height equal to I_{peak}. Also, determine the power dissipation that results when the inverter is switched at 100 MHz.

Power Dissipation - Example
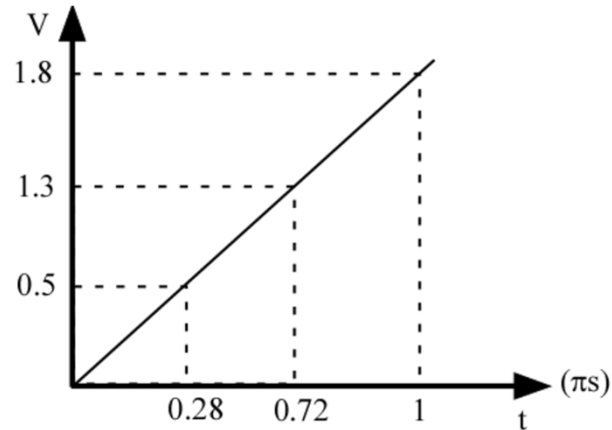
$$I_{Peak} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left(\frac{V_{DD}}{2} - V_{tn}\right)^2$$

$$I_{Peak} = \frac{1}{2} 450 \frac{\mu A}{V^2} \left(\frac{1.8}{2} - 0.5\right)^2 = 36\mu A$$

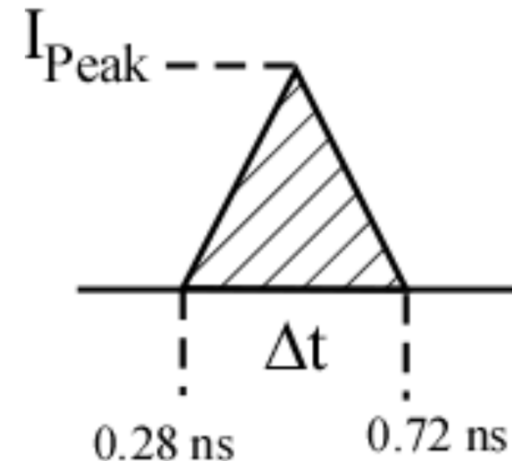# Power Dissipation - Example

The time when the input reaches V_t is:

$$\frac{0.5}{1.8} \times 1 \text{ ns} = 0.28 \text{ ns}$$

The time when the input reaches V_{DD} - V_t is:

$$\frac{1.8 - 0.5}{1.8} \times 1 \text{ ns} = 0.72 \text{ ns}$$

The base of the triangle is

$$\Delta t = 0.72 - 0.28 = 0.44 \text{ ns wide}$$

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Power Dissipation - Example

$$E = \frac{1}{2} I_{Peak} \times V_{DD} \times \Delta t = \frac{1}{2} \times 36 \mu A \times 1.8 \times 0.44 \text{ ns}$$

$$E = 14.3 \ fJ$$

$$P = f \times E = 100 \times 10^{6} \times 14.3 \times 10^{-15} = 1.43 \ \mu W$$