ECE 342
Electronic Circuits

Lecture 35
CMOS Delay Model

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\( V_{IH} \): Input voltage at high state \( \Rightarrow V_{IH\text{min}} \)
\( V_{IL} \): Input voltage at low state \( \Rightarrow V_{IL\text{max}} \)
\( V_{OH} \): Output voltage at high state \( \Rightarrow V_{OH\text{min}} \)
\( V_{OL} \): Output voltage at low state \( \Rightarrow V_{OL\text{min}} \)

Likewise for current we can define

**Currents into input**

\[ I_{IH} \leftrightarrow I_{IH\text{max}} \]
\[ I_{IL} \leftrightarrow I_{IL\text{max}} \]

**Currents into output**

\[ I_{OH} \leftrightarrow I_{OH\text{max}} \]
\[ I_{OL} \leftrightarrow I_{OL\text{max}} \]
Voltage Transfer Characteristics (VTC)

The static operation of a logic circuit is determined by its VTC

- In low state: noise margin is $NM_L$
  
  \[ NM_L = V_{IL} - V_{OL} \]

- In high state: noise margin is $NM_H$
  
  \[ NM_H = V_{OH} - V_{IH} \]

- An ideal VTC will maximize noise margins

\[ \text{Optimum: } NM_L = NM_H = \frac{V_{DD}}{2} \]

$V_{IL}$ and $V_{IH}$ are the points where the slope of the VTC = -1
Switching Time & Propagation Delay

Diagram showing the switching time and propagation delay with input and output signals.

- **Input**
  - $v_I$
  - $v_{IH}$
  - $(v_{IL} + v_{IH})/2$
  - $v_{IL}$
  - 10%
  - 90%
  - $t_r$
  - $t_pHL$

- **Output**
  - $v_o$
  - $v_{oH}$
  - $(v_{oL} + v_{oH})/2$
  - $v_{oL}$
  - 10%
  - 90%
  - $t_{THL}$
  - $t_pLH$
  - $t_{TLH}$
Switching Time & Propagation Delay

\[ t_r = \text{rise time (from 10\% to 90\%)} \]
\[ t_f = \text{fall time (from 90\% to 10\%)} \]
\[ t_{pLH} = \text{low-to-high propagation delay} \]
\[ t_{pHL} = \text{high-to-low propagation delay} \]

Inverter propagation delay:

\[ t_p = \frac{1}{2} \left( t_{pLH} + t_{pHL} \right) \]
CMOS Dynamic Operation

- Exact analysis is too tedious
- Replace all the capacitances in the circuit by a single equivalent capacitance $C$ connected between the output node of the inverter and ground
- Analyze capacitively loaded inverter to determine propagation delay
CMOS – Dynamic Operation

\[ C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w \]
CMOS – Dynamic Operation

(a) CMOS circuit diagram

(b) Voltage waveforms

(c) Voltage transfer characteristic

(d) Capacitor discharge through \( Q_N \)

Operating point at \( t = 0+ \)

Operating point at \( t = 0- \)

Operating point after switching is completed

\( v_{GSN} = V_{DD} \)
CMOS Dynamic Operation

Need interval $t_{PHL}$ during which $v_o$ reduces from $V_{DD}$ to $V_{DD}/2$

$$I_{av} t_{PHL} = C \left[ V_{DD} - \left( \frac{V_{DD}}{2} \right) \right]$$

Which gives

$$t_{PHL} = \frac{C V_{DD}}{2 I_{av}}$$

$I_{av}$ is given by

$$I_{av} = \frac{1}{2} \left[ i_{DN}(E) + i_{DN}(M) \right]$$
CMOS Dynamic Operation

where

\[ i_{DN}(E) = \frac{1}{2} k'_n \left( \frac{W}{L} \right)_n (V_{DD} - V_{tn})^2 \]

and

\[ i_{DN}(M) = k'_n \left( \frac{W}{L} \right)_n \left[ (V_{DD} - V_{tn}) \left( \frac{V_{DD}}{2} \right) - \frac{1}{2} \left( \frac{V_{DD}}{2} \right)^2 \right] \]

this gives

\[ t_{PHL} = \frac{\alpha_n C}{k'_n \left( \frac{W}{L} \right)_n V_{DD}} \]
CMOS Dynamic Operation

Where $a$ is given by

$$\alpha_n = \frac{2}{\left[ \frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left( \frac{V_{tn}}{V_{DD}} \right)^2 \right]}$$

Likewise, $t_{PLH}$ is given by

$$t_{PLH} = \frac{\alpha_p C}{k_p \left( \frac{W}{L} \right)_p V_{DD}}$$

with

$$\alpha_p = \frac{2}{\left[ \frac{7}{4} - \frac{3|V_{tp}|}{V_{DD}} + \left| \frac{V_{tp}}{V_{DD}} \right|^2 \right]}$$
CMOS Dynamic Operation

Where \( a \) is given by

\[
t_p = \frac{1}{2} (t_{PHL} + t_{PLH})
\]

- Components can be equalized by matching transistors
- \( t_p \) is proportional to \( C \) \( \Rightarrow \) reduce capacitance
- Larger \( V_{DD} \) means lower \( t_p \)
- Conflicting requirements exist
CMOS – Propagation Delay

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ 0 \]

\[ 0 \]

\[ t \]

\[ t \]

\[ t_{PHL} \]

\[ t_{PLH} \]
CMOS – Propagation Delay

Capacitance C is the sum of:
- Internal capacitances of $Q_N$ and $Q_P$
- Interconnect wire capacitance
- Input of the other logic gate

$$t_{PHL} = \frac{1.6C}{k_n'(W/L)_n V_{DD}}$$

To lower propagation delay
- Minimize $C$
- Increase process transconductance $k'$
- Increase $W/L$
- Increase $V_{DD}$
Propagation Delay - Example

Find the propagation delay for a minimum-size inverter for which \( k_n' = 3k_p' = 180 \) \( \mu A/V^2 \) and \( (W/L)_n = (W/L)_p = 0.75 \) \( \mu m/0.5 \) \( \mu m \), \( V_{DD} = 3.3 \) V, \( V_{tn} = -V_{tp} = 0.7 \) V, and the capacitance is roughly \( 2fF/mm \) of device width plus \( 1fF/device \). What does \( t_p \) become if the design is changed to a matched one? Use the method of average current.

Solution

\[
\alpha_n = 2 \sqrt{\left[ \frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left( \frac{V_{tn}}{V_{DD}} \right)^2 \right] = 2 \sqrt{\left[ \frac{7}{4} - \frac{3 \times 0.7}{3.3} + \left( \frac{0.7}{3.3} \right)^2 \right] = 1.73}
\]

\[
t_{PHL} = \frac{\alpha_n C}{k_n' (W/L)_n V_{DD}} = \frac{1.73 \times (2fF \times 0.75 + 1fF)}{180 \times 10^{-6} \times \frac{0.75}{0.5} \times 3.3} = \text{13.38}
\]
Propagation Delay - Example

\[ t_{PHL} = 4.85 \, \text{ps} \]

Since \( V_{tn} = |V_{tp}| \), then \( \alpha_n = \alpha_p = 1.73 \)

We also have \( \left( \frac{W}{L} \right)_n = \left( \frac{W}{L} \right)_p \), hence

\[ t_{PLH} = t_{PHL} \times \frac{k'_n}{k_n} = 4.85 \times 3 = 14.55 \, \text{ps} \]

\[ t_{PLH} = \frac{1}{2} \left( t_{PHL} + t_{PLH} \right) = \frac{1}{2} \left( 4.85 + 14.55 \right) = 9.7 \, \text{ps} \]
Propagation Delay - Example

If both devices are matched, then

\[ k_p' = k_n' \]

\[ t_{PLH} = t_{PHL} \]

and

\[ t_p = \frac{1}{2} (t_{PHL} + t_{PLH}) = t_{PHL} = 4.85 \text{ ps} \]
CMOS – Dynamic Power Dissipation

In every cycle

- \( Q_N \) dissipate \( \frac{1}{2} CV_{DD}^2 \) of energy
- \( Q_P \) dissipate \( \frac{1}{2} CV_{DD}^2 \) of energy
- Total energy dissipation is \( CV_{DD}^2 \)

If inverter is switched at \( f \) cycles per second, dynamic power dissipation is: \( P_D = fCV_{DD}^2 \)
In this problem, we estimate the inverter power dissipation resulting from the current pulse that flows in $Q_N$ and $Q_P$ when the input pulse has finite rise and fall times. Let $V_{tn} = -V_{tp} = 0.5 \ V$, $V_{DD} = 1.8\ V$, and $k_n = k_p = 450\ \mu A/V^2$. Let the input rising and falling edges be linear ramps with the 0-to-$V_{DD}$ and $V_{DD}$-to-0 transitions taking 1 ns each. Find $I_{peak}$. 

13.44
To determine the energy drawn from the supply per transition, assume that the current pulse can be approximated by a triangle with a base corresponding to the time for the rising or falling edge to go from $V_t$ to $V_{DD} - V_t$, and the height equal to $I_{peak}$. Also, determine the power dissipation that results when the inverter is switched at 100 MHz.
Power Dissipation - Example

\[ I_{\text{Peak}} = \frac{1}{2} \mu_n C_{\text{ox}} \left( \frac{W}{L} \right)_n \left( \frac{V_{DD}}{2} - V_{tn} \right)^2 \]

\[ I_{\text{Peak}} = \frac{1}{2} \times 450 \mu A \left( \frac{1.8}{2} - 0.5 \right)^2 = 36 \mu A \]
Power Dissipation - Example

The time when the input reaches $V_t$ is:

$$\frac{0.5}{1.8} \times 1\,\text{ns} = 0.28\,\text{ns}$$

The time when the input reaches $V_{DD} - V_t$ is:

$$\frac{1.8 - 0.5}{1.8} \times 1\,\text{ns} = 0.72\,\text{ns}$$

The base of the triangle is

$$\Delta t = 0.72 - 0.28 = 0.44\,\text{ns}$$
Power Dissipation - Example

\[ E = \frac{1}{2} I_{\text{peak}} \times V_{DD} \times \Delta t = \frac{1}{2} \times 36\mu A \times 1.8 \times 1.44 \text{ ns} \]

\[ E = 14.3 \text{ fJ} \]

\[ P = f \times E = 100 \times 10^6 \times 14.3 \times 10^{-15} = 1.43 \mu W \]