ECE 342
Electronic Circuits

Lecture 35
CMOS Logic

Jose E. Schutt-Aine
Electrical & Computer Engineering
University of Illinois
jesa@Illinois.edu

Digital Logic - Generalization

De Morgan's Law

$$\overline{A + B + C + \ldots} = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \ldots$$

$$\overline{A \cdot B \cdot C \cdot \ldots} = \bar{A} + \bar{B} + \bar{C} + \ldots$$

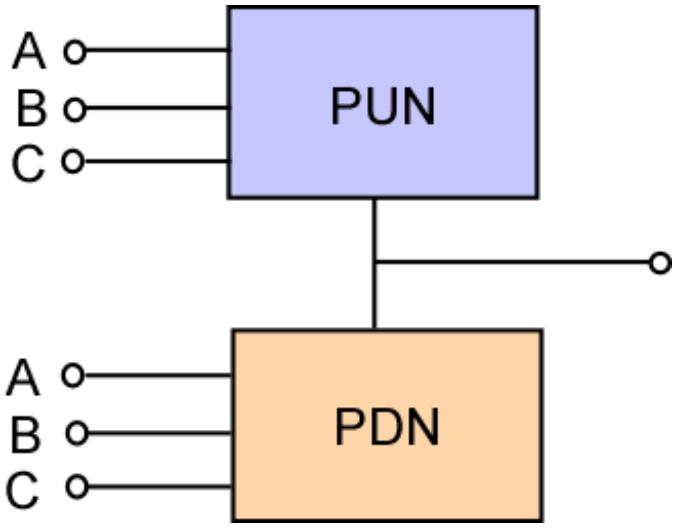
Distributive Law

$$AB + AC + BC + BD = A(B + C) + B(C + D)$$

- **General Procedure**
  1. Design PDN to satisfy logic function
  2. Construct PUN to be complementary of PDN in every way
  3. Optimize using distributive rule

CMOS Logic Gate Circuits

- **Two Networks**
  - Pull-down network (PDN) with NMOS
  - Pull-up network (PUN) with PMOS

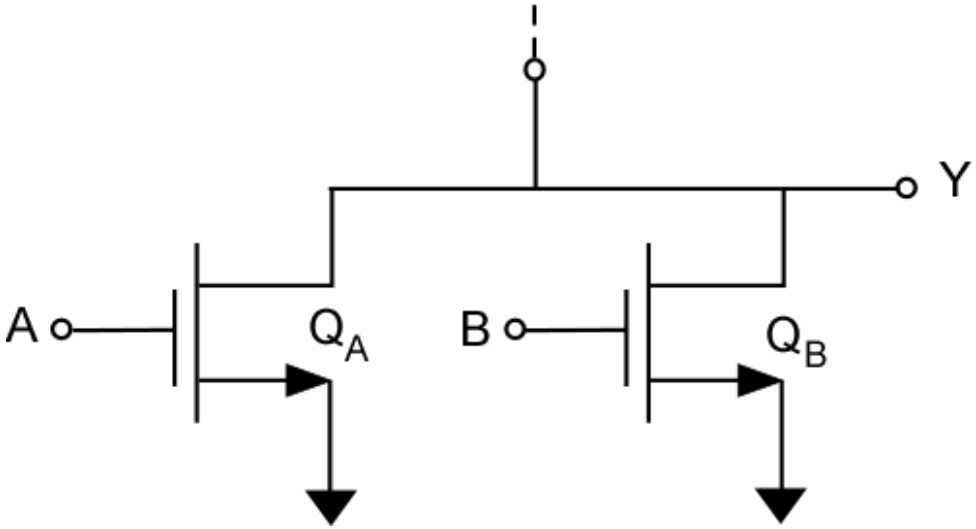


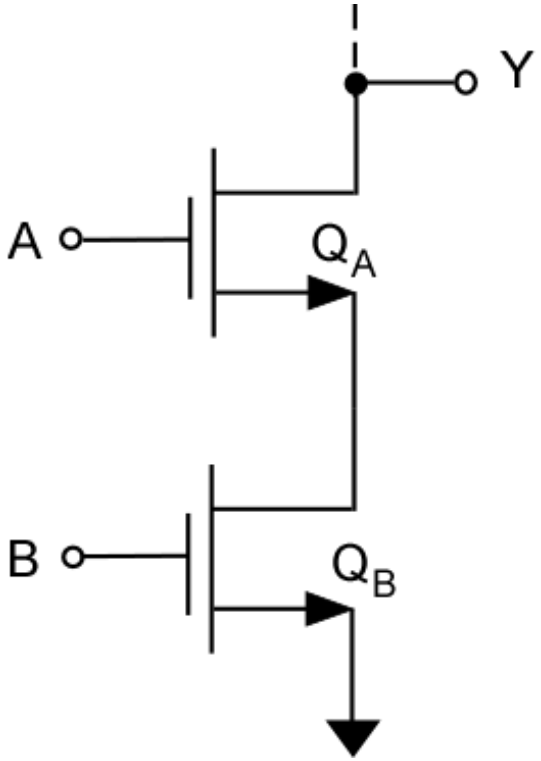
PUN conducts when inputs are low and consists of PMOS transistors

PDN consists of NMOS transistors and is active when inputs are high

- **PDN and PUN utilize devices**
  - In parallel to form OR functions
  - In series to form AND functions

Pull-Down Networks

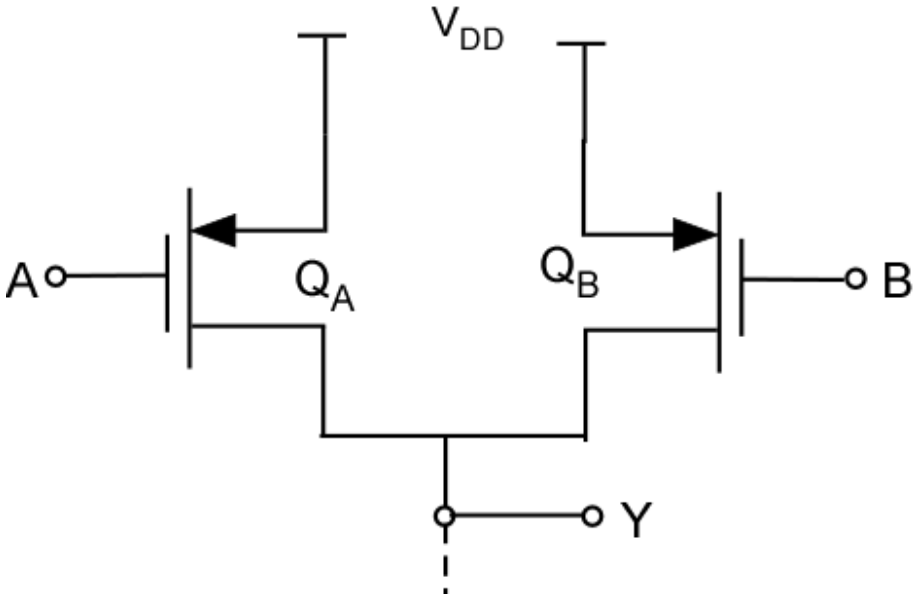




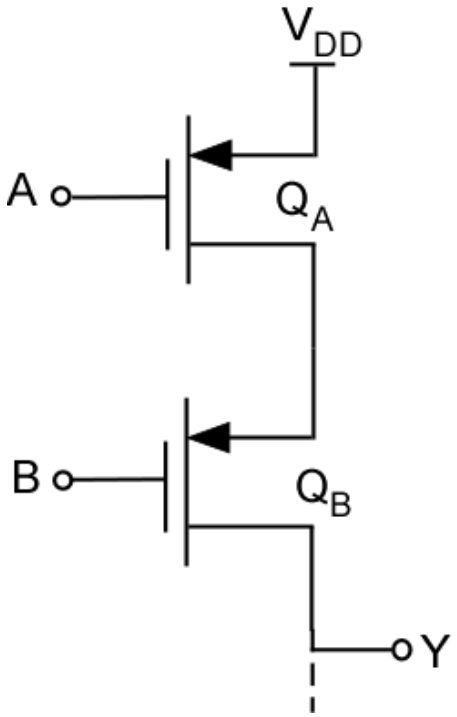
$$\overline{Y} = A + B$$

$$\overline{Y} = AB$$

Pull-Up Networks

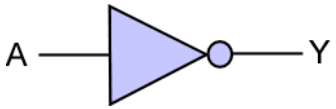
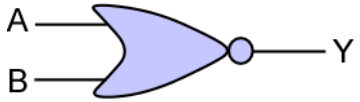
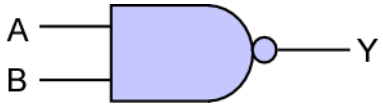
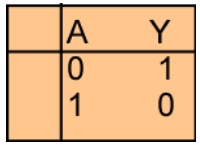
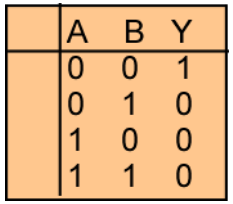
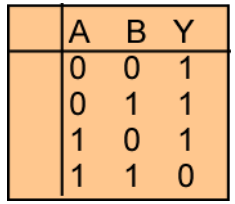


$$Y = \overline{A} + \overline{B}$$



$$Y = \overline{A}\,\overline{B}$$

Basic Logic Function

Basic Function	INVERTER	NOR	NAND
Symbol			
# Devices PUN	1 PMOS	2 PMOS-Series	2 PMOS-Parallel
# Devices PDN	1 NMOS	2 NMOS-Parallel	2 NMOS-Series
Truth Table			

A	Y
0	1
1	0

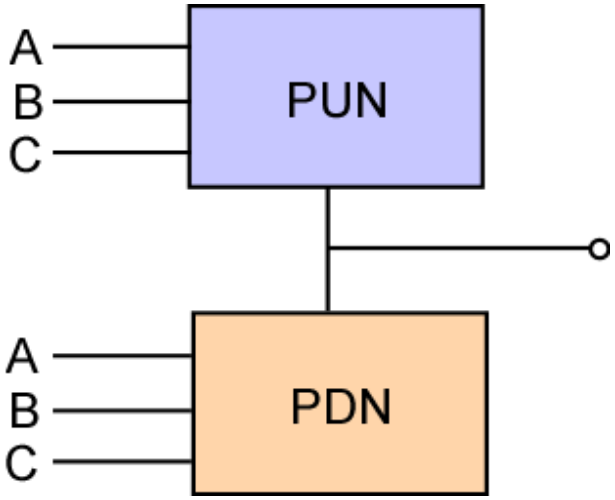
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Pull-Down and Pull-Up Functions

Pull-up network (PUN)

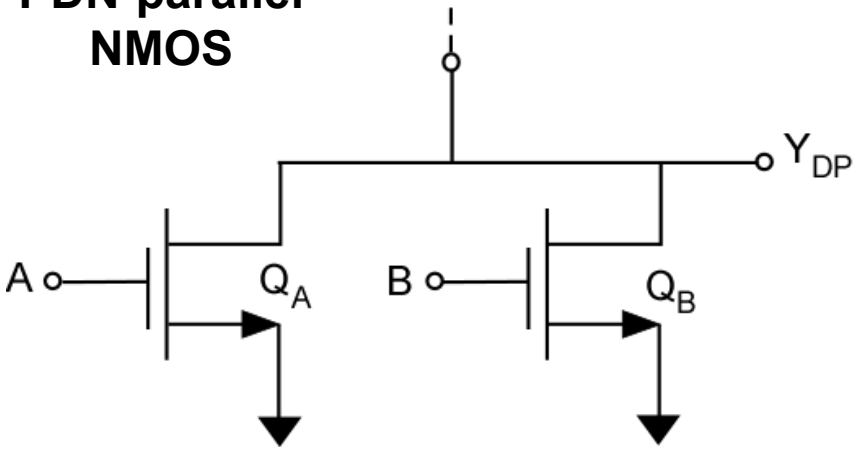
Pull-down network (PDN)



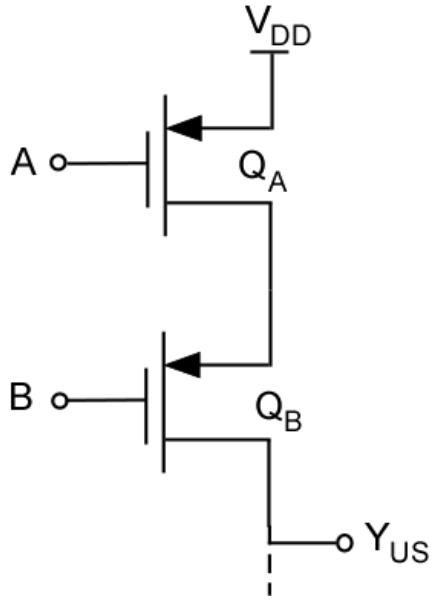
- **Key features**
  - When PDN switch is on, PUN switch is off and vice versa
  - Conditions for being on and off are complementary

Pull-Down and Pull-Up

PDN-parallel NMOS



PUN-series PMOS



Truth Tables

$$Y_{DP} = \overline{A + B}$$

A	B	Y_{DP}
0	0	1
0	1	0
1	0	0
1	1	0

$$Y_{US} = \overline{A}\,\overline{B}$$

A	B	Y_{US}
0	0	1
0	1	0
1	0	0
1	1	0

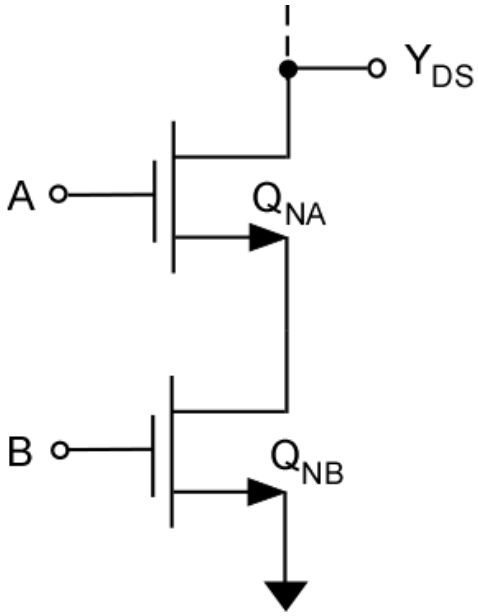
Pull-Down and Pull-Up

When Y_{DP} in PDN-parallel is low, this means that either A or B (or both) is high. When either A or B (or both) is high, either transistor (or both) in PUN-series are off➔Y_{US}=low

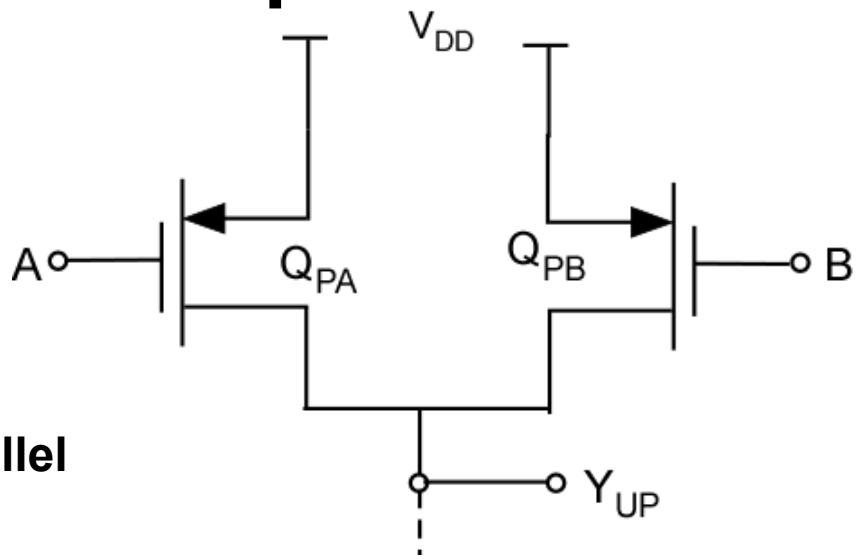
When Y_{DP} in PDN-parallel is high, both A and B are low. Both transistors in PUN-Series are on creating a path to VDD. Y_{US}=high➔Y_{US}=Y_{DP}.

PDN-Parallel and PUN-series are complementary

Pull-Down and Pull-Up



PDN-Series
NMOS



PUN-Parallel
PMOS

Truth Tables

$$Y_{DS} = A\overline{B}$$

A	B	Y_{DS}
0	0	1
0	1	1
1	0	1
1	1	0

$$Y_{UP} = \overline{A} + \overline{B}$$

A	B	Y_{UP}
0	0	1
0	1	1
1	0	1
1	1	0

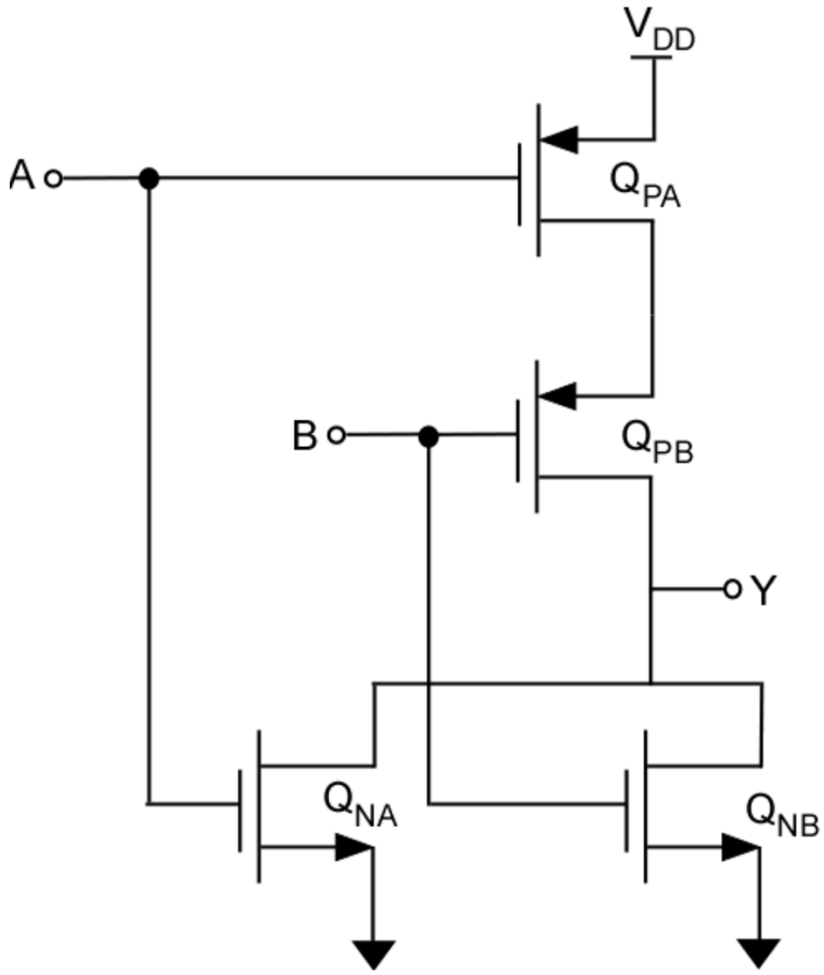
Pull-Down and Pull-Up

If Y_{DS} is low, both A and B must be high in which case both transistors in PUN-Parallel are off providing no path to V_{DD} → Y_{UP}=low → Y_{UP}=Y_{DS}.

If Y_{DS} is high, then either A or B (or both) are off (low) in which case either Q_{PA} or Q_{PB} in PUN-Parallel will be on and present a path to V_{DD}; thus Y_{UP}=high → Y_{UP}=Y_{DS}

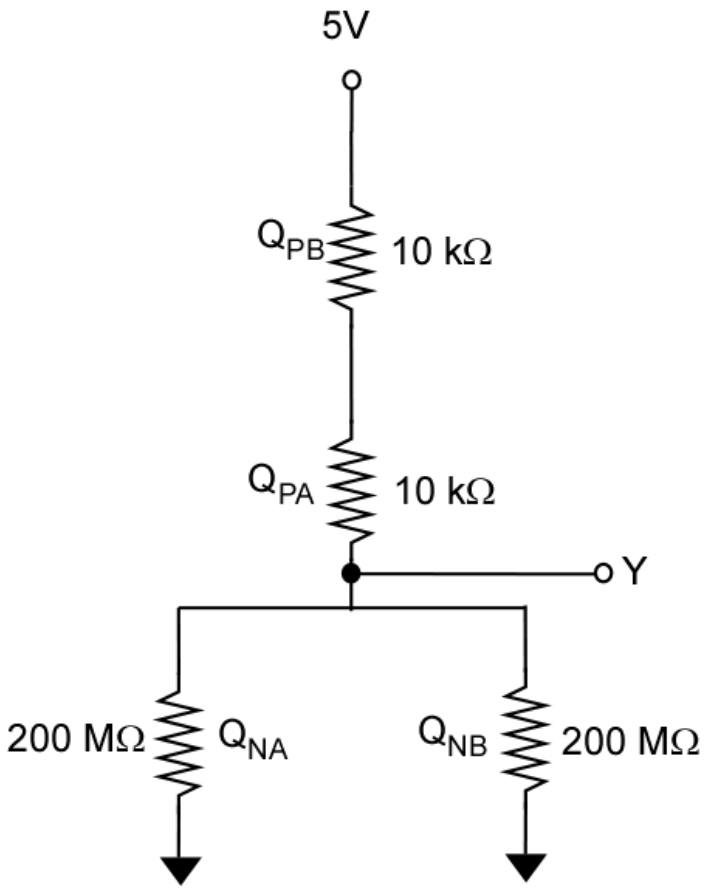
PDN-Series and PUN-Parallel are complementary

Two-Input NOR Gate

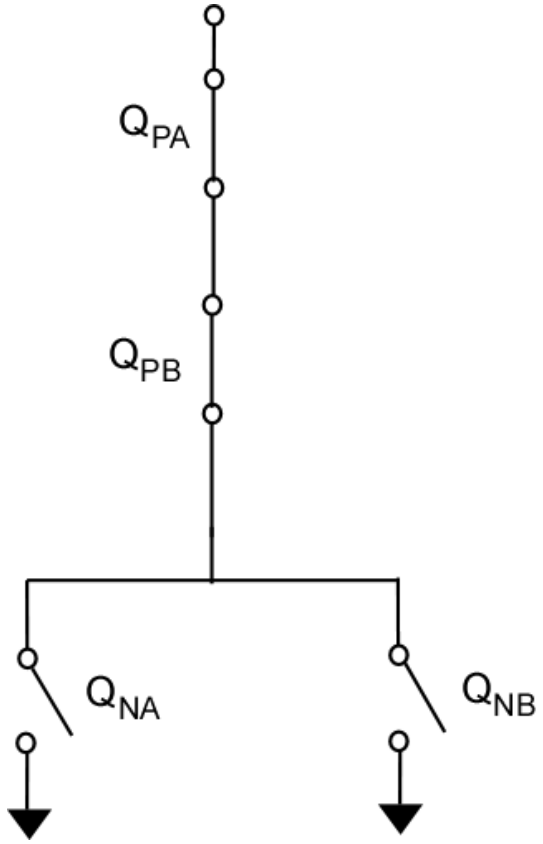


$$Y = \overline{A + B} = \bar{A}\bar{B}$$

Two-Input NOR Gate

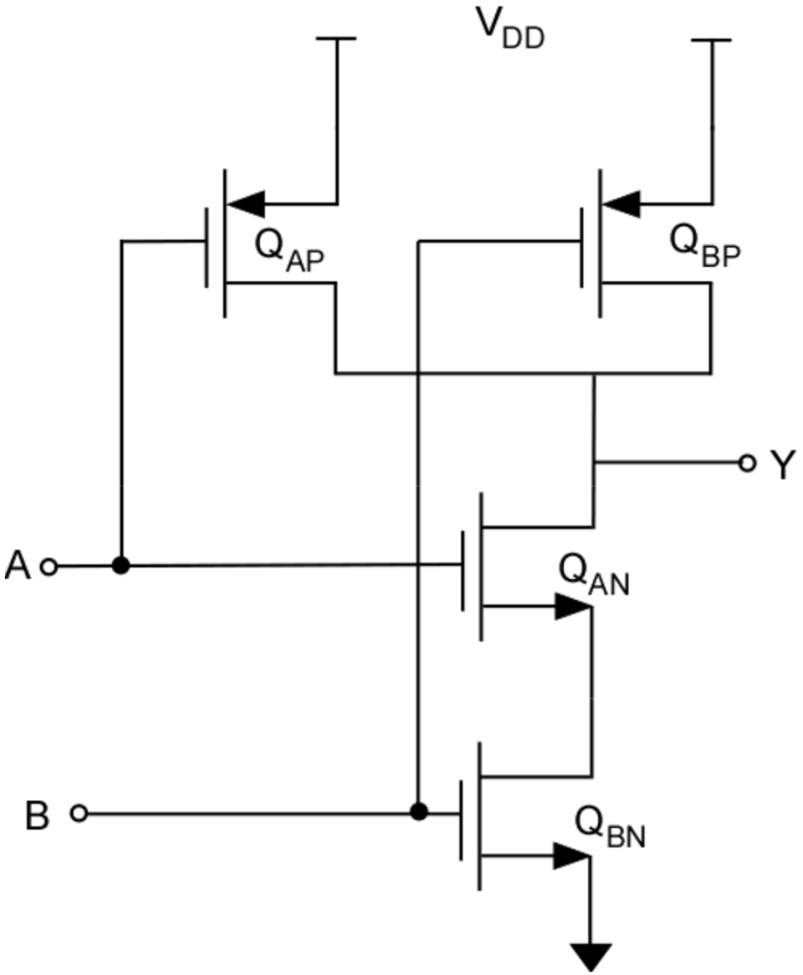


Actual



Ideal

Two-Input NAND Gate



$$Y = \overline{AB} = \overline{A} + \overline{B}$$

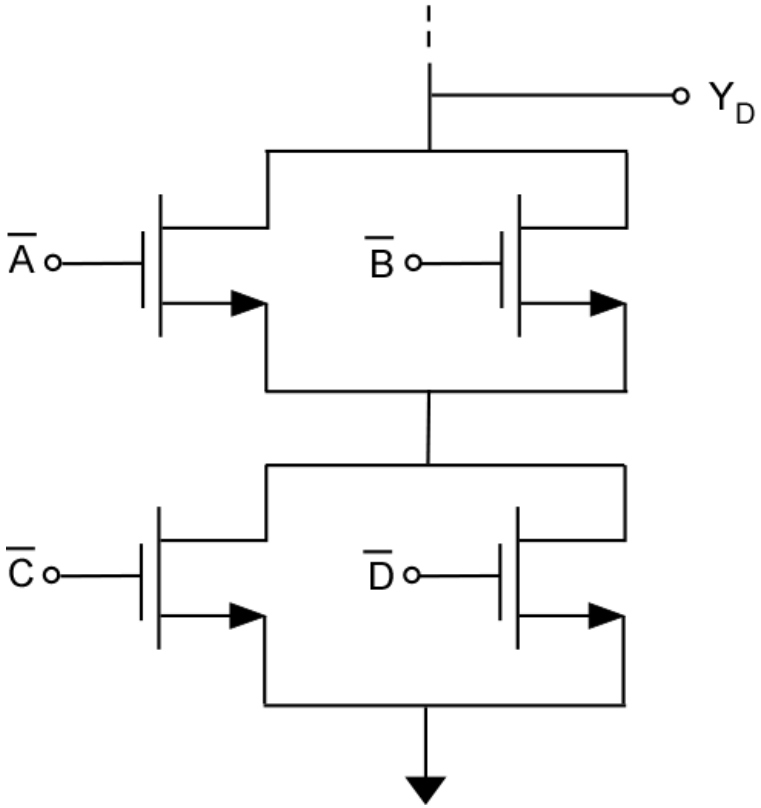
Example

$$Y = \overline{A\overline{B} \cdot \overline{C\overline{D}}}$$

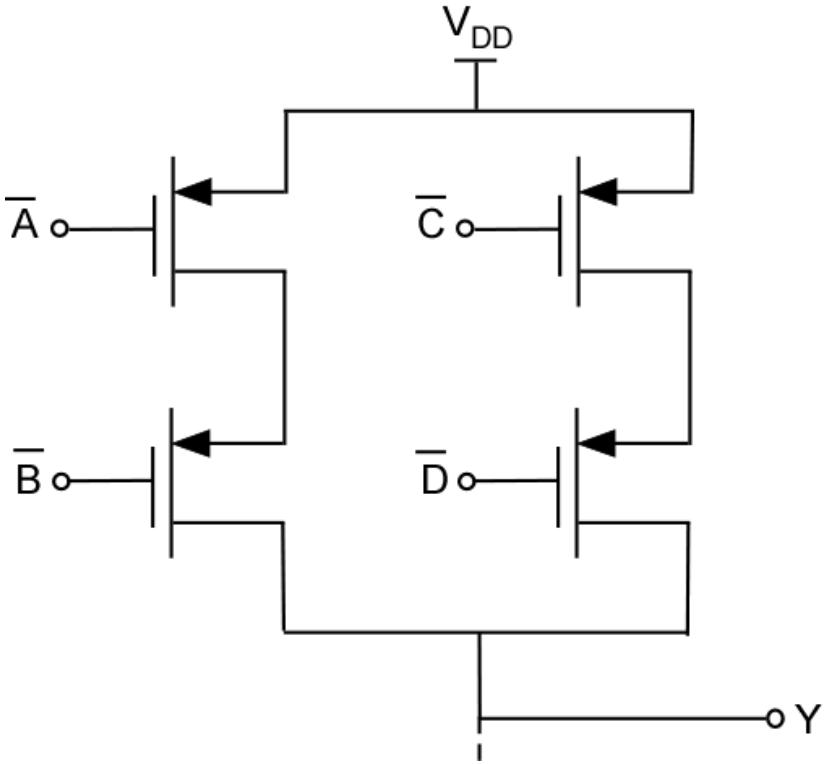
Using De Morgan's Law

$$Y = \overline{A\overline{B} \cdot \overline{C\overline{D}}} = AB + CD = \overline{(\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})}$$

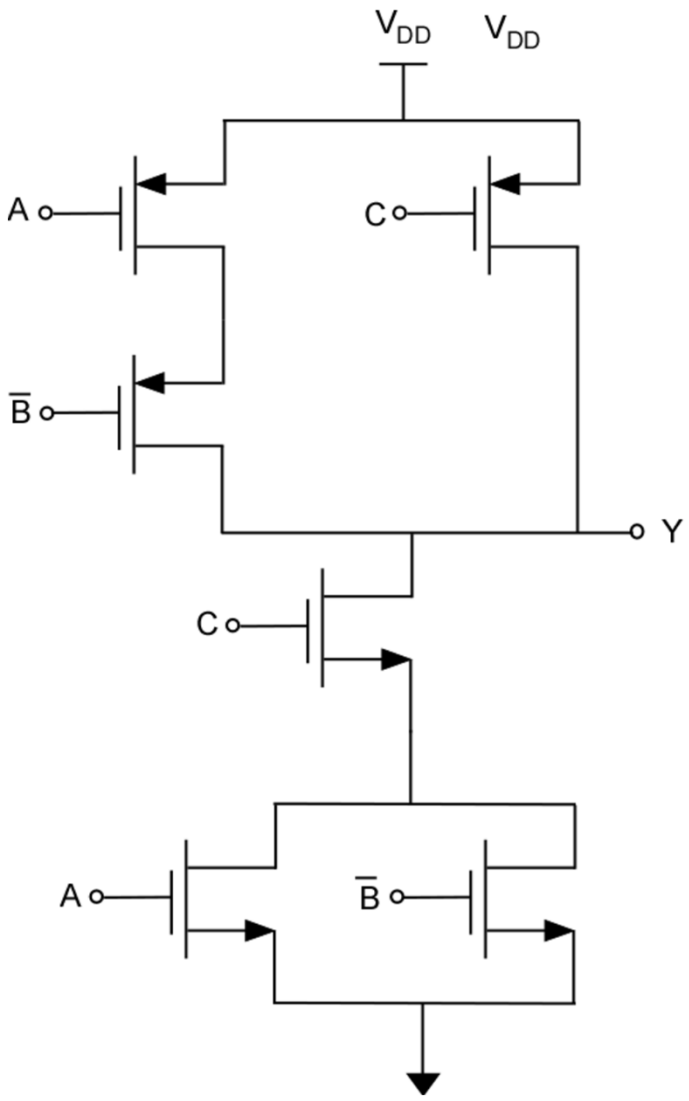
Pull-down network



Pull-up network



Example 1



Evaluate Logic Function

$$Y = \overline{(A + \overline{B})C}$$ from pull down

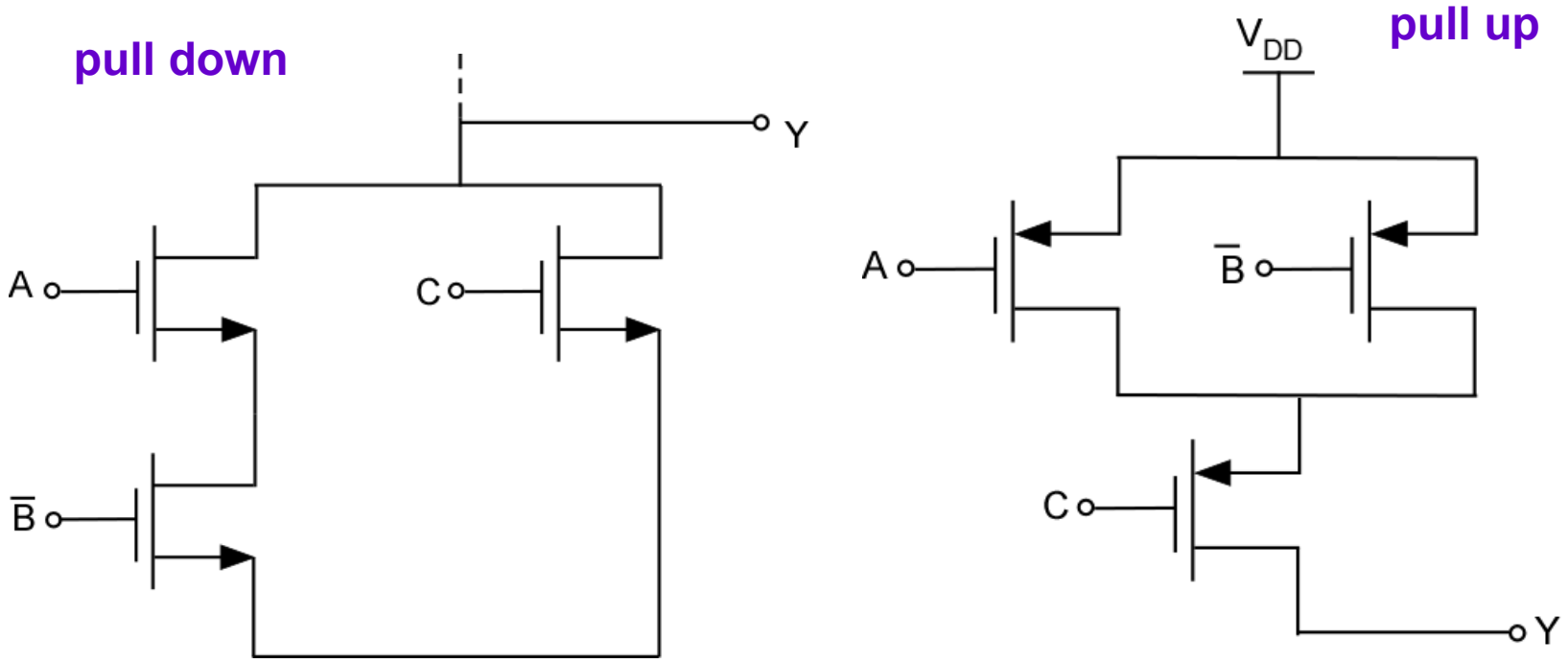
$$Y = \overline{A}B + \overline{C}$$ from pull up

$$\overline{A}B + \overline{C} = \overline{\overline{\overline{A}B} \cdot C} = \overline{(A + \overline{B})C}$$

Example 2

Implement the function

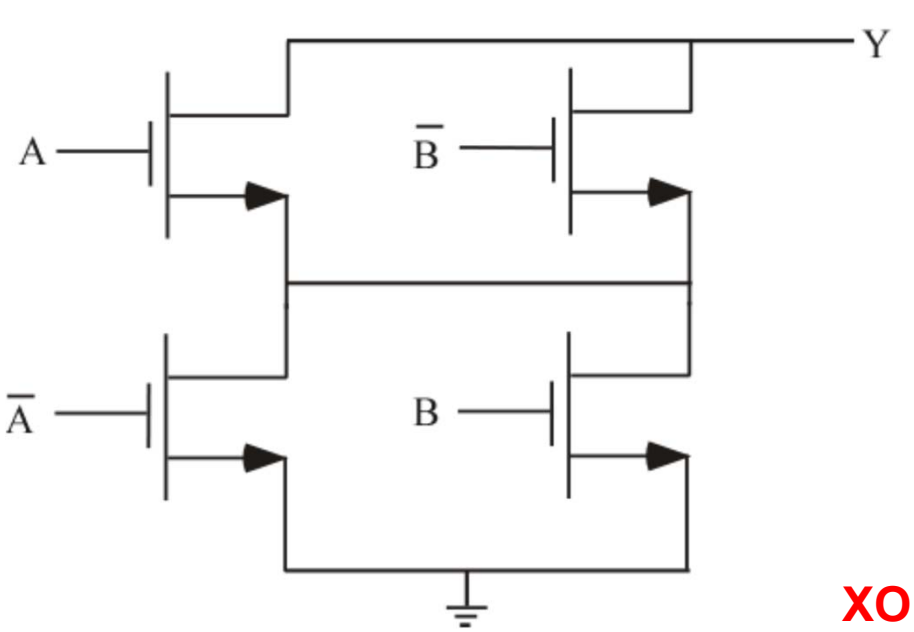
$$\overline{Y} = A\overline{B} + C$$

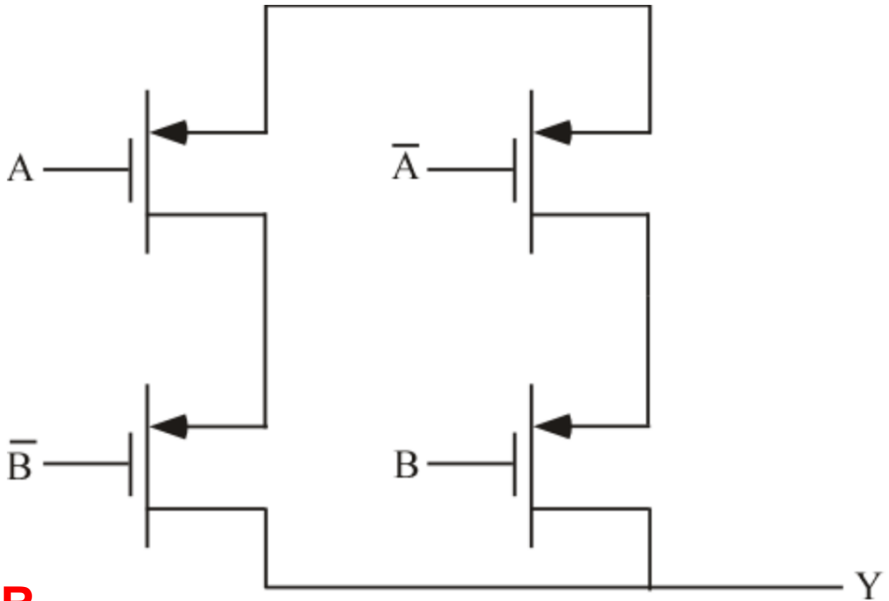


$$Y = \overline{A\overline{B} + C} = \overline{A\overline{B}} \cdot \overline{C} = (\overline{A} + B) \cdot \overline{C}$$

Exclusive-OR (XOR) Function

$$Y = A\overline{B} + \overline{A}B \qquad \overline{Y} = (\overline{A} + B)(A + \overline{B})$$





pull down

pull up

XOR

	A	B	Y
	0	0	0
	0	1	1
	1	0	1
	1	1	0

Transistor Sizing

Objectives

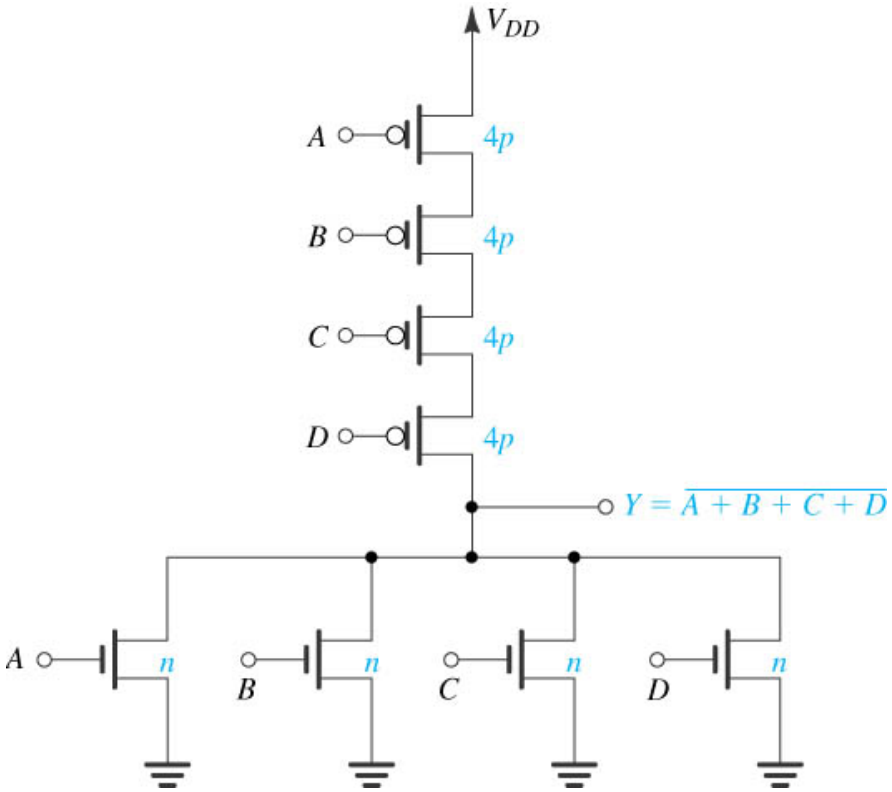
- PDN provides discharge current of at least that of an NMOS
- PUN provides charging current of at least that of a PMOS
- Worst case gate delay equal to that of basic inverter
- Find combination that results in lowest output current
- For transistors in parallel aspect ratios add
- For transistors in series, inverses of aspect ratios add

$$Series: \frac{1}{(W/L)_{eq}} = \frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \ldots + \frac{1}{(W/L)_M}$$

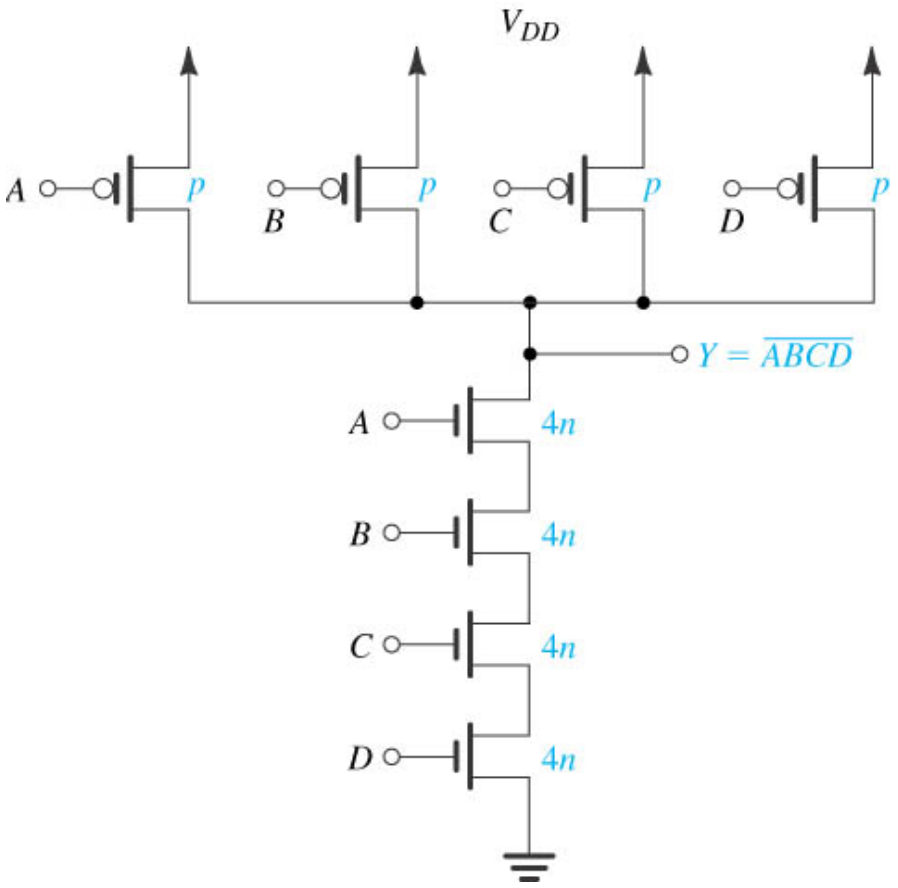
$$Parallel: (W/L)_{eq} = (W/L)_1 + (W/L)_2 + \ldots + (W/L)_M$$

$$p = (W/L)_p \qquad n = (W/L)_n$$

Transistor Sizing



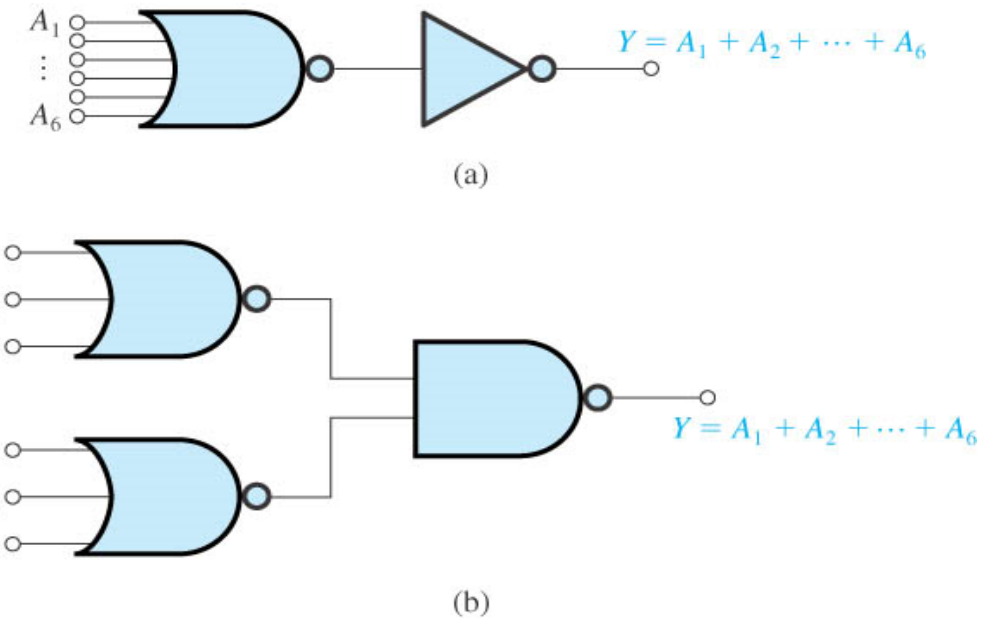
NOR



NAND

Transistor Sizing – Example 1

Two approaches to realizing the OR function of six input variables. Assuming that the transistors in both circuits are properly sized to provide each gate with a current-driving capability equal to that of the basic matched inverter, find the number of transistors and the total area of each circuit. Assume the basic inverter to have a $(W/L)_n$ ratio of 1.2 μm/0.8 μm and a $(W/L)_p$ ratio of 3.6 μm/0.8 μm.



Transistor Sizing – Example 1

For design (a), there are 2(6)+2=14 transistors:
All 7 NMOS use $(W/L)_n = n$
1 PMOS uses $(W/L)_p = p$
6 PMOS use $(W/L)_p = 6p$
Total Area = 7(1.2)0.8+ 1(3.6)0.8 + 6(6)(3.6)0.8 = 113.3 μm^2

For design (b), there are 2(3)2 + 1(2)2=16 transistors:
6 NMOS use $(W/L)_n = n$
6 PMOS use $(W/L)_p = 3p$
2 PMOS use $(W/L)_p = p$
2 NMOS use $(W/L)_n = 2n$
Total Area = 70(1.2)0.8 = 67.2 μm^2, or 59% of (a)