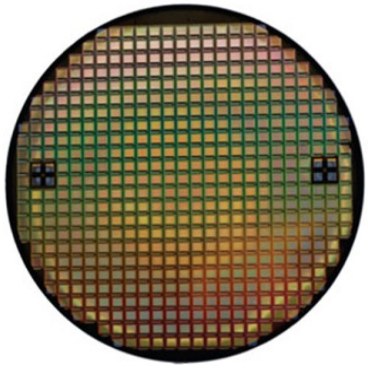
ECE 451

Automated Microwave Measurements Laboratory

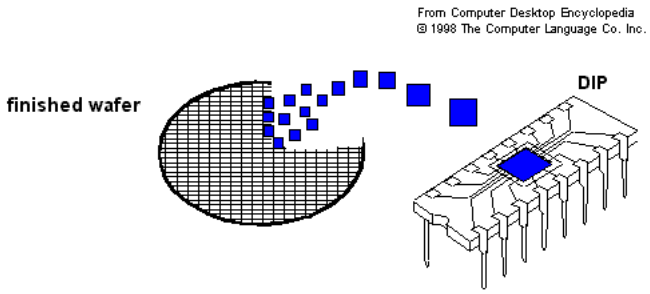
Experiment 07 - On-wafer measurement - Signal integrity with eye diagram

1 Introduction

ICs are fabricated in the *clean room* using dedicated processes on the *wafer*. Figure 1a shows a typical wafer. The wafer carrying the circuitry is then diced into many dies, each die is, in fact, the actual circuit that powers computers, smart phones and many other electronics devices. The die is then packaged in a "shell", this is called packaging. The concept is illustrated in Figure 1b. The IC's ports are extended to the pins of the "cover" such that the package can be wired on a PCB. Such extensions can be done using *wire bond*. Figure 2 shows an IC packaged using wire bond.



(a) Diced wafer



(b) From wafer to package

Figure 1: IC packaging concept

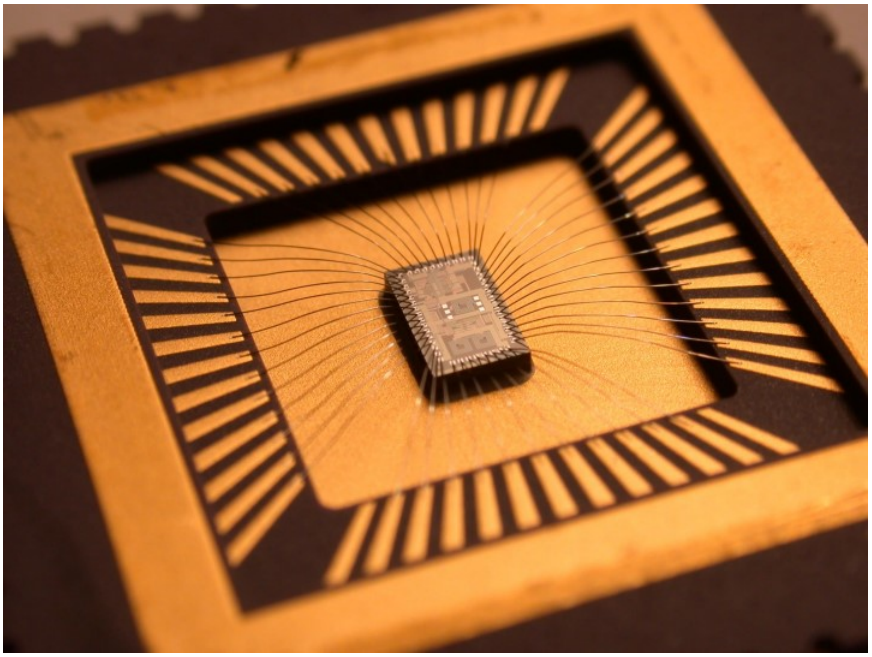


Figure 2: Packaging

Testing performance of a package is important, yet testing the circuitry which is the core of a package is more imperative. Thus, on-wafer measurements become demanding to provide a direct mean for learning the performance of an IC under test. De-embedding techniques, which will be introduced later in the course, could be used as well. However, it could introduces more errors into the characterization process, hence is not as desireable as on-wafer measurement. However, facilities required for such measurement are quite expensive. There must be a dedicated testing system for it. It is the *wafer prober*.

In this experiment, you will have a chance to earn a hands-on experience with the probe station. Please be advised that **the probe tips are very easily broken**. Handle the probe properly with high precaution. You will measure a simple coplanar waveguide with unknown characteristic impedance. Measurement data will be used to perform simulations to obtain a very famous tool used to judge the performance of interconnects in signal integrity engineering: the eye diagram.

The performance of high-speed digital systems is a strong function of the input-output bandwidth of the communication channels. Present-day applications require the transmission of data at multi-gigabit rates over interconnects in which channel signal degradation due to losses and crosstalk are prominent. *Skin effect* and *dielectric absorption* introduce dispersion in these channels and limit the overall performance at higher data rates. *Intersymbol interference* is observed when a symbol sent over a line at a certain time interferes with another symbol over the same line at a different time. This is due to the fact that the residual energy from the transmitted bit can be transferred to the next bit and thus corrupts the information. Intersymbol interference limits the maximum data rate that can be applied into a package. Interconnects are modeled as transmission lines and can be simulated using different design automation tools such as ADS. The effect of intersymbol interference is analyzed and demonstrated by using eye diagrams at different bit rates on different types of transmission lines.

Useful links:

1. `http://www.geek.com/chips/from-sand-to-hand-how-a-cpu-is-made-832492/`
2. `https://en.wikipedia.org/wiki/Wafer_testing`
3. `http://info.tek.com/rs/tektronix/images/54W-22137-X.pdf`

2 Background

Eye diagram

A serial digital signal can suffer impairments as it travels from a transmitter to a receiver. The transmitter, PCB traces, connectors, and cables will introduce interference that will degrade a signal both in its amplitude and timing. A signal can also suffer impairments from internal sources. For example, when signals on adjacent pairs of PCB traces or IC pins toggle, *crosstalk* among those signals can interfere with other signals. Thus, you need to determine at what point to place the oscilloscope probe in order to generate an eye diagram that will help you locate the source of the problem. Furthermore, where you place an oscilloscope's probe will produce differing signals on the display.

An eye diagram is a common indicator of the quality of signals in high-speed digital transmissions. An oscilloscope generates an eye diagram by overlaying sweeps of different segments of a long data stream driven by a master clock. The triggering edge may be positive or negative, but the displayed pulse that appears after a delay period may go either way; there is no way of knowing beforehand the value of an arbitrary bit. Therefore, when many such transitions have been overlaid, positive and negative pulses are superimposed on each other. Overlaying many bits produces an eye diagram, so called because the resulting image looks like the opening of an eye.

In an ideal world, eye diagrams would look like rectangular boxes. In reality, communications are imperfect, so the transitions do not line perfectly on top of each other, and an eye-shaped pattern results. On an oscilloscope, the shape of an eye diagram will depend upon various types of triggering signals, such as clock triggers, divided clock triggers, and pattern triggers. Differences in timing and amplitude from bit to bit cause the eye opening to shrink.

As can be seen in Figure 3, an eye diagram can reveal important information. It can indicate the best point for sampling, divulge the SNR (signal-to-noise ratio) at the sampling point, and indicate the amount of jitter and distortion. Additionally, it can show the time variation at zero crossing, which is a measure of jitter [1].

Eye diagrams provide instant visual data that engineers can use to check the signal integrity of a design and uncover problems early in the design process. Used in conjunction with other measurements such as bit-error rate, an eye diagram can help a designer predict performance and identify possible sources of problems.

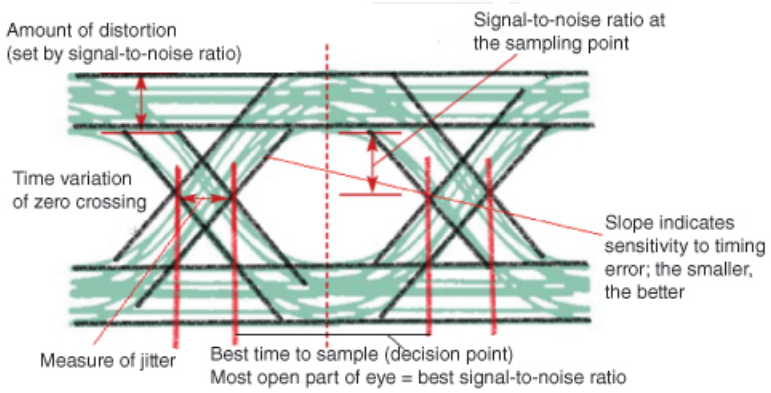


Figure 3: A typical eye diagram [1]

In ADS, eye diagram is generated using a dedicated solver, namely the ChannelSim simulator.

Wafer prober

A wafer prober station is a mechanical system used to physically acquire signals from the internal nodes of a semiconductor device. The probe station utilizes manipulators which allow the precise positioning of thin "needles" on the surface of an on-wafer circuit. Figure 4 shows the probe station measuring a wafer sample. The "needles" are parts of the probe tip. They are used to make contact between the test ports of the VNA and the circuit under test.

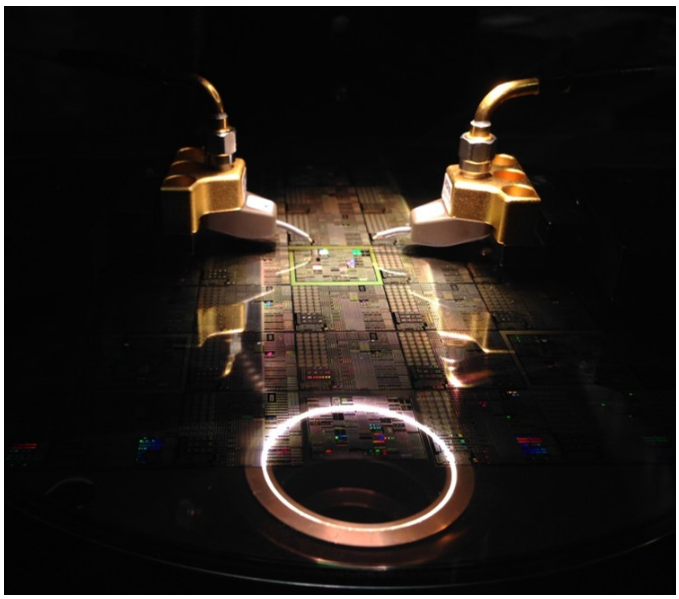


Figure 4: Wafer testing using probe station

There are various types of probe tips. One of which is the ACP series probe shown in Figure 5. There are various style of probe, ground-signal-ground (GSG) is the most common type of RF probe. This is similar to coplanar waveguide. Ground-signal (GS/SG) probes are also available. This probe would be needed if your RF circuit only had one ground pad.

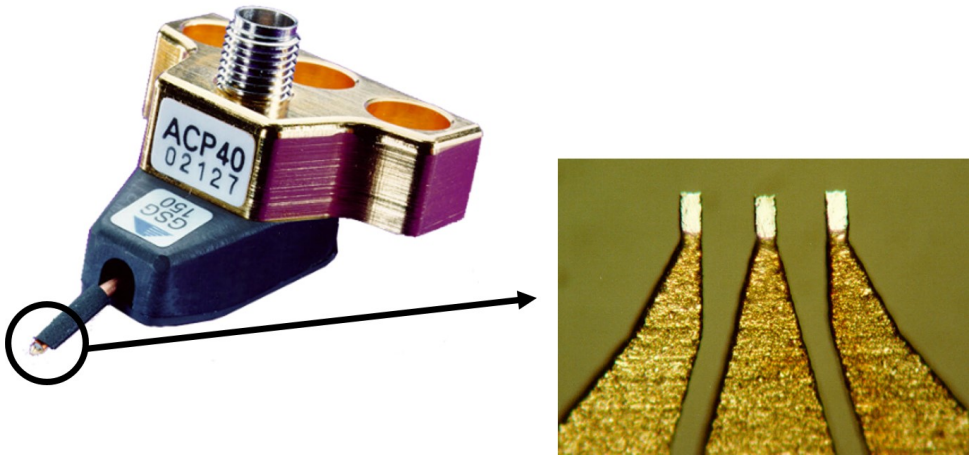


Figure 5: ACP Series probe

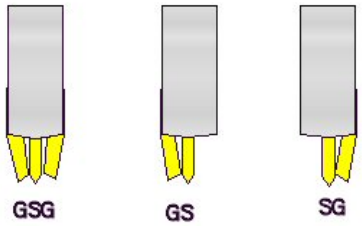


Figure 6: Probe styles

Here is a few tips how to make on-wafer measurement without damaging the equipment.

- **Always put the probe high enough so that it does not hit the chuck surface or the DUT when the probe platen handle comes down. Always put the probe high enough so that when you move the probe to different locations on the DUT or when you move the chuck base, the probes won't scratch the DUT surface.**

- Adjust the zoom and focus so that you could clearly see the DUT on the wafer surface. When the probe is lowered down to touch the DUT, it will eventually enters the focus range of the camera, you will see it clearer and clearer. That is when you should slow down, carefully lower the probe bit by bit. On Figure 7, port 1 probe is making contact with the DUT while port 2 probe is not.

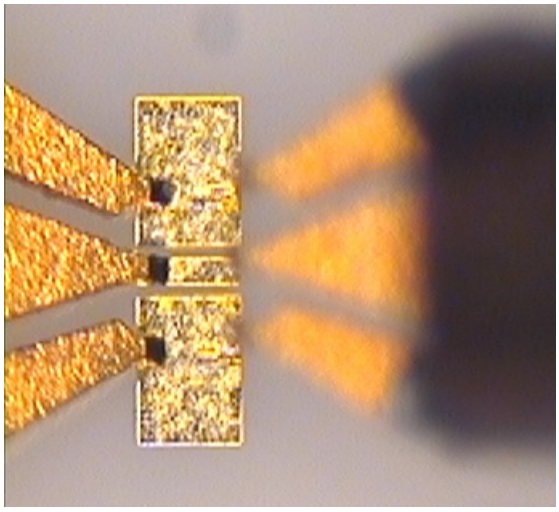


Figure 7: A THRU is measured, port 1 probe is well aligned and contacts while port 2 probe is above the wafer surface

- As the probe makes contact with the surface, the contact force will cause it to move forward a little bit, this is called *"skate"*. About 25-30 micron (μm) of skate is required to make a good contact. Too much skate will scratch the ISS surface severely.
- You should align the probe well using the alignment marks on the ISS.
- You should simultaneously look at the camera capture as well as the VNA to know the probe has made contacts with the DUT surface. For example, Figure 8 shows that as soon as your port 2 probe touches the 50Ω standard, you should obtain the Smith Chart on the right.

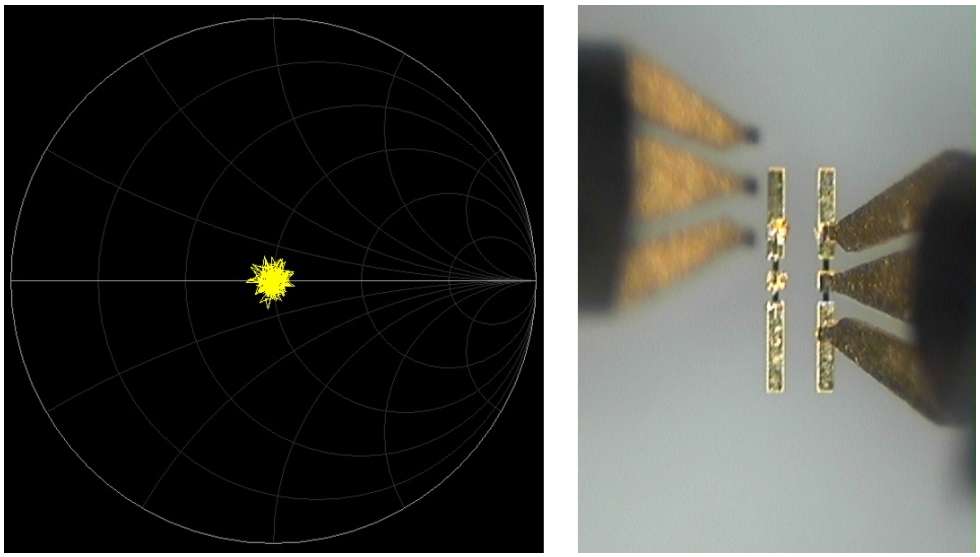


Figure 8: As soon as the probe contacts a 50Ω standard, corresponding change is instantly observed on VNA

Here is a series of video tutorial for the probe station usage: `https://www.cascademicrotech.com/support/probes-support/rf-probe-setup-videos/rf-probe-video-guide`

3 Pre-lab

1. What is coplanar waveguide? How does electromagnetic waves travel through a coplanar waveguide (medium, mode, speed)? What are advantages and disadvantages of using a coplanar waveguide?

2. How to generate an eye diagram of a digital signal from a sequence of bits?
3. A transmission line is designed to support 5Gbps data rate, what is the Unit time Interval (UI)[1] of the data signal?
4. A transient signal has the rise/fall time is 10 psec. How large does the spectrum of this signal span?

4 Equipment

- CMT S5048 Compact VNA.
- Cascade Microtech 101-190 SOLT Impedance Standard Substrate (ISS).
- On-wafer DUT.
- Keysight ADS.

5 Procedure

Part I - On-wafer measurement

1. Go to `https://www.cascademicrotech.com/files/iss_map_101-190.pdf` to see the standard map. Notice that the standards are arranged in columns and rows. **Ask your TA which standard set you should use for your measurement**.
2. Set frequency range for your on-wafer measurement to 20kHz-6GHz.
3. Perform SOLT calibration on the probe station and measure the DUTs, collect data then plot it on Smith Chart.

Part II - Eye diagram simulation

1. Eye diagram simulation using **Transient** simulator with determinstic bit sequences

   Open ADS, create a new workspace. Draw the schematic diagrams and run the transient simulation.

   VtBitSeq item can be found in the palette 'Sources-Time Domain'.

   TLIN (ideal transmission line model) in 'TLines-Ideal' palette.

   TRANSIENT in 'Simulation-Transient' palette.

   Label the nodes before and after your SnP block (click on the NAME icon on the toolbar immediately above your schematic window). Run the simulation.

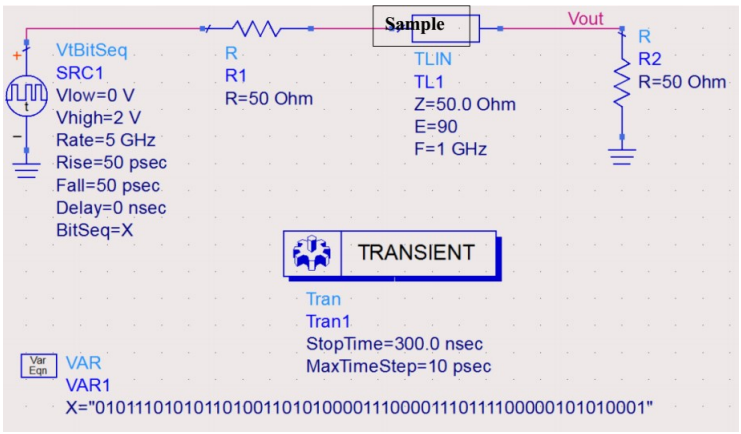


Figure 9: Eye diagram generation with a 5Gbps data transmission using Transient simulator

[1] `https://en.wikipedia.org/wiki/Unit_interval_(data_transmission)`

After running the simulation, open a data display window. Use FrontPanel_eye()[2] command in ADS to create data for the eye data plot. Then plot it on a retangular plot, you will have the eye diagram.

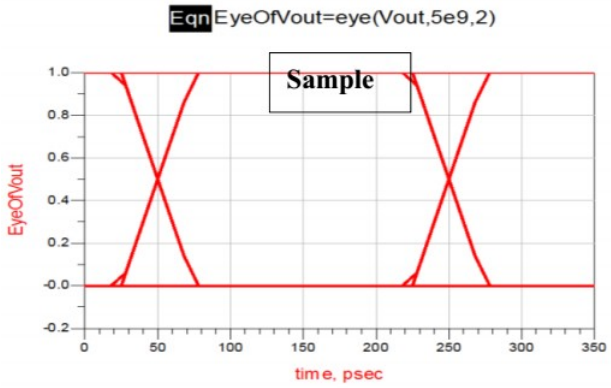


Figure 10: Eye diagram of a 5 Gbps data transmission over an ideal 50 ohm matched line

2. Eye diagram using statistical tool **ChannelSim** [3]

Now we will use a different approach. In modern systems error rates are usually very low. Therefore, to reliably analyze such systems one will have to run very long transient simulations (very long bit sequences). Instead of creating an actual predefined bit sequence and running a transient simulation, we will employ statistical channel analysis. Parts used in the schematic below are found in the 'Simulation-ChannelSim' palette. We will observe transmission through a microstrip transmission line rather than ideal T-line model. You will need to specify parameters of the line (MLIN component found in 'TLines-Microstrip') and the substrate ('MSub' component) as shown in Figure 11.

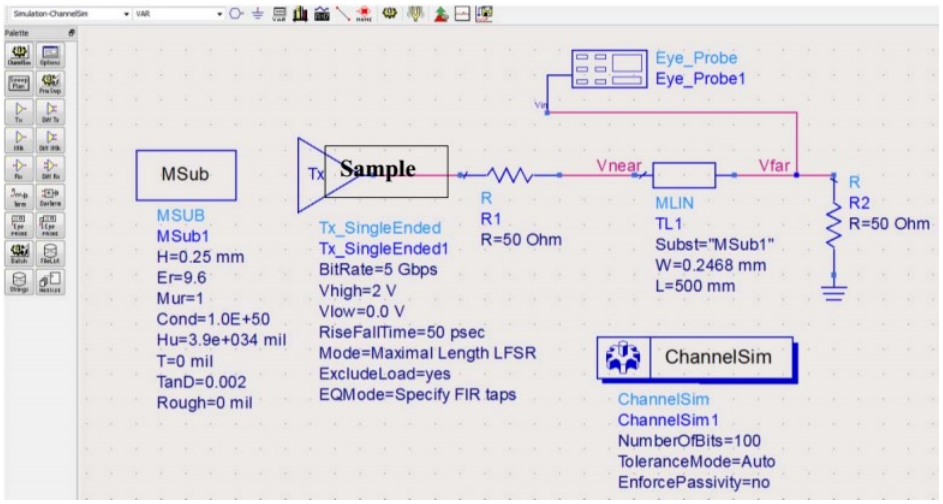


Figure 11: Schematic of a 5 Gbps data transmission over a microstrip line.

Tx is the statistical model of a driver (source) who launches a sequence of bits into the microstrip line which is loaded with a 50 ohms receiver represented by a 50Ω resistor.

In the Data Display window you can plot 'Density' to observe the eye diagram pattern as in Figure 12

[2] http://edadocs.software.keysight.com/pages/viewpage.action?pageId=5088729
[3] `http://edadocs.software.keysight.com/pages/viewpage.action?pageId=5081595`

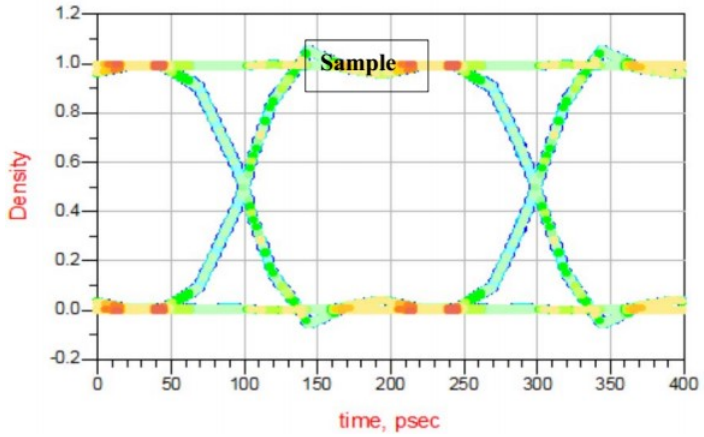


Figure 12: Eye diagram of a 5 Gbps data transmission over a Microstrip Line.

Change the RiseFallTime parameter of the transmitter (10 psec, for instance). Also try changing the width of the microstrip line to W = 0.03 mm (which approximately corresponds to characteristic impedance Zc = 100 Ohms). Include the eye diagrams in your report and comment on the results.

Let's do another example, this time, we will extend the design space to multi-layer circuits. Shown in Figure 13 is a simple cross-section of a multi-layer PCB where there are two (02) microstrip on two sides of the board, they are connected by a *via*[4].

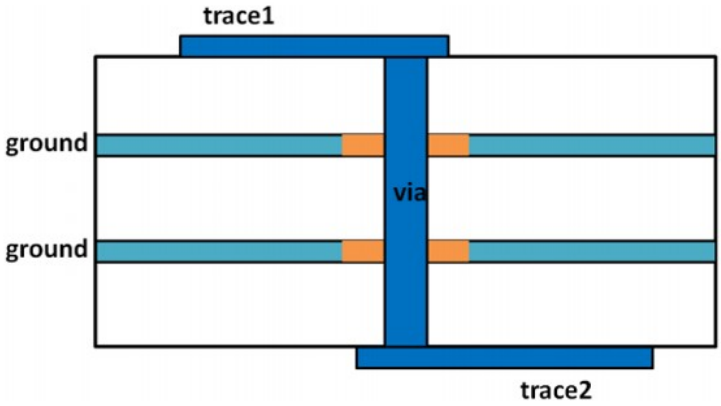


Figure 13: Transmission line discontinuity by *via* in multi-layer circuit

Figure 14 shows an equivalent circuit model for the structure in Figure 13 in which the via is modelled by a lumped circuit with $L = 0.5nH$ and $C = 2.0pF$. There are many factors have been ignored and we have an ideal case here. Set up the simulation as shown in Figure 14.

[4] http://www.interfacebus.com/Dictionary-of-Printed-Circuit-vias-in-high-speed-design.html

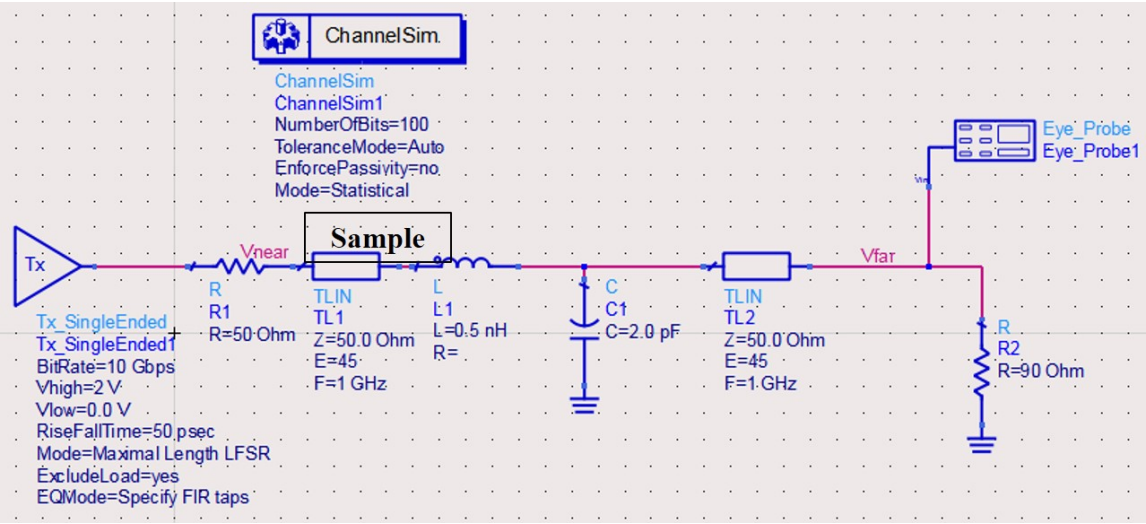


Figure 14: Simple model for Figure 13

Obtain the eye diagram similar to Figure 15. You should be able to observe that the eye is bad eventhough we use ideal models in Figure 14.

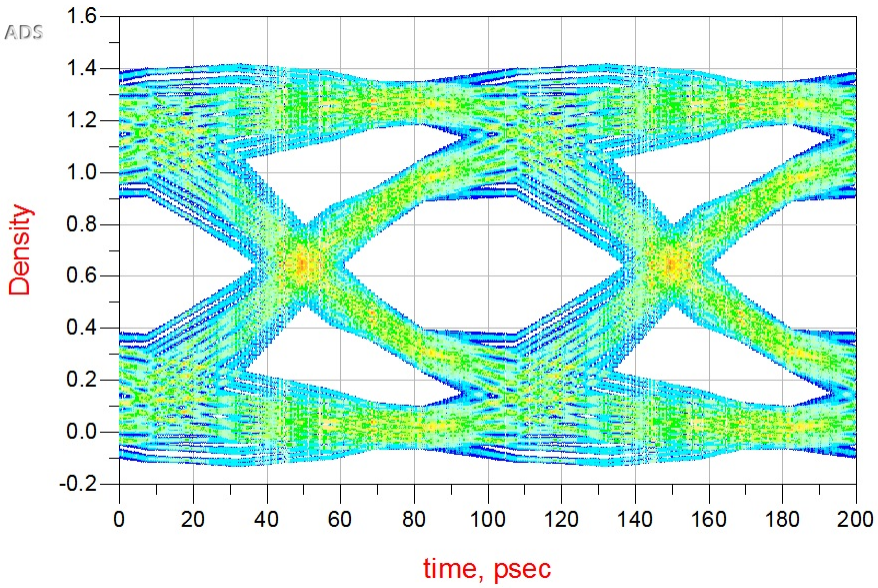


Figure 15: Eye diagram of the receiver voltage in Figure 14

Explain the reason why such a design in Figure 14 gives such a bad eye as in Figure 15. Try to fix the design, resimulate the circuit and obtain the new eye to prove your fix works. What is your consclusion about this?

3. Eye diagram with real measurement data

   Now you have been familiar with how to set up a channel simulation, use your measurement of Part I to obtain the eye diagram when you use the measured channel in Part I to transmit data at 2Gbps. Your set up should look like Figure 16.

   Submit a screenshot of your schematic windows and eye diagram. State clearly your choice of RiseFallTime. Show your calculations. Comment on the result.

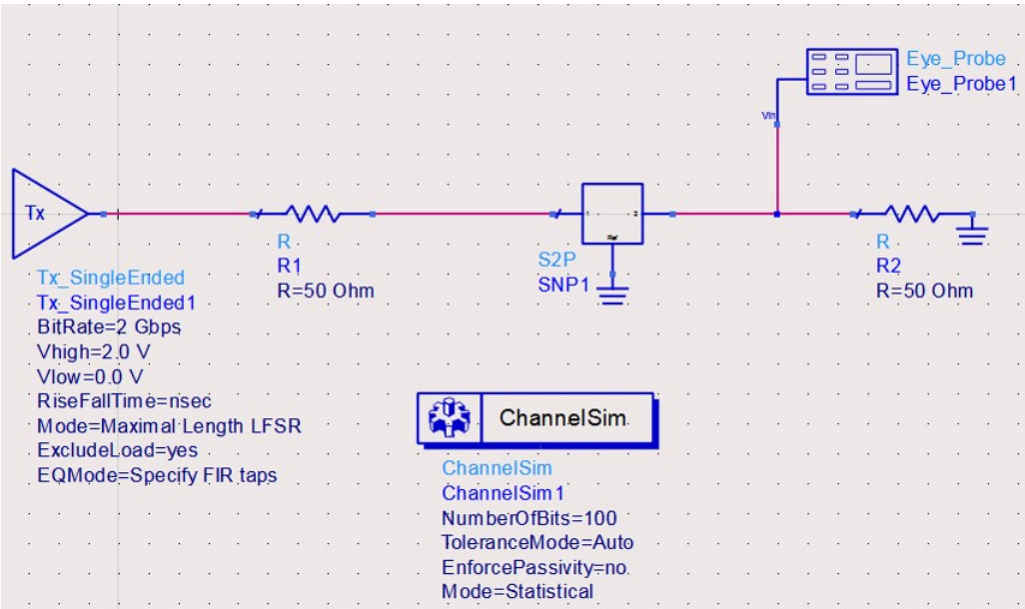


Figure 16: Schematic to simulate the eye diagram of the measured transmission line

6 Conclusion

1. How is having a matched system important? Show data to prove your answer.
2. How does a high data rate requirement affect a channel design (i.e. as data rate increases, what is the requirement on bandwidth of your transmission line)? Why is it (designing a good channel at high frequency) a difficult problem to solve?

References

[1] Gary Breed. Analyzing Signals Using the Eye Diagram. *High Frequency Electronics*, nov 2005.