ECE 451
Packaging Technologies

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Need for Heterogeneous Integration - 1

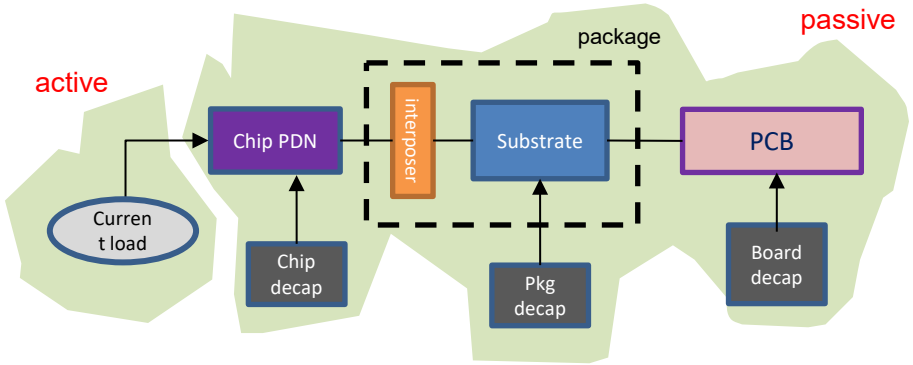
AI Requirements

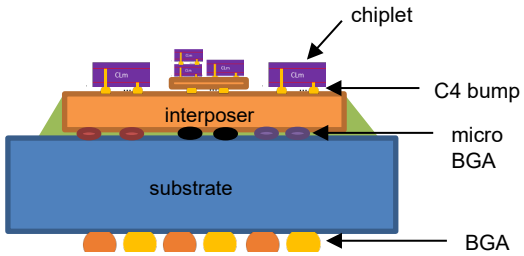
Training a large language model like GPT-3, for example, is estimated to use just under **1,300 megawatt hours (MWh)** of electricity; about as much power as consumed annually by 130 US homes. To put that in context, streaming an hour of Netflix requires around 0.8 kWh (0.0008 MWh) of electricity. That means you'd have to watch 1,625,000 hours to consume the same amount of power it takes to train GPT-3.

Source: James Vincent, How much electricity does AI consume? The Verge - 2/16/2024
https://www.theverge.com/24066646/ai-electricity-energy-watts-generative-consumption

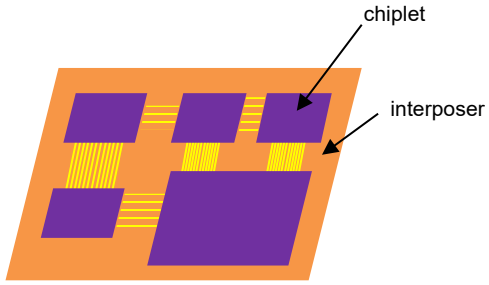
Need for Heterogeneous Integration - 3

Chiplet PDN

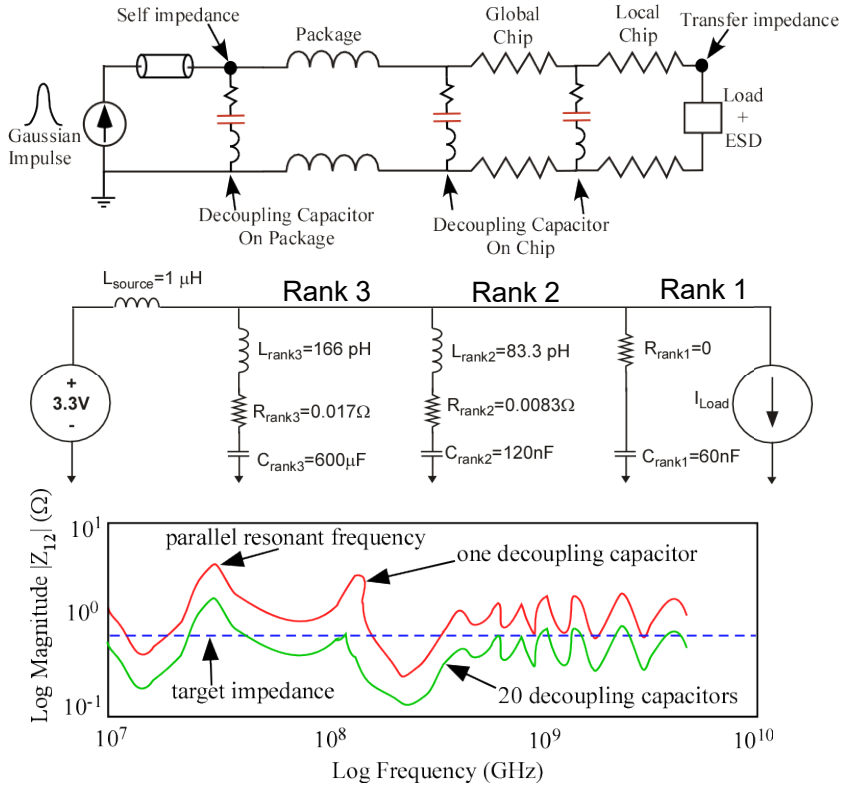




Package side view

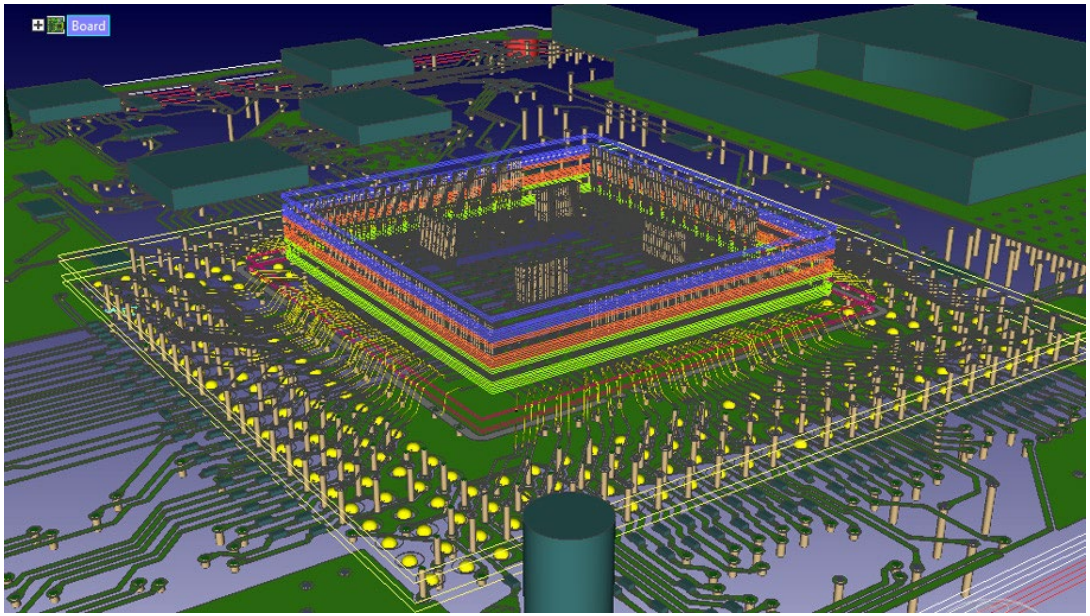


Interposer top view



Heterogeneous Integration

- Focus on minimizing energy and delay
- Identify and address conflicting requirements,
- Take advantage of novel interconnect technologies
- Leverage from AI methodologies
- Address design and computational complexity



System-Level Integration (Microelectronic Packaging)

Semiconductor

* Unprecedented Innovations in CMOS, Si-Ge,Copper Wiring
* Fundamental technical Limits

Electronic Systems

* Computers, telecom & Consumer Products Merge
* Portable, Wireless, & Internet Accessible
* Very Low Cost & Very High Performance

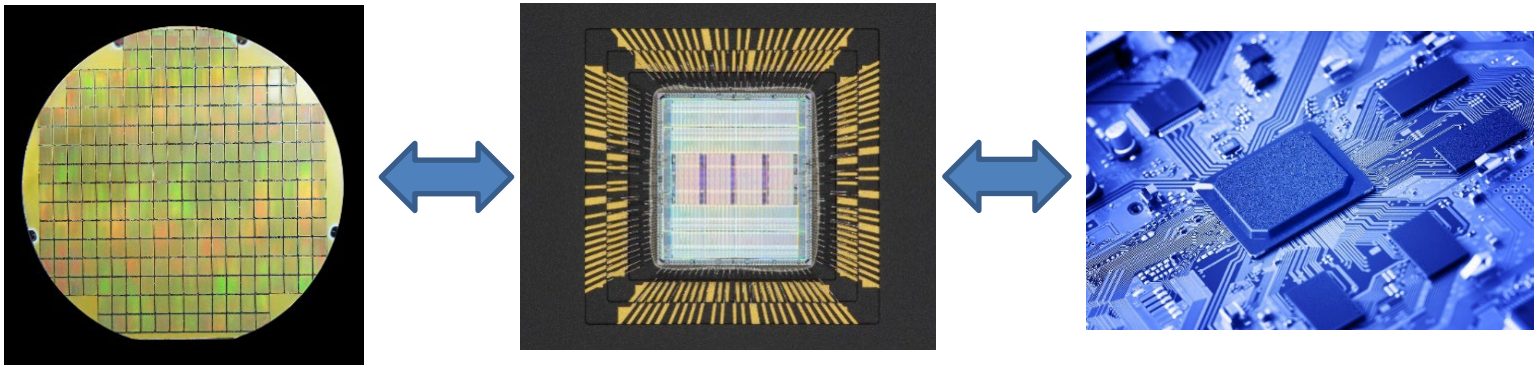
Microelectronic Packaging

* High Cost, Low Performance, Low Reliability
* Lack of Skilled Human Resources

Packaging Challenges

- Package is bottleneck to system performance
- Package cost is increasing percentage of system cost
- Package limits IC technology
- On-chip system can outperform package capability

Levels of Integration



CHIP

- Transistors
- Nonlinear
- SPICE
- Scaling with tech

PACKAGE

- Interconnects
- Linear
- EM Tools
- Scaling with λ

BOARD

- Transmission lines, sensors
- Linear+Nonlinear
- EM Extraction, SPICE, IBIS,…
- Scaling with λ

Advantages of SOC

* Fewer Levels of Interconnections
* Reduced Size and Weight
* Merging of Voice, Video, Data,...

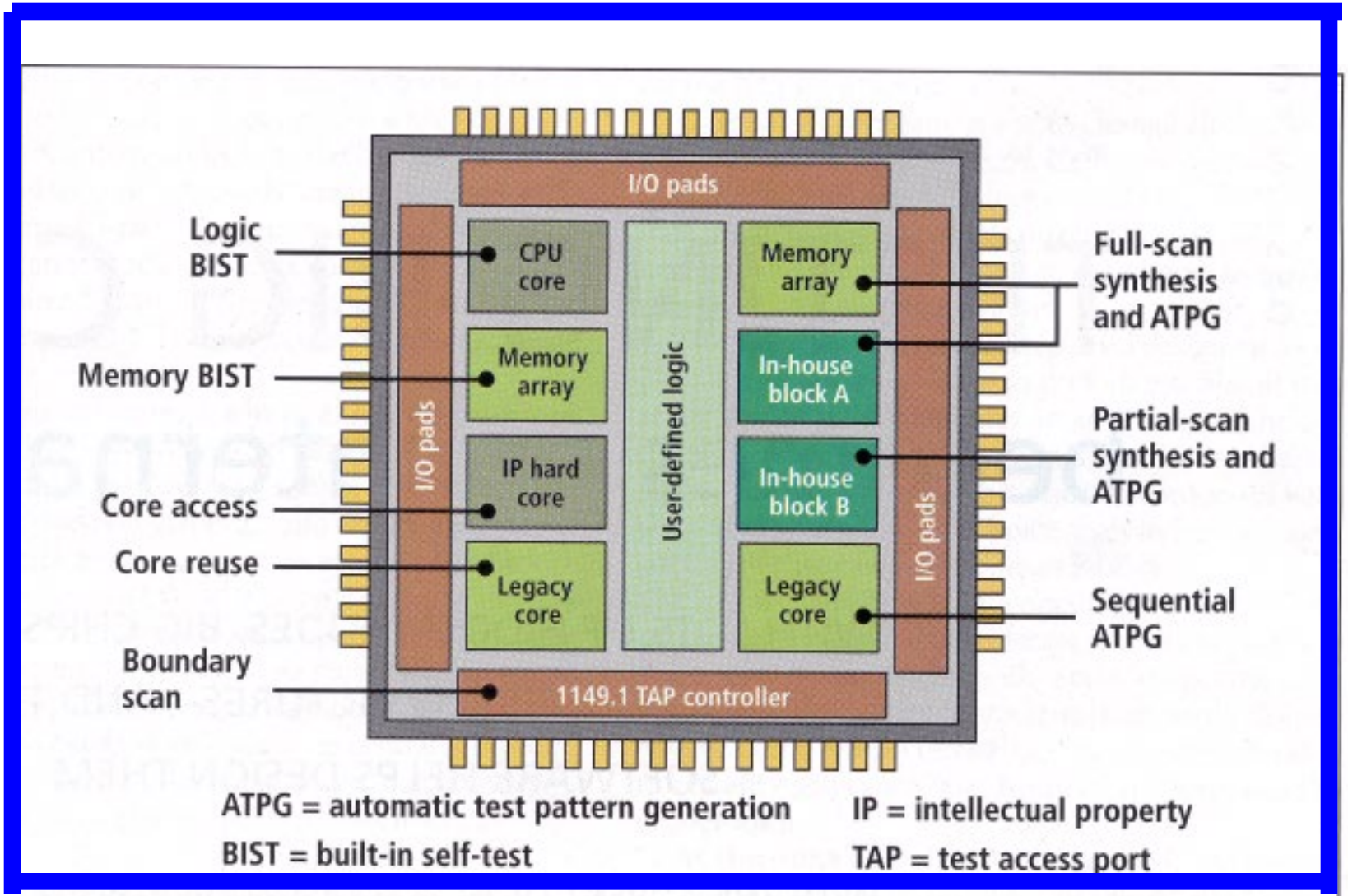
Arguments against SOC

* Challenges too Big
* Legal issues

Challenges for SOC

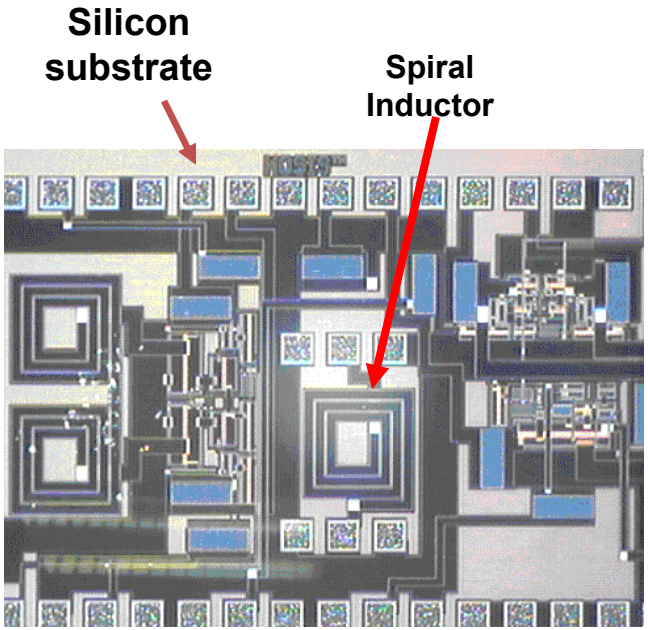
* Different Types of Devices
* Single CMOS Process for RF and Digital
* Design Methodology not available
* EDA Tools cannot handle level of complexity
* Intellectual Property
* Signal Integrity
* High-Power Requirements of PA

System on a Chip (SOC)



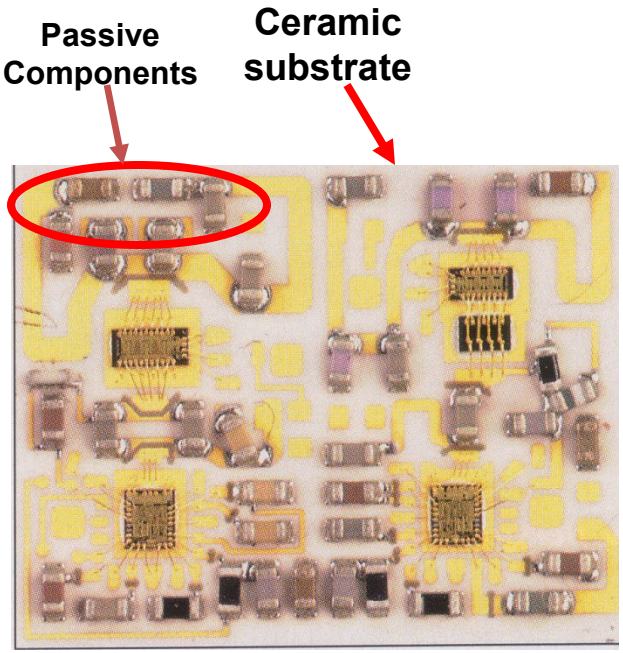
SOC vs SOP

System on Chip



Voltage Controlled Oscillator
(UIUC-CAD group – 1999)

System on Package



Triple-band GSM/EDGE Power Amp Module
(RF Design Magazine – 4/02)

SOP vs SOC

	SOP	SOC
Low cost consumer products (<$200)	YES	YES
Portable products ($200-$2000)	YES	NO
Single processor products ($1-$5K)	YES	NO
High Performance Products (>5K)	YES	NO
Automotive and Space Applications	YES	NO

RF Front End Technologies

Product	PA	LNA	Mixer	VCO	Filter	Switch
Technology (Standard)	GaAs Si SiGe	Si	Si	Si GaAs	Si	Si GaAs
Technology (Alternate)	InP GaAs SiGe	InP GaAs	InP GaAs	InP GaAs	MEMS	InP GaAs MEMS
Criterion	PAE, linearity	Low power	Linearity, 1/f noise	1/f noise	High Q	Isolation, Insertion loss

Transistor Technologies

	Si Bipolar	GaAs MESFET	GaAs HBT	InP HBT
base resistance	high	-	low	low
transit time	high	-	low	low
Beta*Early voltage	low	-	high	high
col-subst capacitance	high	-	low	low
turn on voltage	0.8	-	1.4	0.3
thermal conductivity	high	-	low	medium
transconductance	50X	1	50X	50X
device matching	< 1 mV	> 10 mV	1 mV	1 mV
hysteresis or backgating	negligible	> 10 mV	negligible	negligible
breakdown voltage	< 10 V	> 8 V	> 10 V	low
fT (GHz)	30	100	100	160

Trends & Enabling Technologies

Materials/Processing

- RF CMOS, SiGe
- AlGaAs/GaAs, InGaP/GaAs
- Metamorphic GaAs
- InP SHBT, DHBT

Radio Architectures

- Polar vs Cartesian loop
- Direct Conversion
- Software Radio

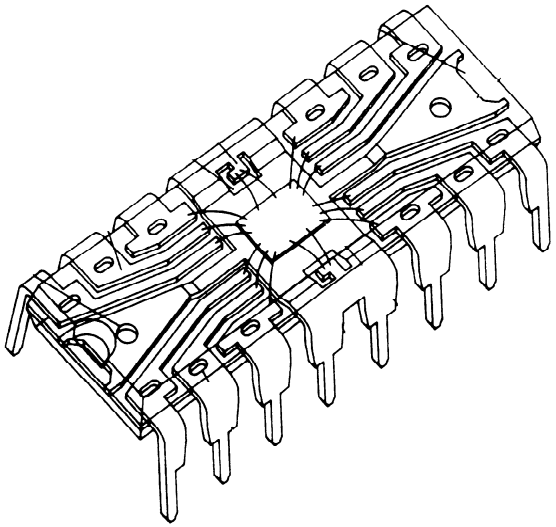
CAD Tools

- Device behavioral models
- RF Time-domain tools
- Fast Solvers

Packaging

- Differential designs
- RF MEMS
- LTCC

Dual-in-Line (DIP) Package

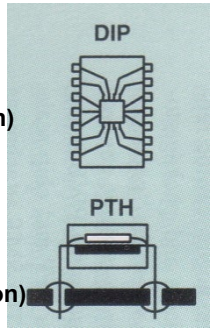


- Mounted on PWB in pin-through-hole (PTH) configuration
- Chip occupies less than 20% of total space
- Lead frame with large inductance

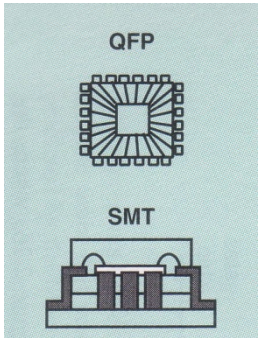
Package Types

Top View
(showing chip topackage connection)

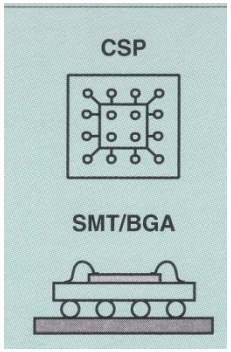
Plane View
(showing package to board connection)



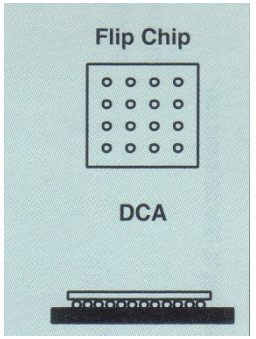
DIP



QFP



CSP



Flip Chip

	DIP	QFP	CSP	Flip Chip
Chip Size (mm × mm)	5 ×5	16 × 16	25 ×25	36 × 36
Chip Perimeter (mm)	20	64	100	144
Number of I/Os	64	500	1600	3600
Chip Pad Pitch (μm)	312	128	625	600
Package Size (in × in)	3.3 × 1.0	2.0 × 2.0	1.0 × 1.0	1.4 × 1.4
Lead Pitch (mils)	100	16	25	24
Chip Area (mm^2)	25	256	625	1296
Feature Size (μm)	2.0	0.5	0.25	0.125
Gates/Chip	30K	300K	2M	10M
Max Frequency (MHz)	5	80	320	1280
Power Dissipation (W)	0.5	7.5	30	120
Chip Pow Dens (W/cm^2)	2.9	4.8	9.3	2.0
Pack Pow Dens (W/cm^2)	0.024	0.3	4.8	9.8
Supply Voltage (V)	5	3.3	2.2	1.5
Supply Current (A)	0.1	2.3	13.6	80

Substrate Materials

Material	Surface roughness (μm)	$10^4 \tan\delta$ at 10 GHz	ε_r	Thermal conductivity K ($W/cm^2/^oC$)	Dielectric strength (kV/cm)
Air (dry)	N/A	~0	1	0.00024	30
Alumina: 99.5% 96% 85%	 0.05-0.25 5-20 30-50	 1-2 6 15	 10.1 9.6 15	 0.37 0.28 0.2	 4×10^3 4×10^3 4×10^3
Sapphire	0.005-0.025	0.4-0.7	9.4,11.6	0.4	4×10^3
Glass, typical	0.025	20	5	0.01	-
Polyimide	-	50	3.2	0.002	4.3

Substrate Materials

Material	Surface roughness (μm)	$10^4 \tan\delta$ at 10 GHz	ε_r	Thermal conductivity K ($W/cm^2/^oC$)	Dielectric strength (kV/cm)
Irradiated polyolefin	1		2.3	0.001	~300
Quartz (fused) i.e. SiO2	0.006-0.025	1	3.8	0.01	10×10^3
Beryllia	0.05-1.25	1	6.6	2.5	-
Rutile	0.25-2.5	4	100		-
Ferrite/garnet	0.25	2	13-16	0.03	4×10^3

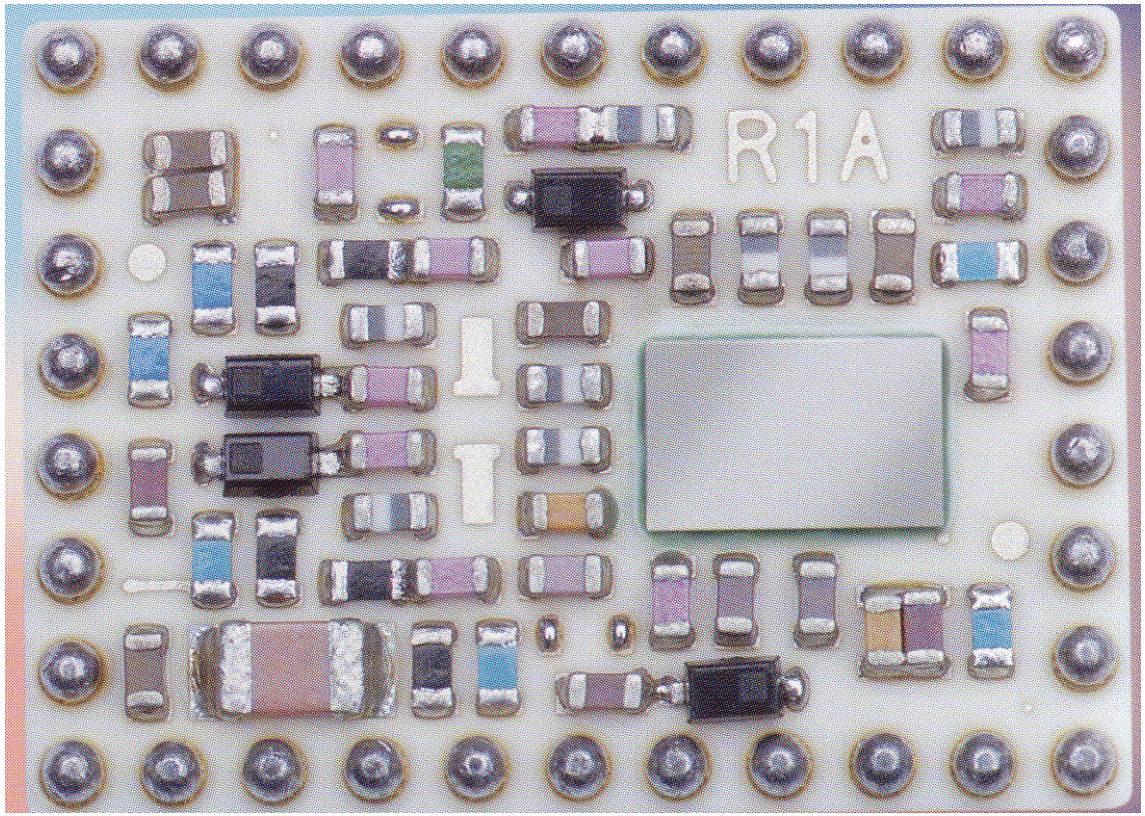
Substrate Materials

Material	Surface roughness (μm)	$10^4 \tan\delta$ at 10 GHz	ε_r	Thermal conductivity K ($W/cm^2/^oC$)	Dielectric strength (kV/cm)
FR4 circuit board	~6	100	4.3-4.5	0.005	-
RT-duroid 5880	0.75-1 4.25-8.75	5-15	2.16-2.24	0.0026	-
RT-duroid 6010	0.75-1 4.25-8.75	10-60	10.2-10.7	0.0041	-
AT-1000	-	20	10.0-13.0	0.0037	-
Cu-flon	-	4.5	2.1	-	-

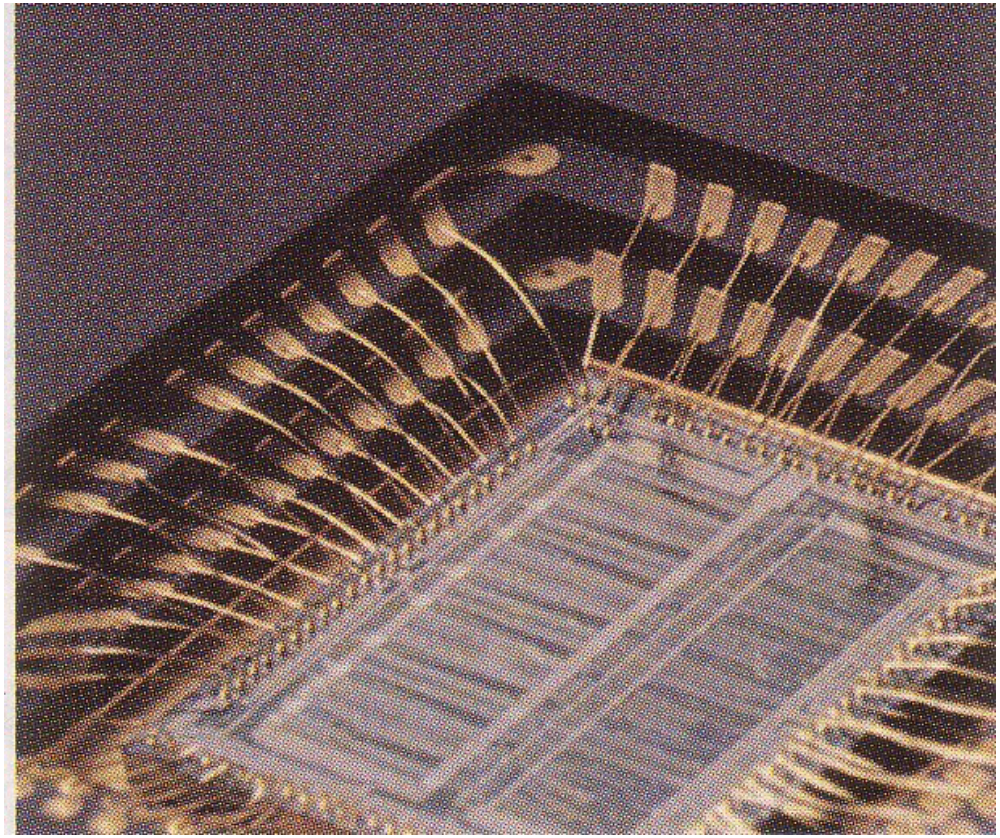
Substrate Materials

Material	Surface roughness (μm)	$10^4 \tan\delta$ at 10 GHz	ε_r	Thermal conductivity K ($W/cm^2/^oC$)	Dielectric strength (kV/cm)
Si (high resistivity)	0.025	10-100	11.9	0.9	300
GaAs	0.025	6	12.85	0.3	350
InP	0.025	10	12.4	0.4	350
SiO2 (on chip)	-	-	4.0-4.2	-	-
LTCC (typical green tape 951)	0.22	15	7.8	3	400

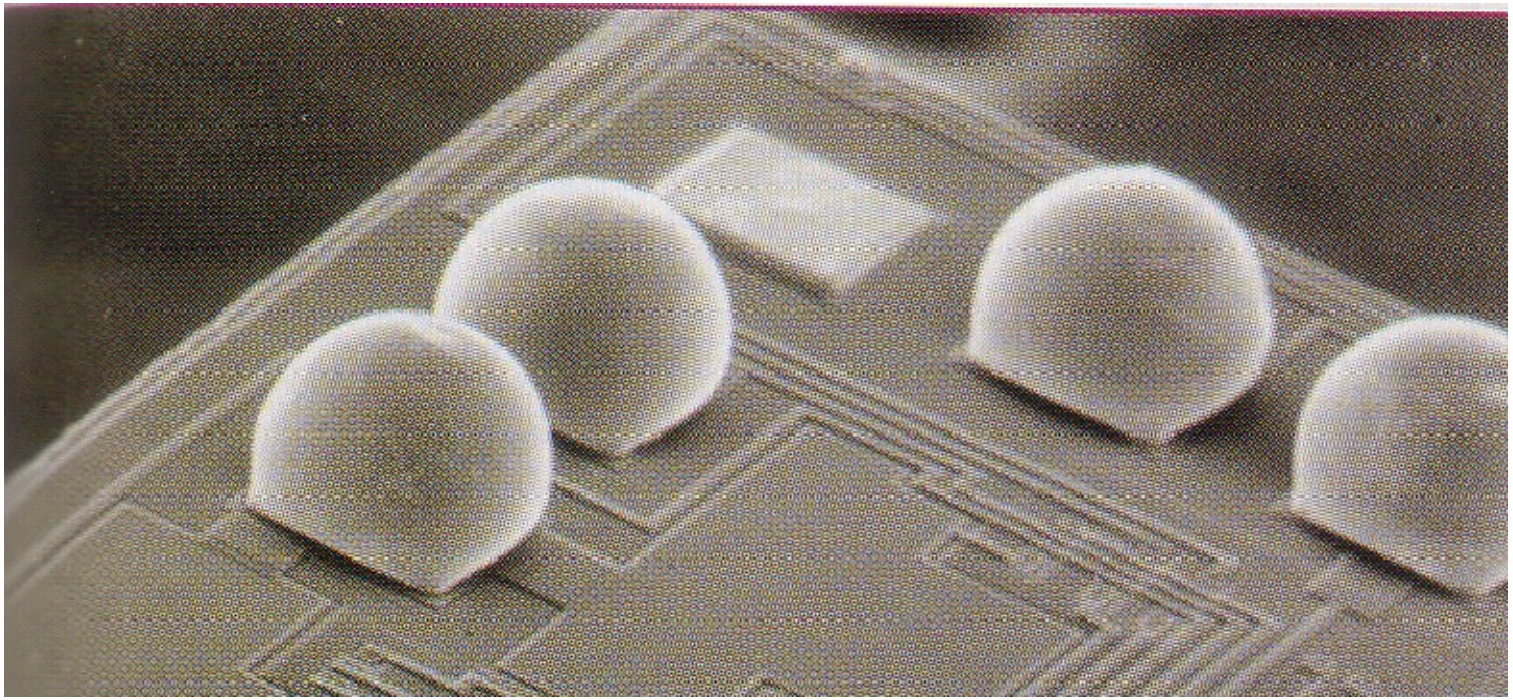
Ceramic Substrate



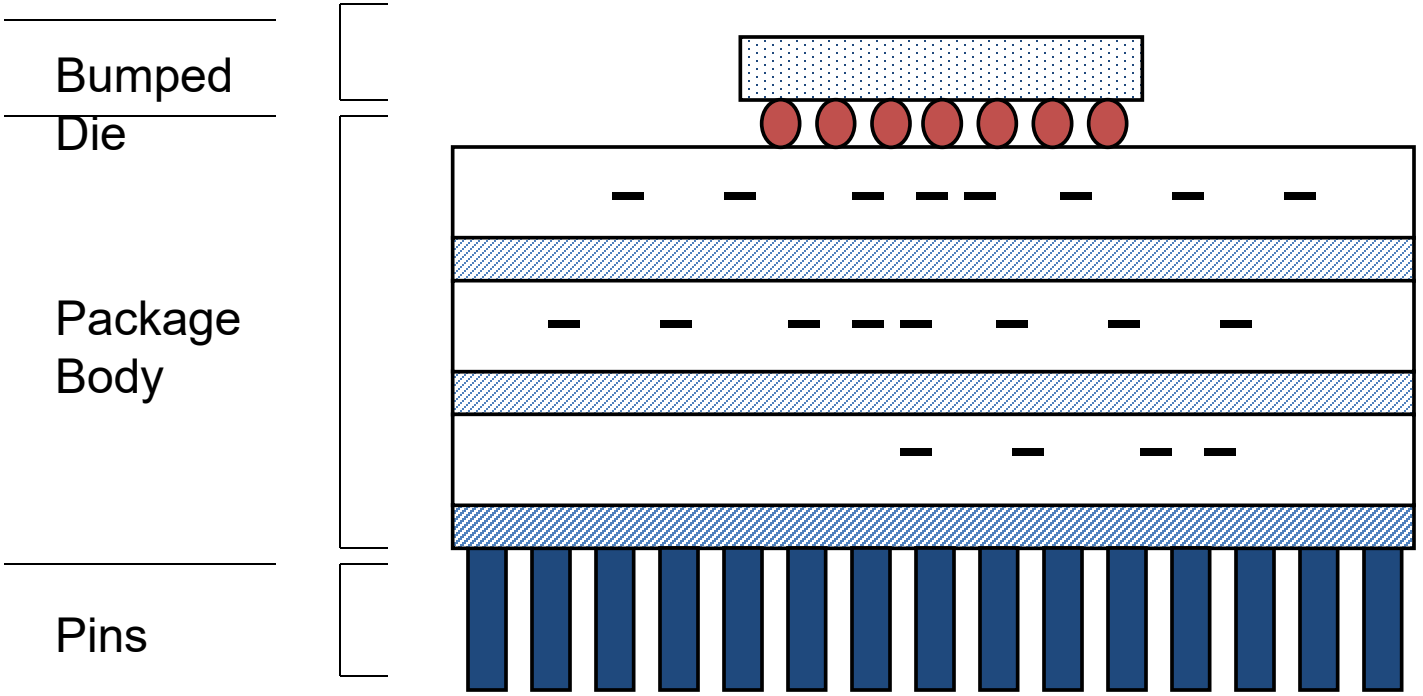
Stacked Wire Bonds



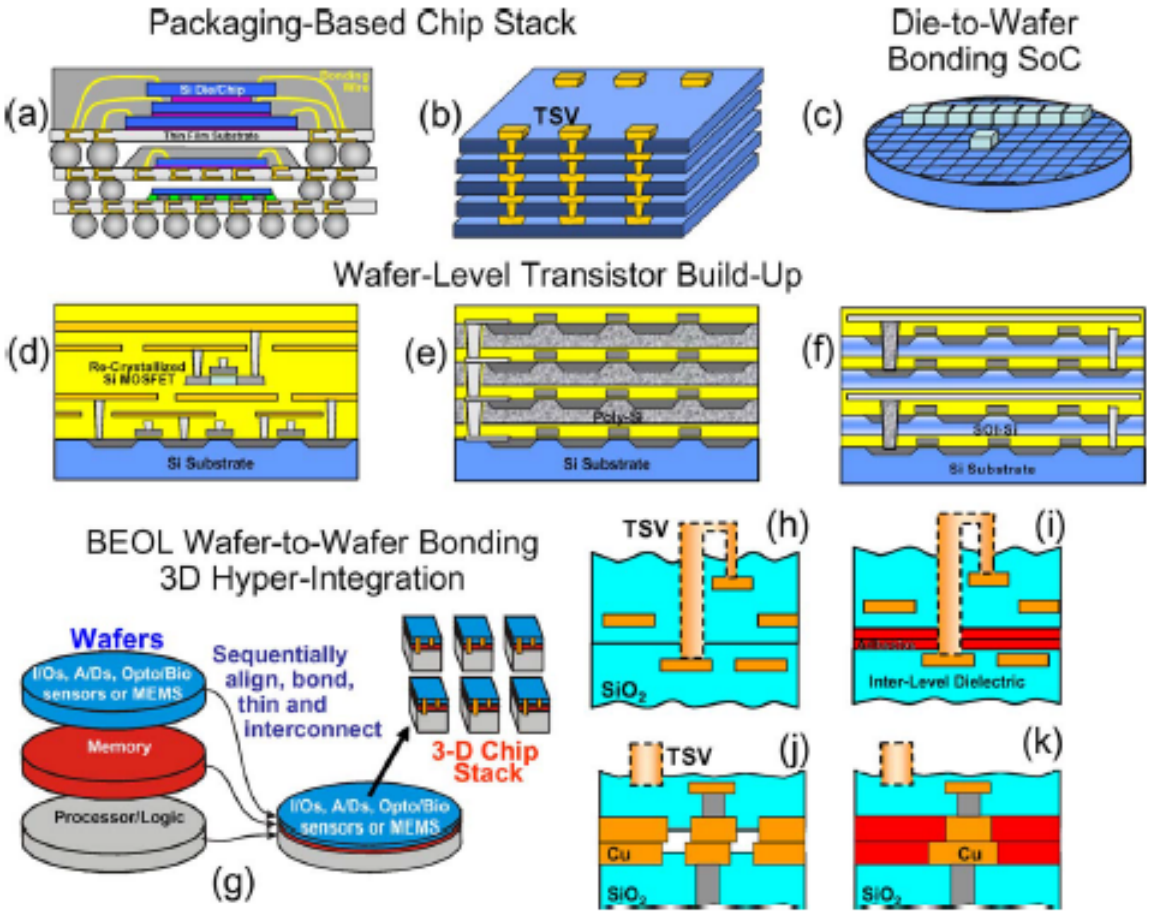
Ball Bonding for Flip Chip



Flip Chip Pin Grid Array (FC-PGA)

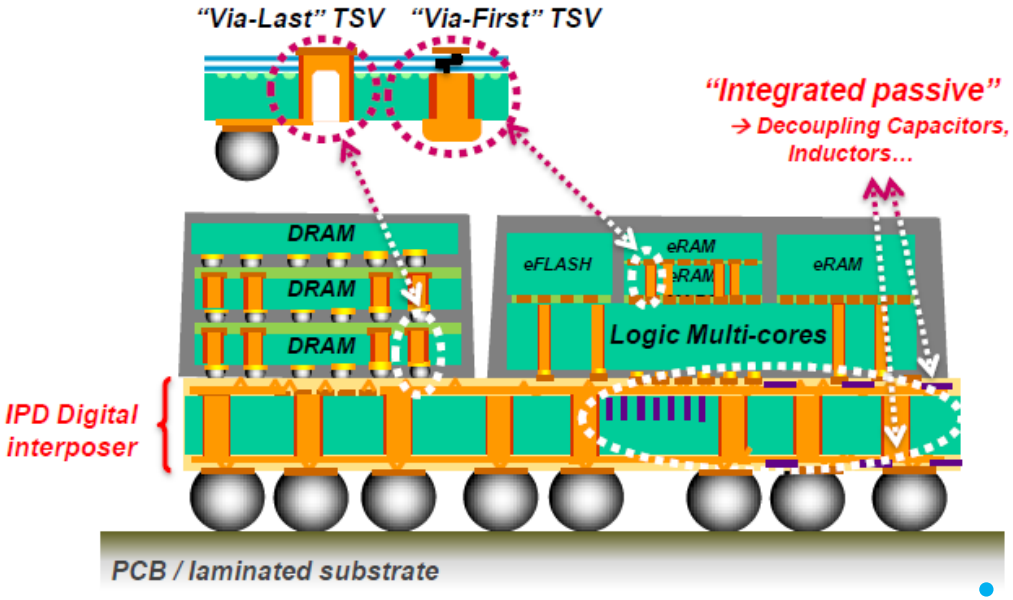


3D Packaging



Source: Jian-Qiang Lu, "3-D Hyperintegration and Packaging Technologies for Micro-Nano Systems", Proceedings of the IEEE, pp 18-30, Vol. 97, No. 1, January 2009.

3D Packaging



Source: Yole Report 2009.

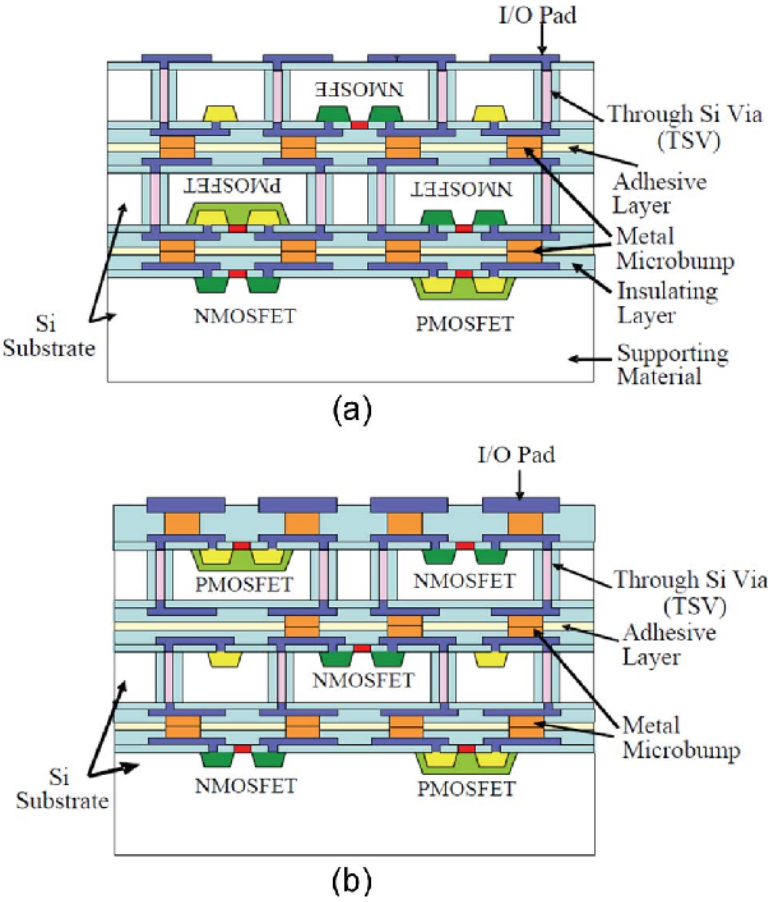
Key concepts

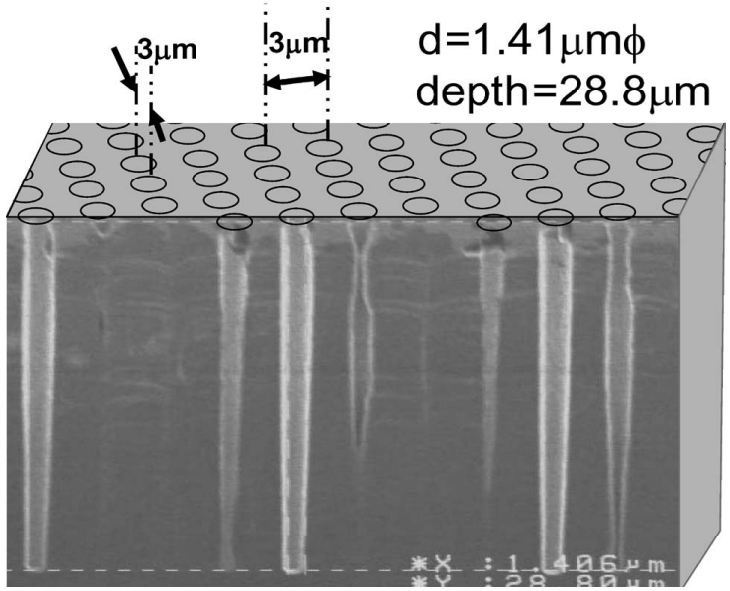
- Wires
  - shorter
  - lots of it
- Heterogeneous integration
  - Analog and digital
  - Technologies (GaAs and Si?)

3D Industry

- Samsung
  - 16Gb NAND flash (2Gx8 chips) Wide Bus DRAM
- Micron
  - Wide Bus DRAM
- Intel
  - CPU + Memory
- OKI
  - CMOS Sensor
- Xilinx
  - 4 die 65 nm interposer
- Raytheon/Ziptronix
  - PIN Detector Device
- IBM
  - RF Silicon Circuit Board/ TSV Logic & Analog
- Toshiba
  - 3D NAND

Through-Silicon Vias





From: M. Motoshi, "Through-Silicon Via, Proc. of IEEE Vol. 97, No. 1, January 2009.

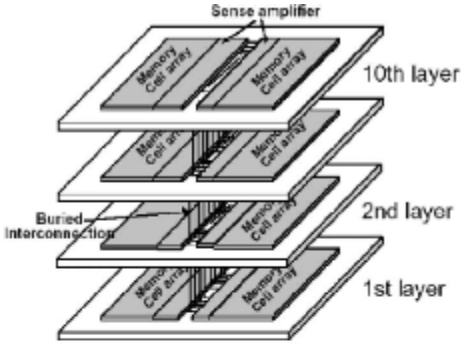
Mitsumasa Koyanagi," High-Density Through Silicon Vias for 3-D LSIs" Proceedings of the IEEE, Vol. 97, No. 1, January 2009

TSV Density: $10/cm^2$ - $10^8/cm^2$

Through-Silicon Vias (TSV)

Advantages

- Make use of third dimension
- several orders of magnitude ($10/cm^2$ to $10^8/cm^2$)
- Minimize interconnection length
- More design flexibility



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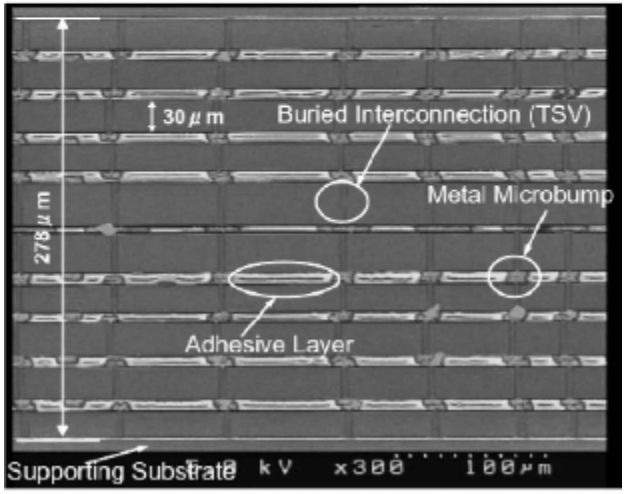


(b)

From Koyanagi et al., IEEE Proceedings, Feb 2009

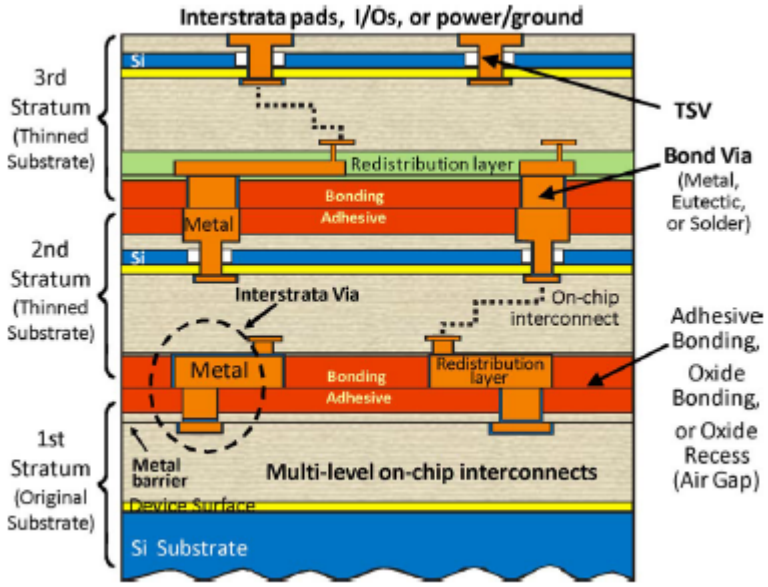
Issues

- **3D Infrastructure & supply chain**
- **I/O Standardization**
- **EMI**
- **Thermal management and reliability**

TSV Pitch

TSV Pitch ≠ Area / Number of TSVs

- TSV pitch example
  - 1024 bit busses require a lot of space with larger TSVs
  - They connect to the heart and most dense area of processing elements
  - The 45nm bus pitch is ~100 nm; TSV pitch is > 100x greater



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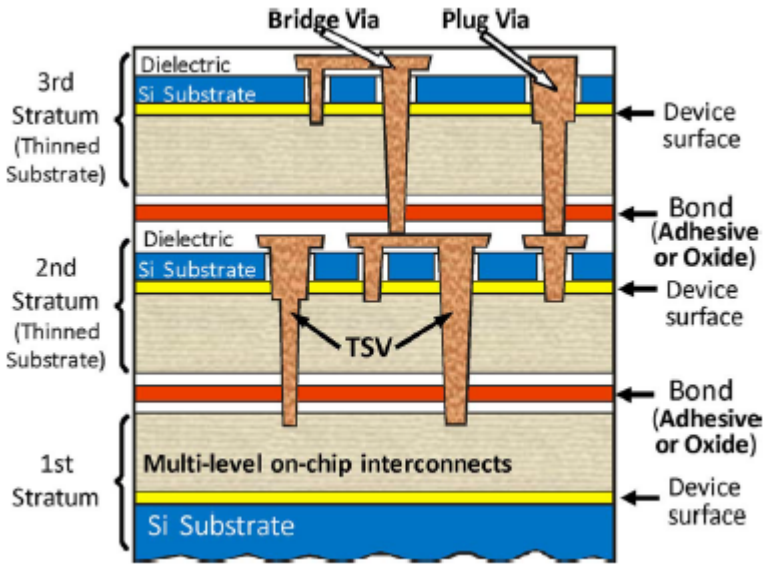
Through-Silicon Vias (TSV)

- Via First
- Via Last
- Via at Front End (FEOL)
- Via at Mid line
- Via at Back end (BEOL)



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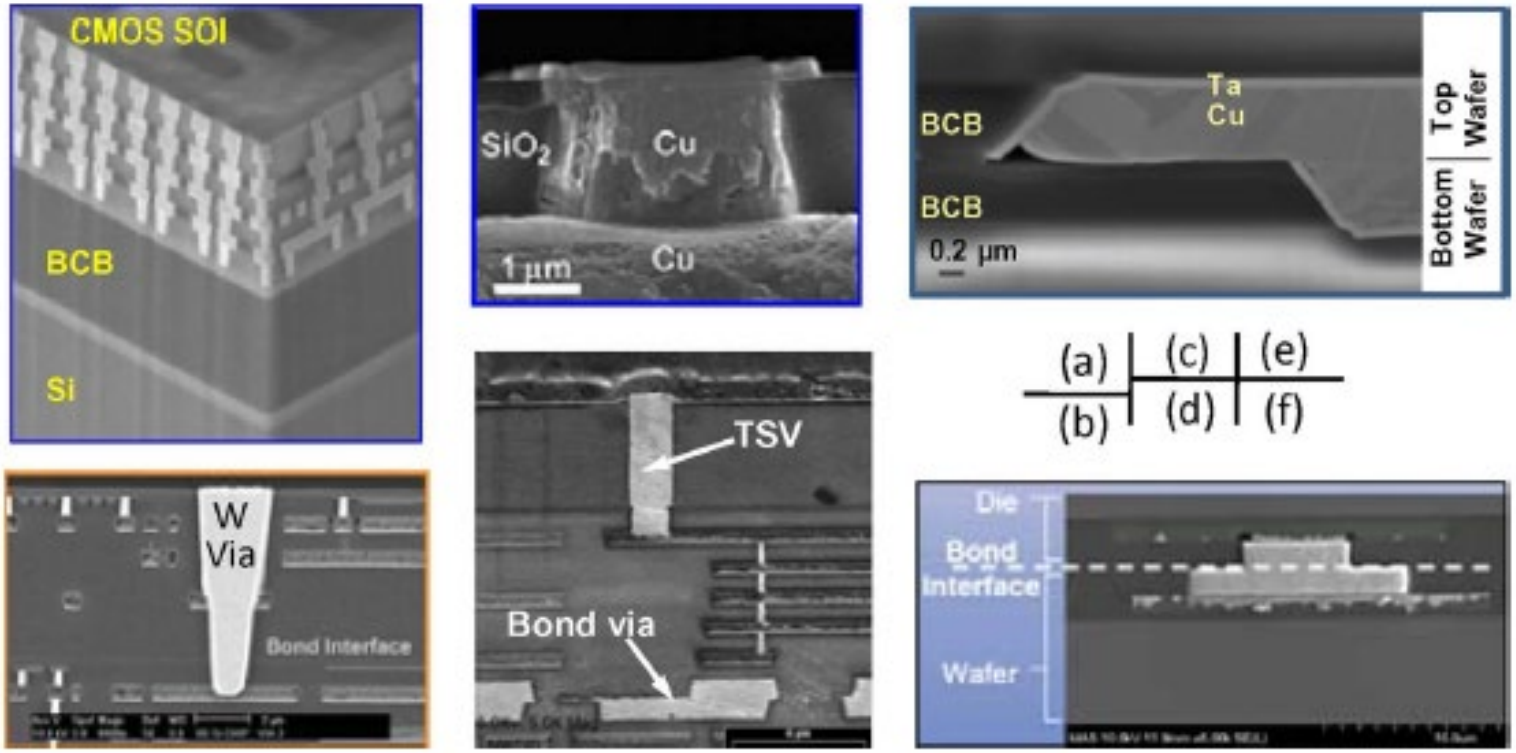
Through-Silicon Vias (TSV)



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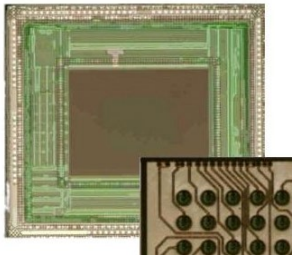
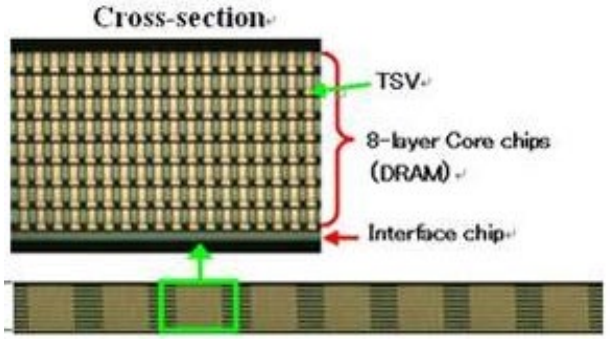
TSV-Based Products



STMicro CMOS image sensor in WLP/TSV package

Sony Video / DSC camera with BSI CMOS image sensors



Elpida's 3D TSV stacked DRAM memory

There are currently about 15 different 3D-IC pilot lines worldwide

3D-IC and TSV

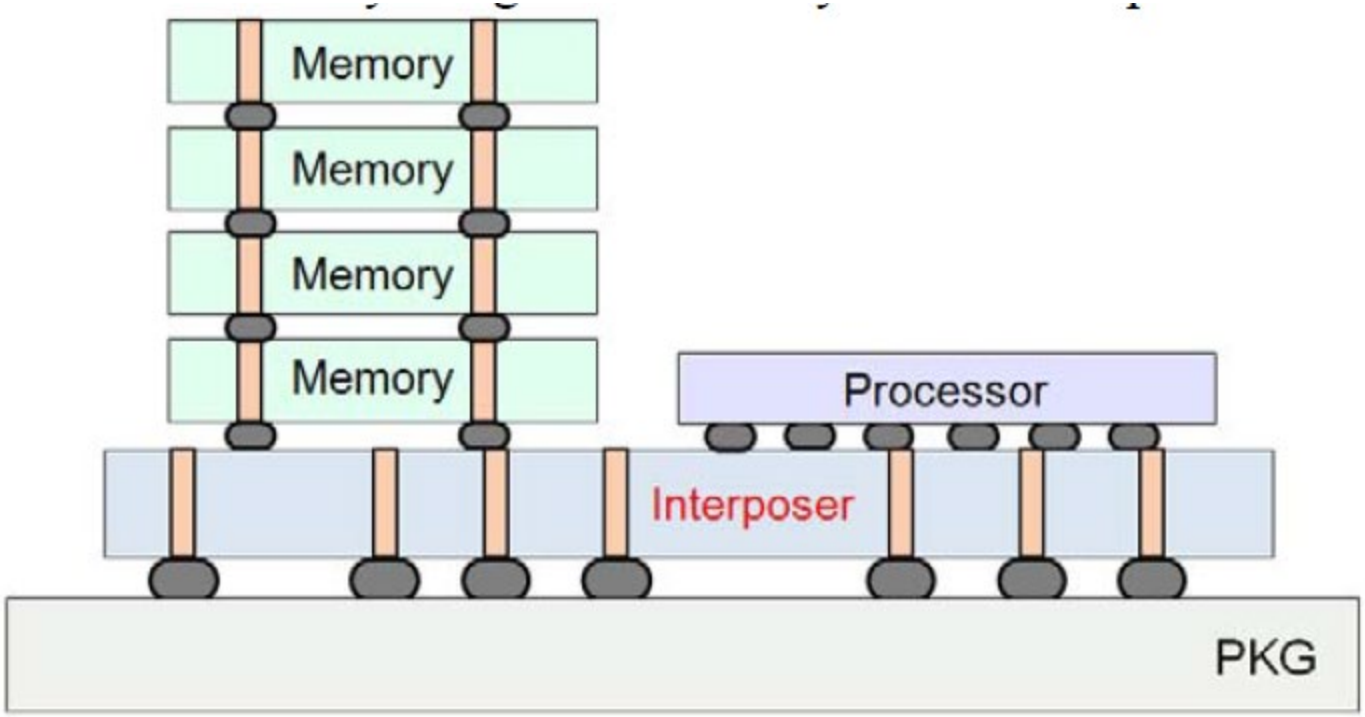
- Stacking of chips makes heat transfer through the z-direction difficult.
- Lossy silicon substrate makes coupling between adjacent TSVs strong.
- TSV noise can be easily coupled to the adjacent TSV through conductive silicon substrate
- 3D IC yields are much lower than 2D-IC
- Difficult to detect TSV and MOS failures

Solution: Use 2.5D integration

2.5D Integration

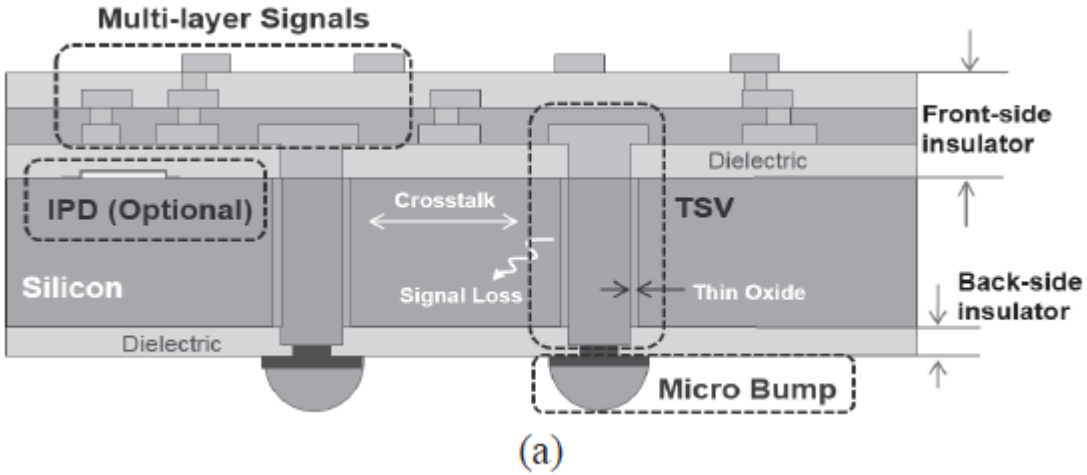
- 2.5D-IC emerges as a temporary solution
- In 2.5D-IC, several chips are stacked on interposer only homogeneous chip stacking is used.
- fine-pitch metal routing is necessary because it increase I/O counts
- For this purpose, an interposer is used where small width and small space metal routing is possible.
- Silicon substrate is usually used for an interposer because on-silicon metallization process is mature and fine-pitch metal routing is possible

Silicon Interposers



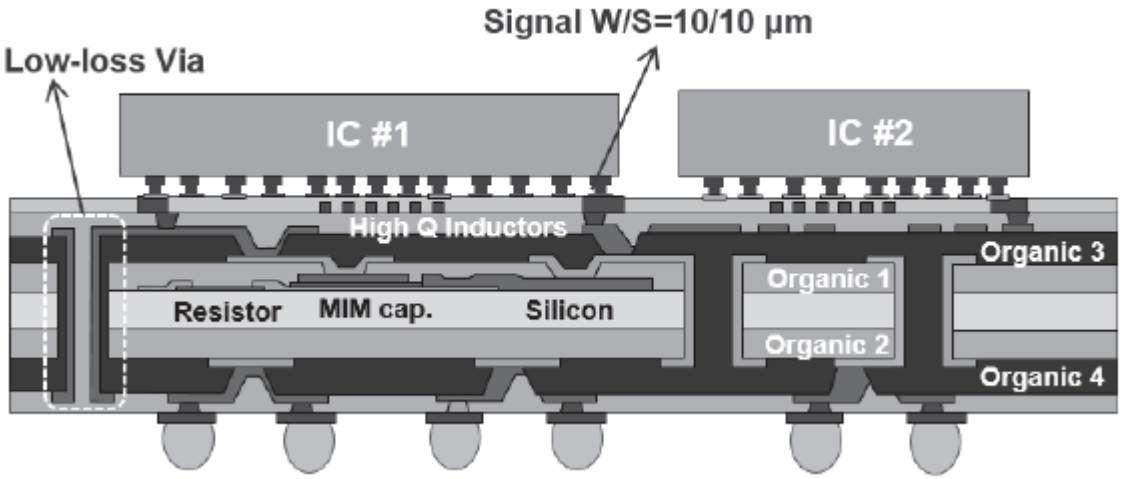
Source: J. Kim et al – DesignCon 2013.

Silicon Interposers



Source: Jong-Min Yook, Dong-Su Kim, and Jun-Chul Kim, "Double-sided Si-Interposer with Embedded Thin Film Devices", 2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013), pp 757-760.

Silicon Interposers



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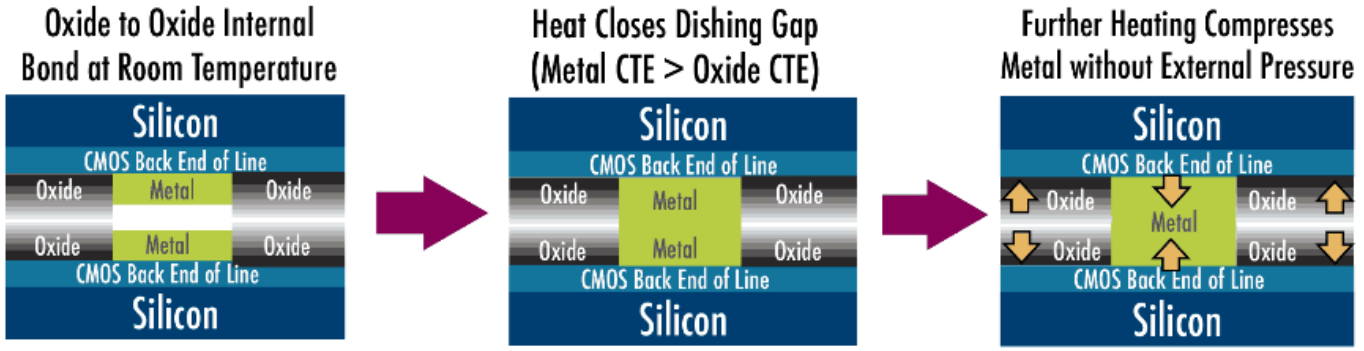
Hybrid Bonding

simultaneous bonding of dielectric and metal bond pads in one bonding step



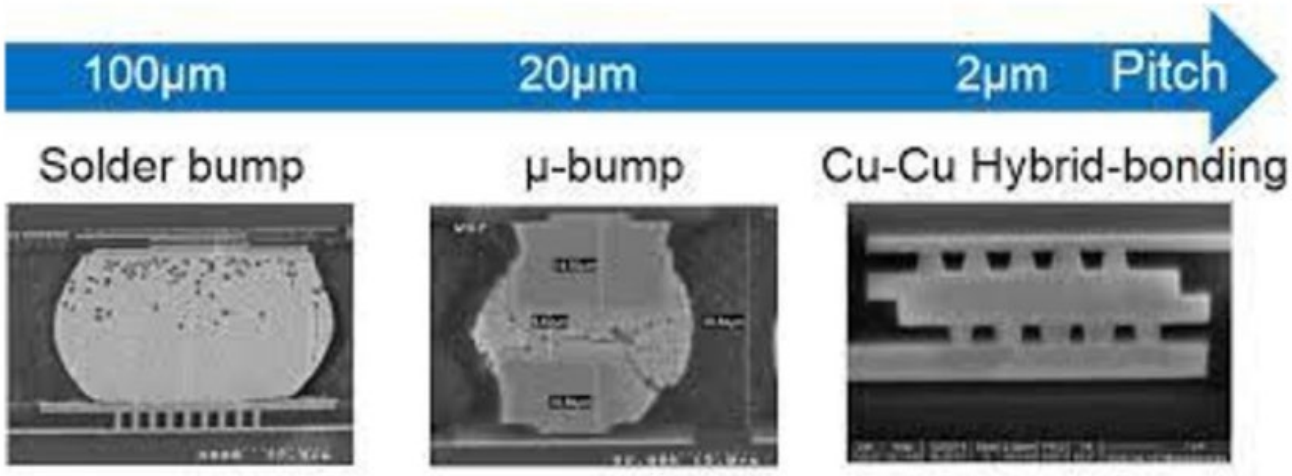


Image Credit: Imed Jani. Test and characterization of 3D high-density interconnects. Micro and Nanotechnolo- gies/Microelectronics. Université Grenoble Alpes, 2019. English. NNT : 2019GREAT094 . tel- 02634259

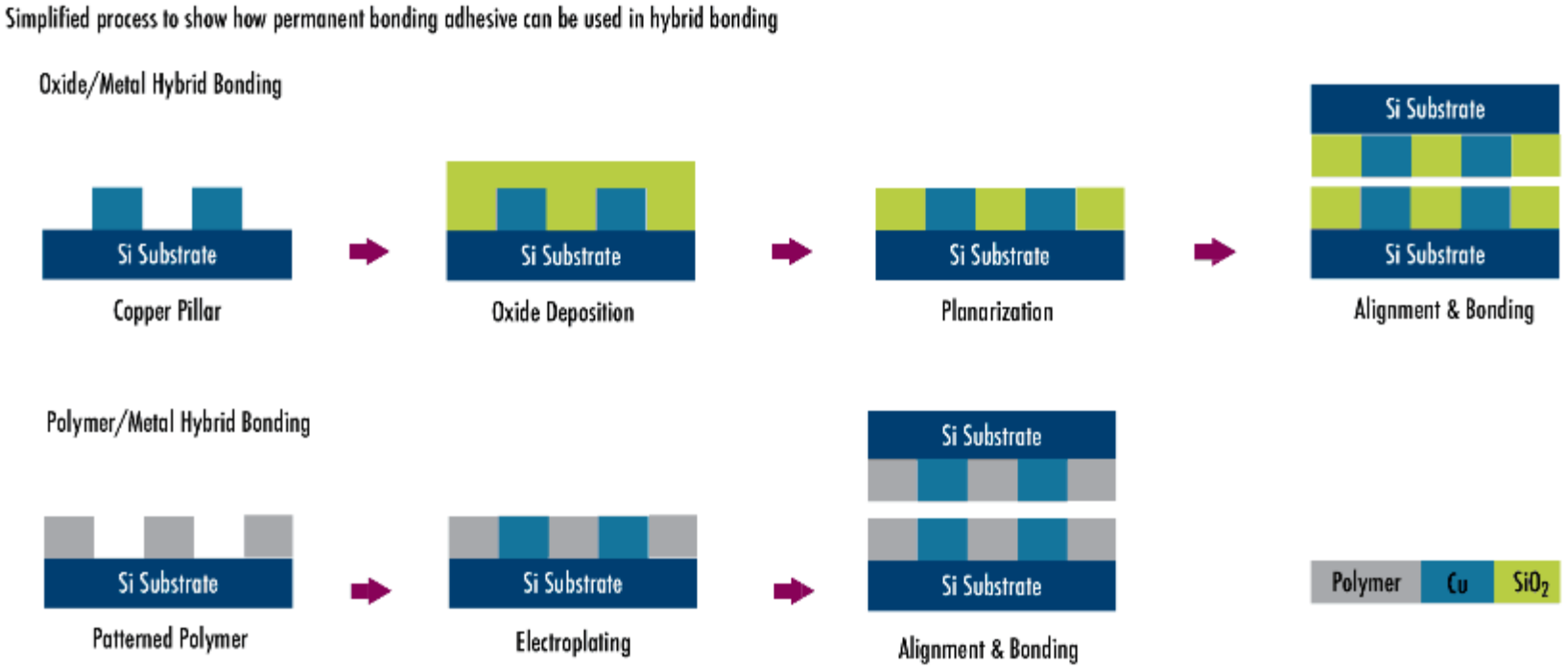
Hybrid Bonding

Advantages

- Allows advanced 3D device stacking
- Highest I/O
- Enables sub-10-μm bonding pitch
- Higher memory density
- Expanded bandwidth
- Increased power
- Improved speed efficiency
- Eliminates the need for bumps, improving performance with no power or signal penalties

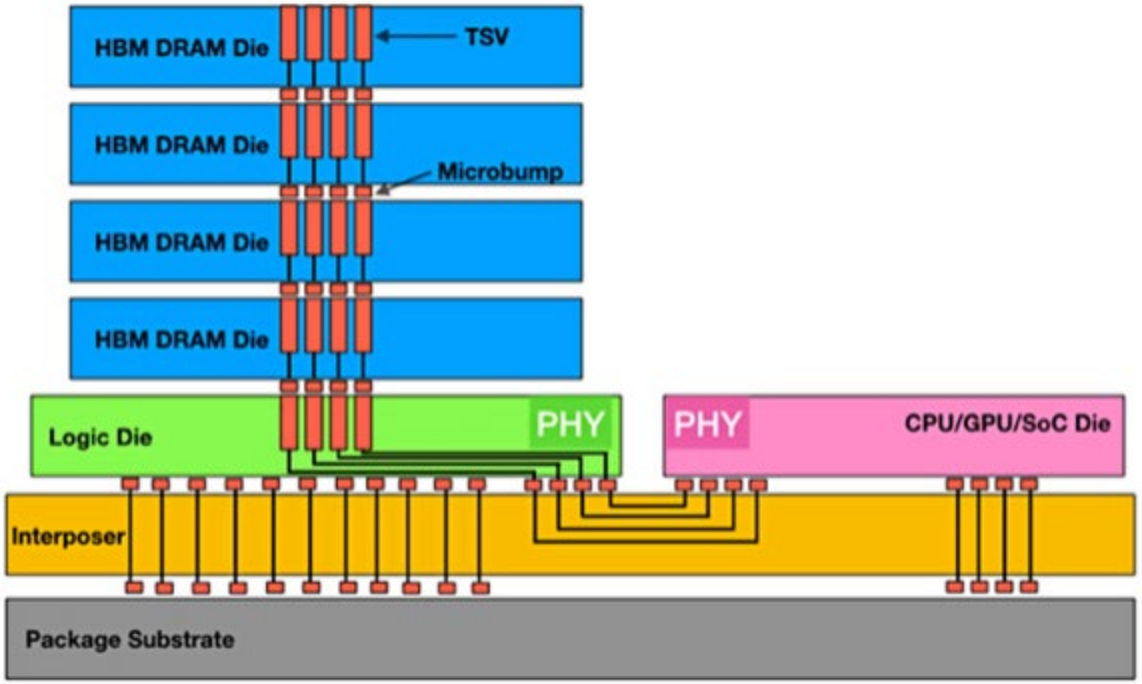
Hybrid Bonding

Processing Steps



Hybrid Bonding

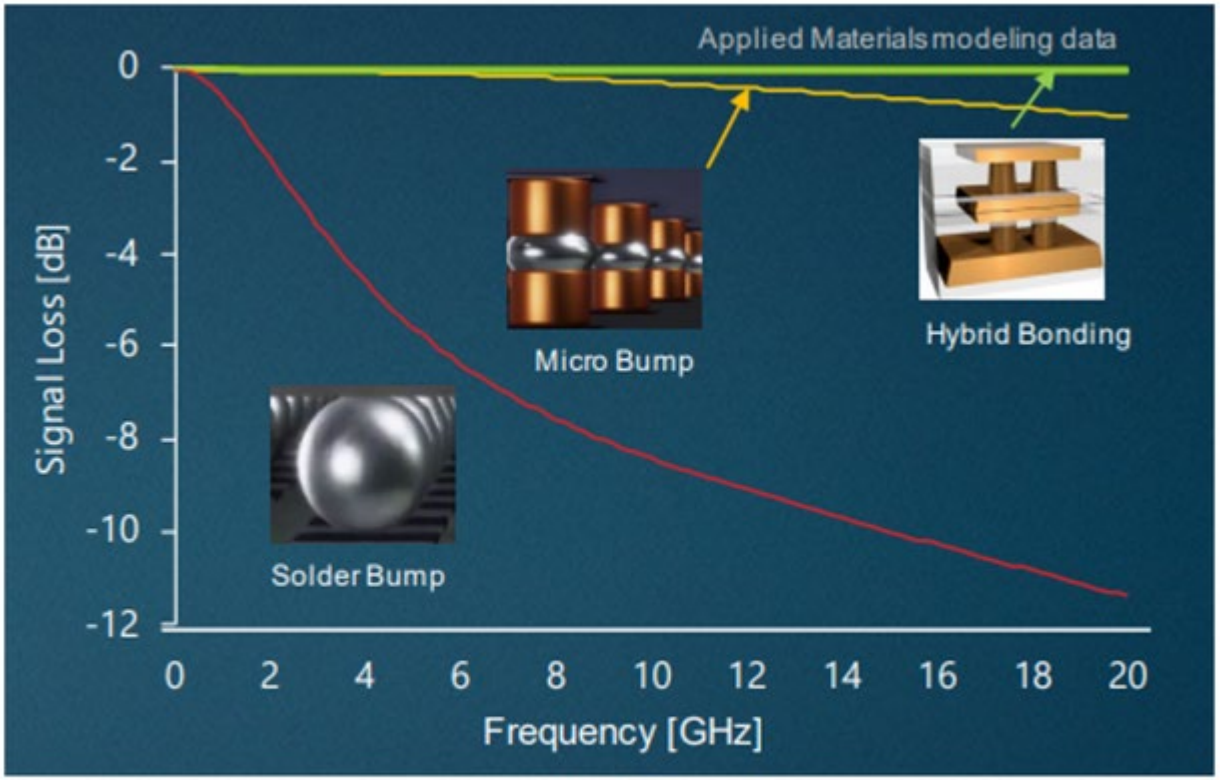
Applications



HBM stack for maximum data throughput. Source: Rambus

Hybrid Bonding

Comparison

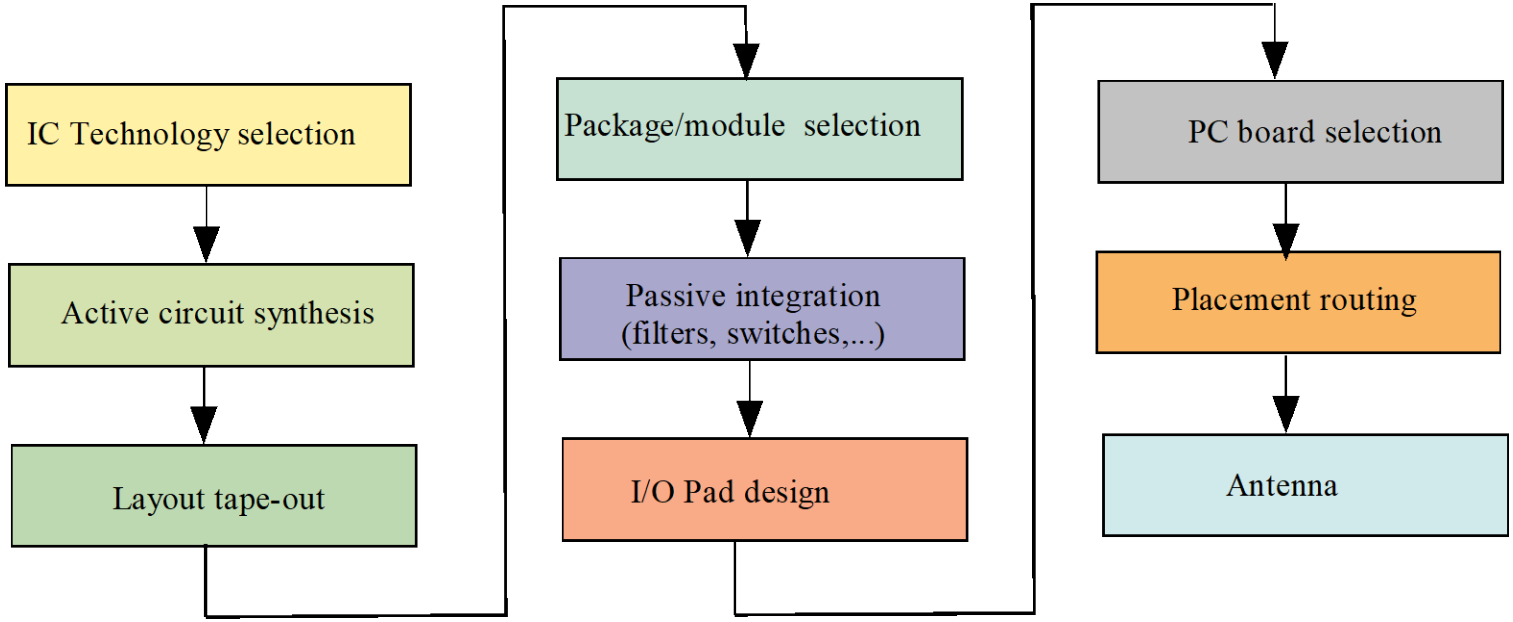


Hybrid bonding virtually eliminates signal loss. Source: Applied Materials

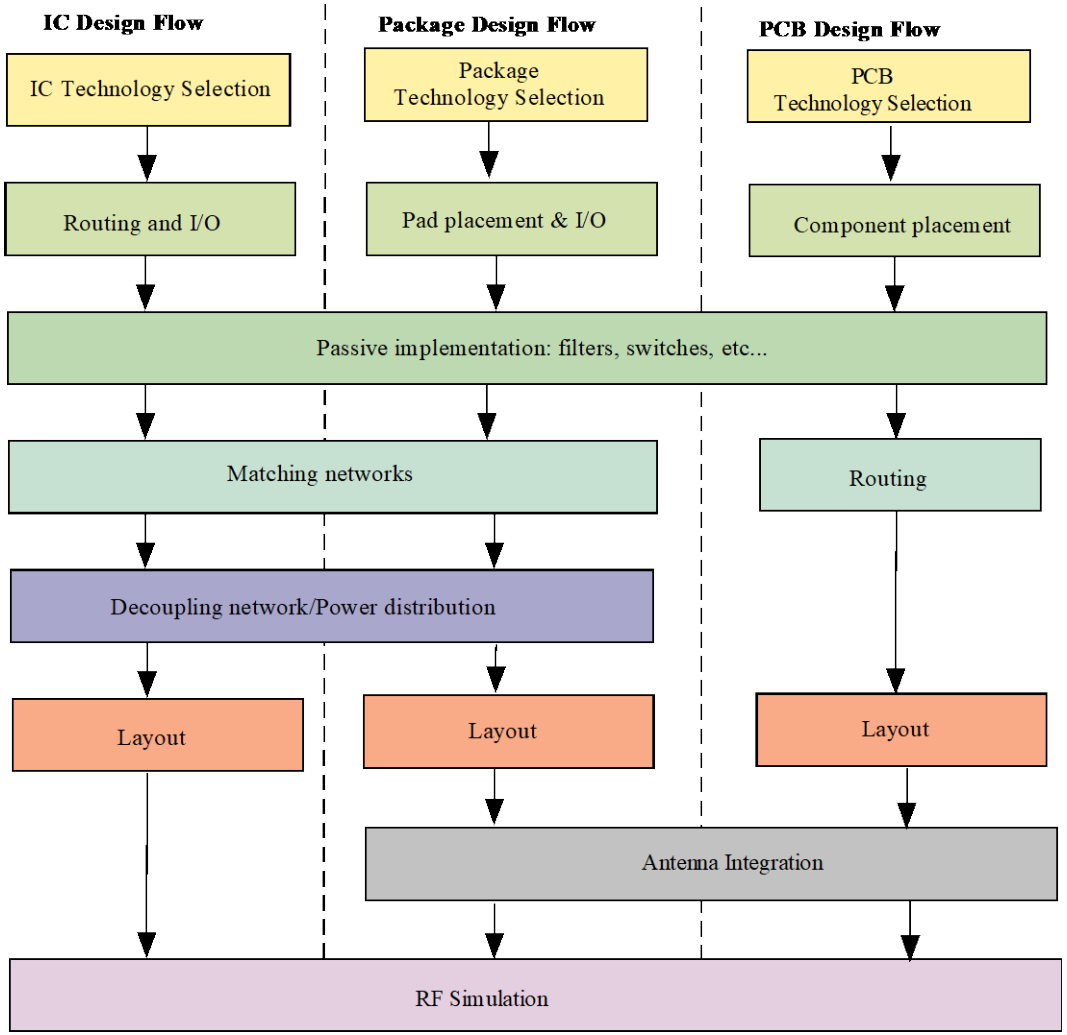
What is Co-Design?

- Level Co-design
  - Chip
  - Package
  - Board
- Function-based Co-design
  - Thermal aware
  - Signal integrity aware
  - Testability
  - Security aware
- Physics-based Co-design
  - Thermal
  - Electrical
  - Mechanical
  - Optical
- Domain-based Co-design
  - Hardware
  - Software
  - Architecture

Traditional Design Flow

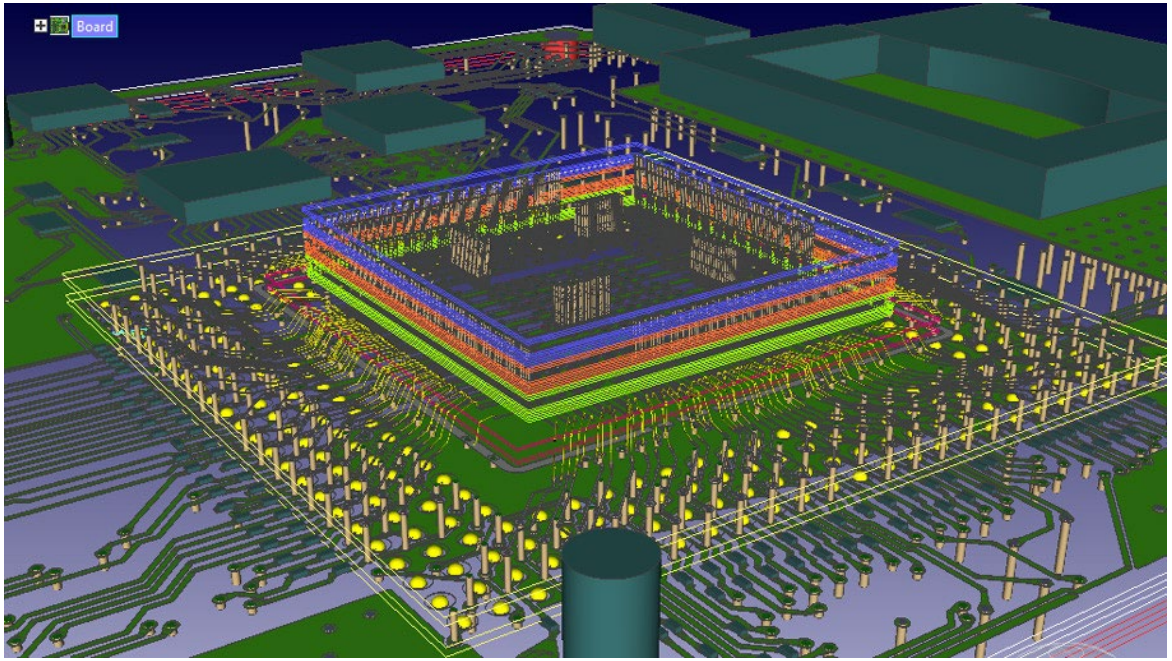


Co-Design Flow



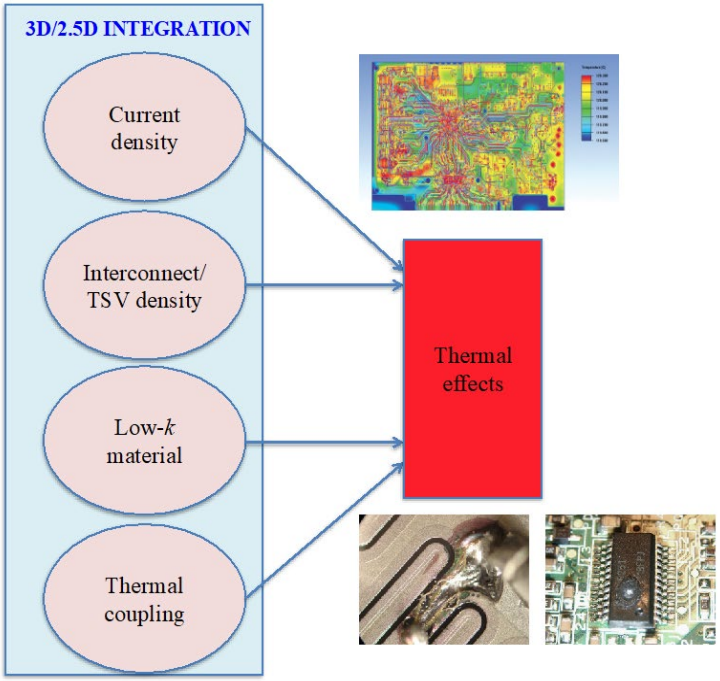
Co-Design Requirements

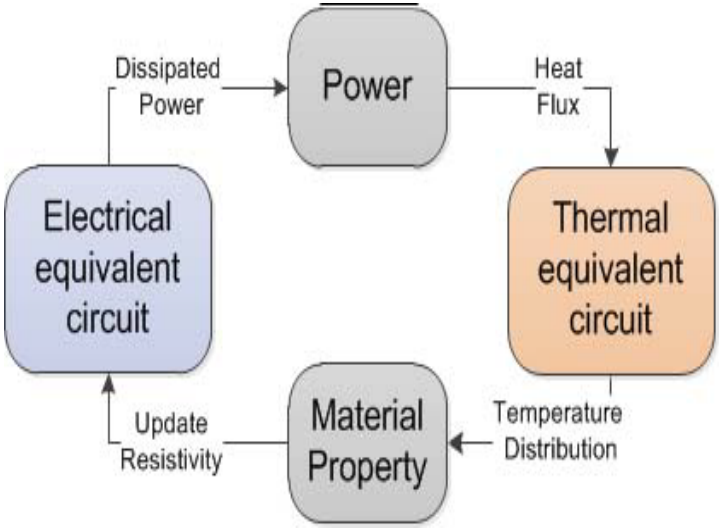
- Tradeoffs in advance
- Translation and domains
- Propagate information
- Manage connectivity
- Database formats



Courtesy of Zuken

Thermal-Aware Co-Design

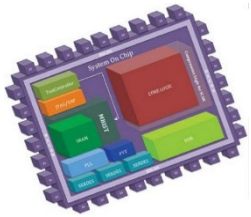


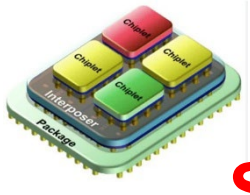


Multi-Chiplet Challenge

- Objectives
  - 1000 chiplets on panel
  - New layer of abstraction needed
  - Abundance of wires (~6000/mm)
- Challenges
  - Logic connectivity vs physical connectivity
  - Fragmented design ecosystem
  - Increased design complexity

SOC

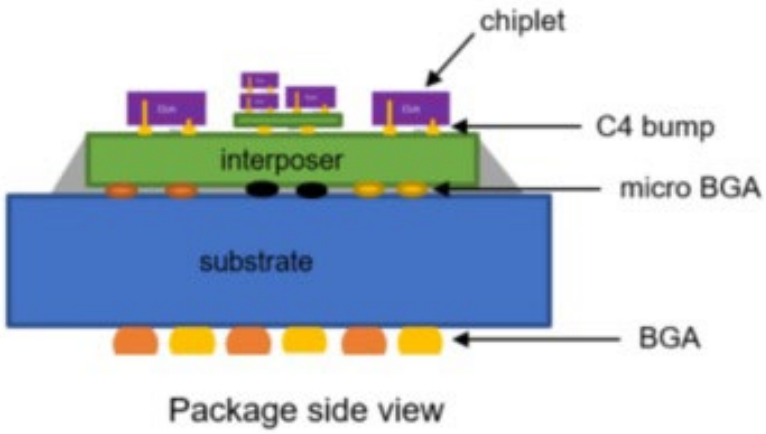




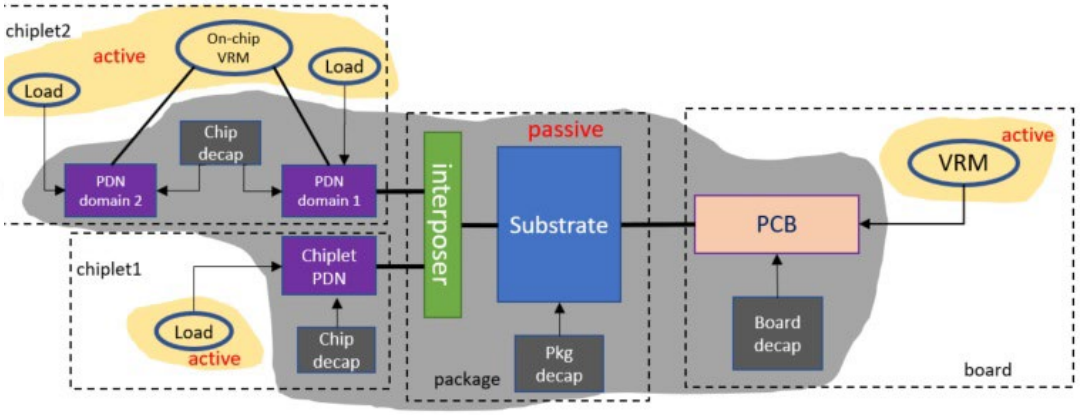
SiP

Power Delivery for Chiplet-Based SiP

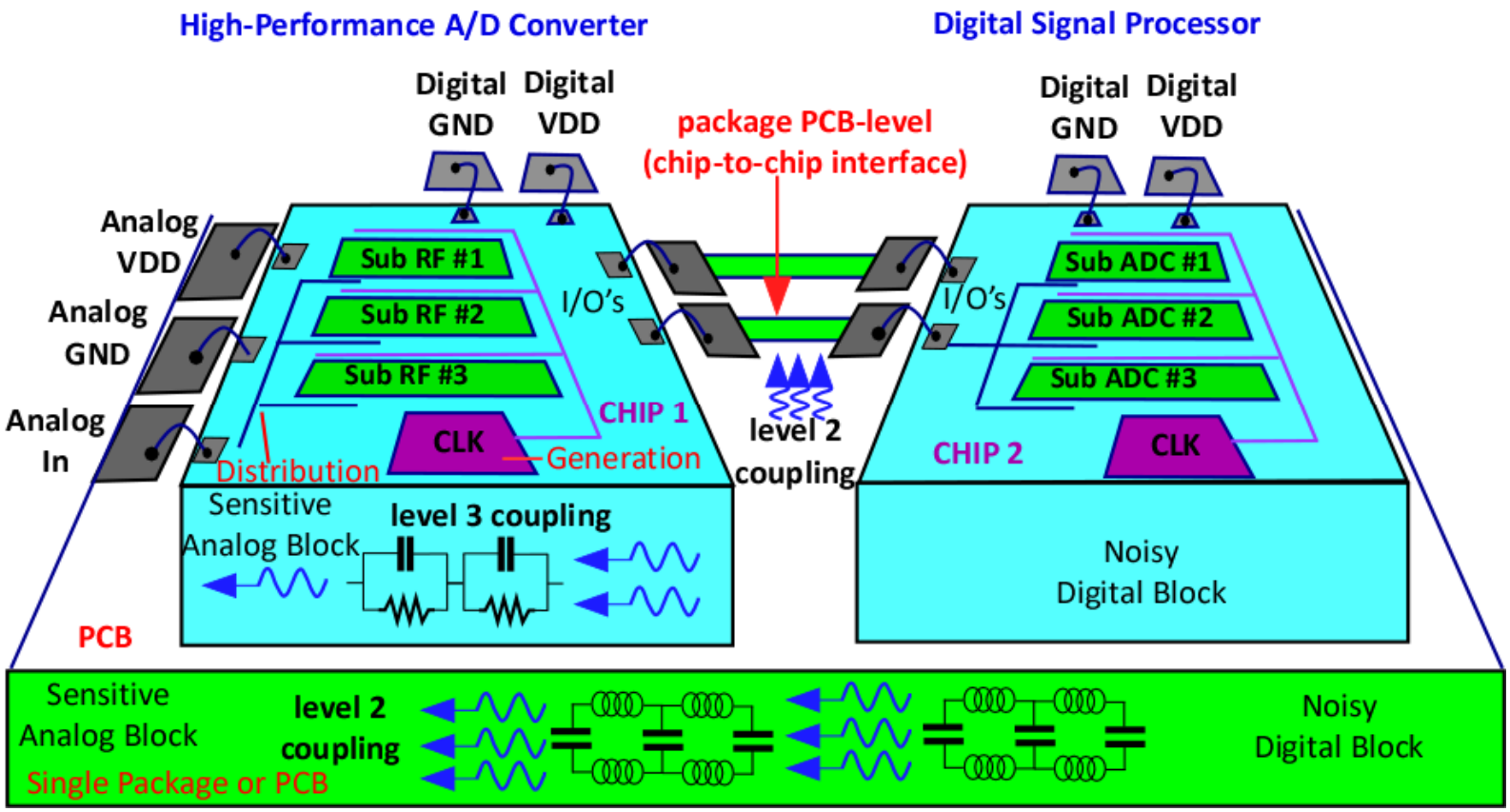
Chiplets must be positioned in their respective locations and provided with paths through the power distribution network. There can be multiple power domains. Package builder tools are used to automate the placement of vias, ball grid arrays and traces to the PDN. To mitigate supply voltage fluctuations decoupling capacitors (“decaps”) are placed on the PCB, package substrate, package interposer, and the silicon dies.



Package side view



Coupling Noise in Mixed Signal Systems

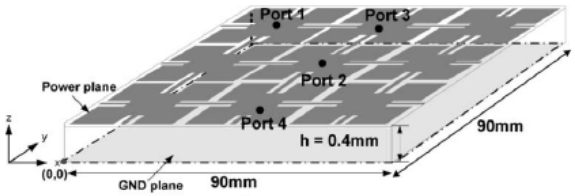


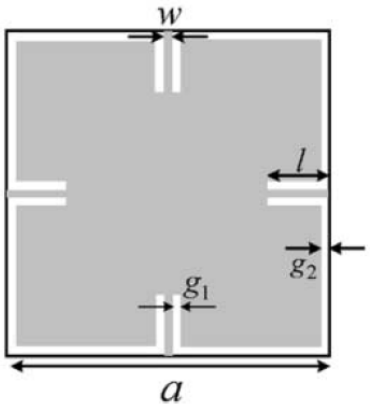
Proposed Solution

- Electromagnetic Bandgap (EBG) Structures
  - Definition: One-, Two- or Three-Dimensional Periodic Metallic/Dielectric System which Exhibits Band Rejection Behavior
  - Bandstop filter characteristics due to shunt capacitances and series inductance
  - Design can be optimized for PDN applications

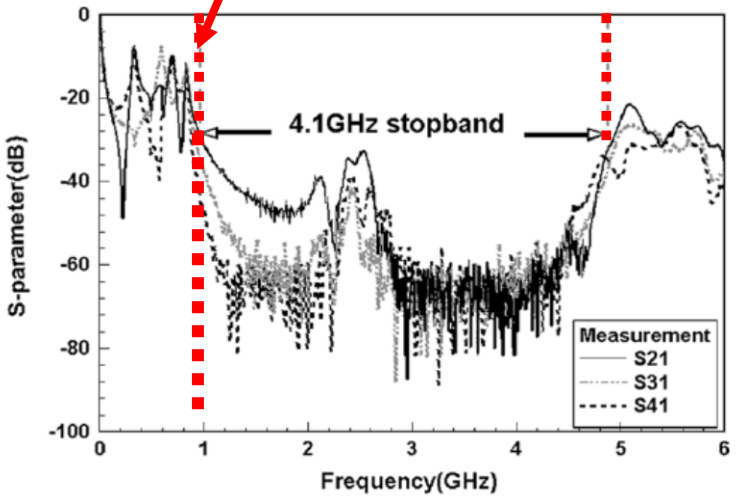
Electromagnetic Bandgap Structures (EBG)

IEEE MWCL July 2004

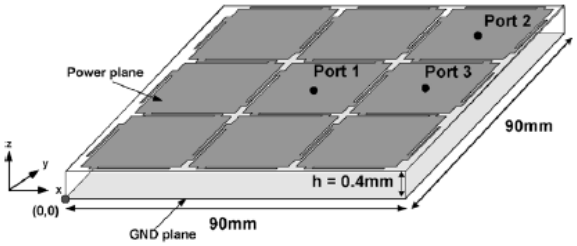


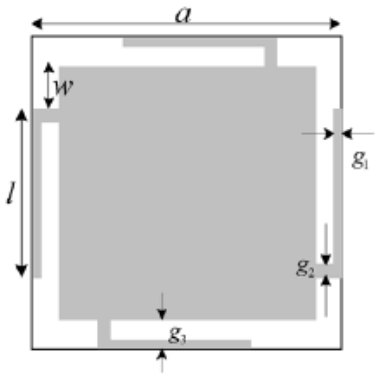


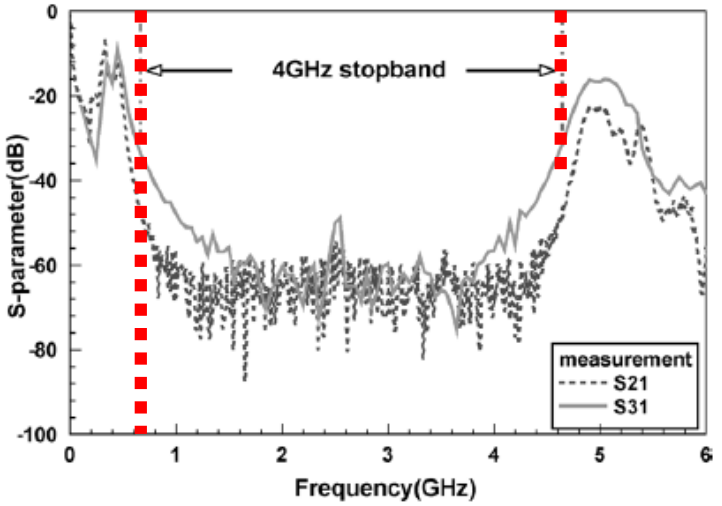
LPF: C_P and L_{bridge}



IEEE MWCL Mar. 2005

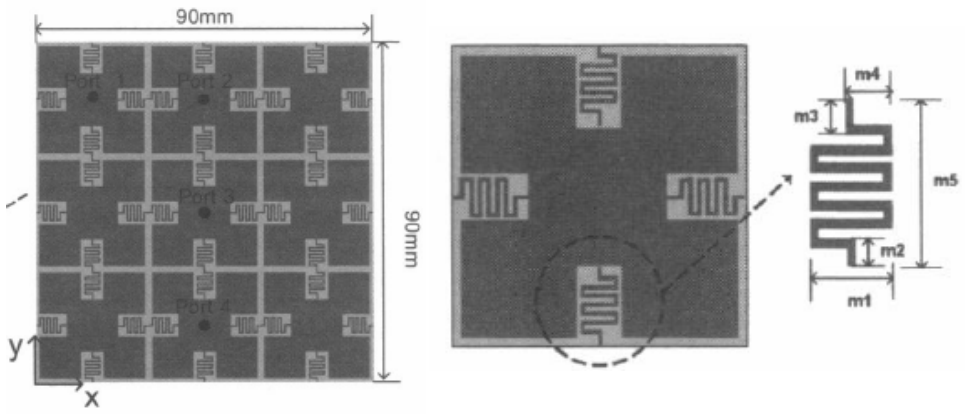


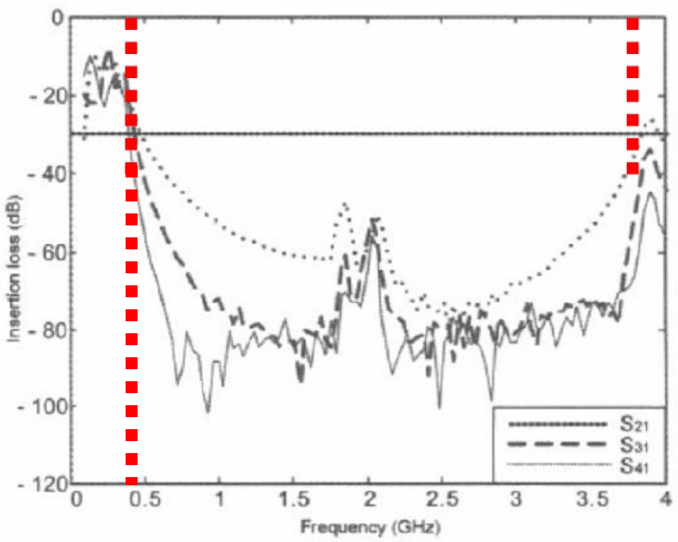




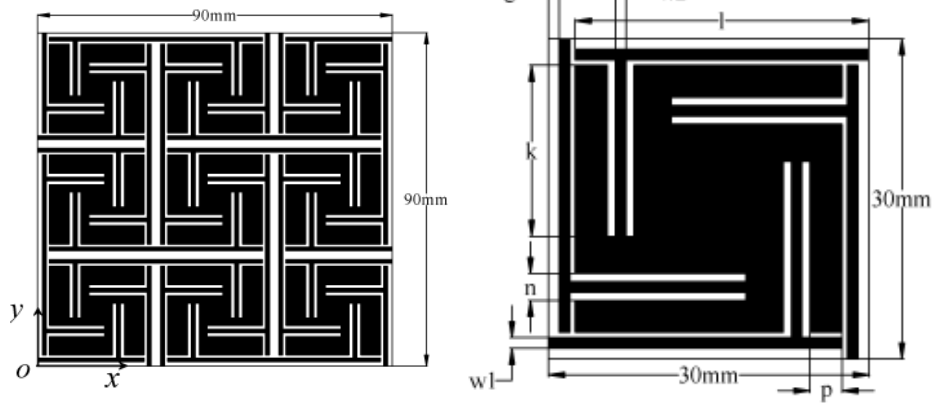
Planar-type EBG Structures

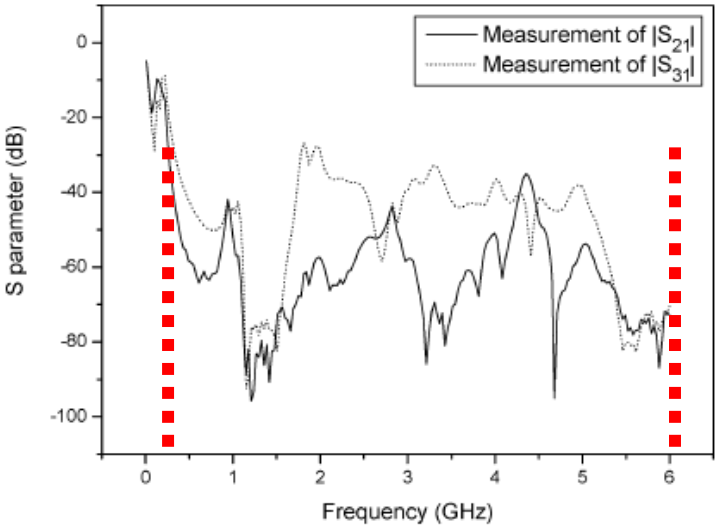
IEEE APS July 2005





IEEE MWCL Mar. 2006

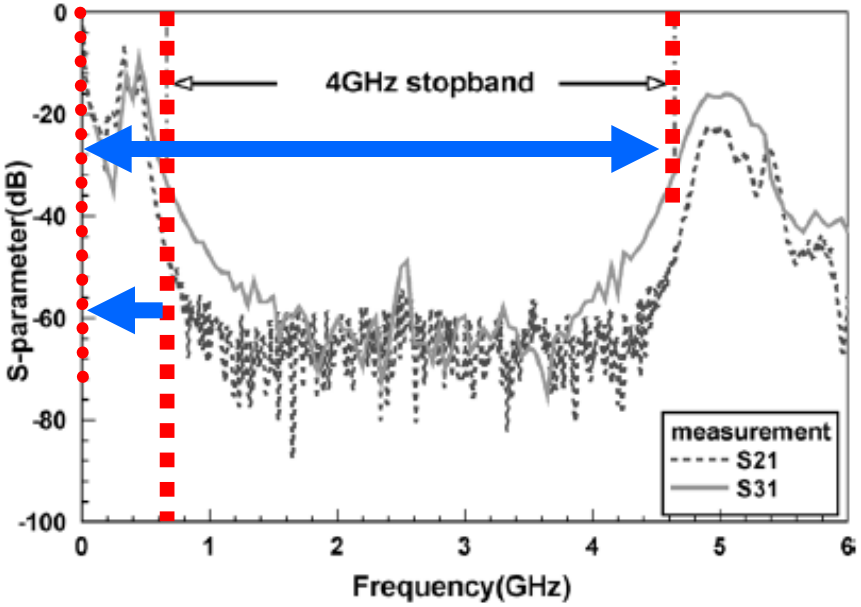


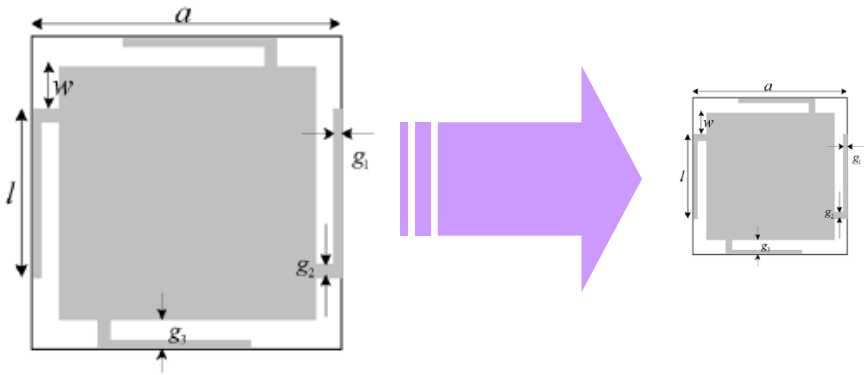


EBG Structure

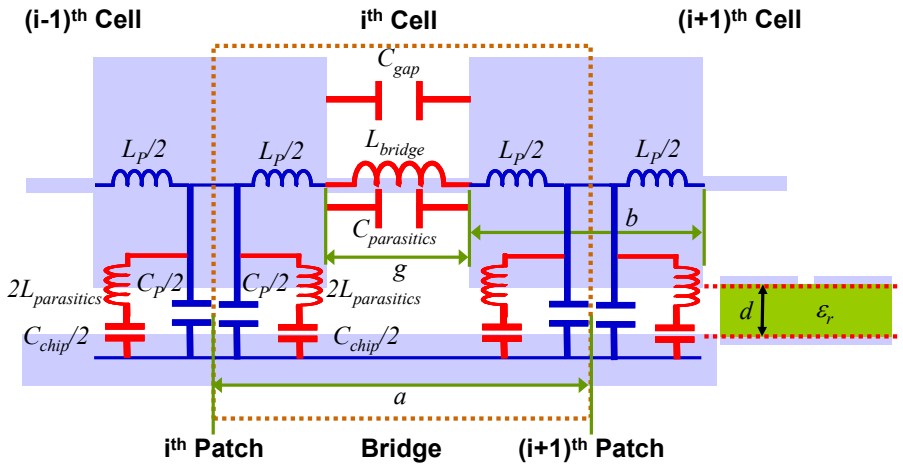
1. Reducing Cut-off Frequency of Planar-type EBG Structure
   - (In Consequence) Enhancing Noise Suppression Bandwidth

2. Miniaturizing Unit Cell of Planar-type EBG Structure
   - Without Degradation in Stopband Bandwidth



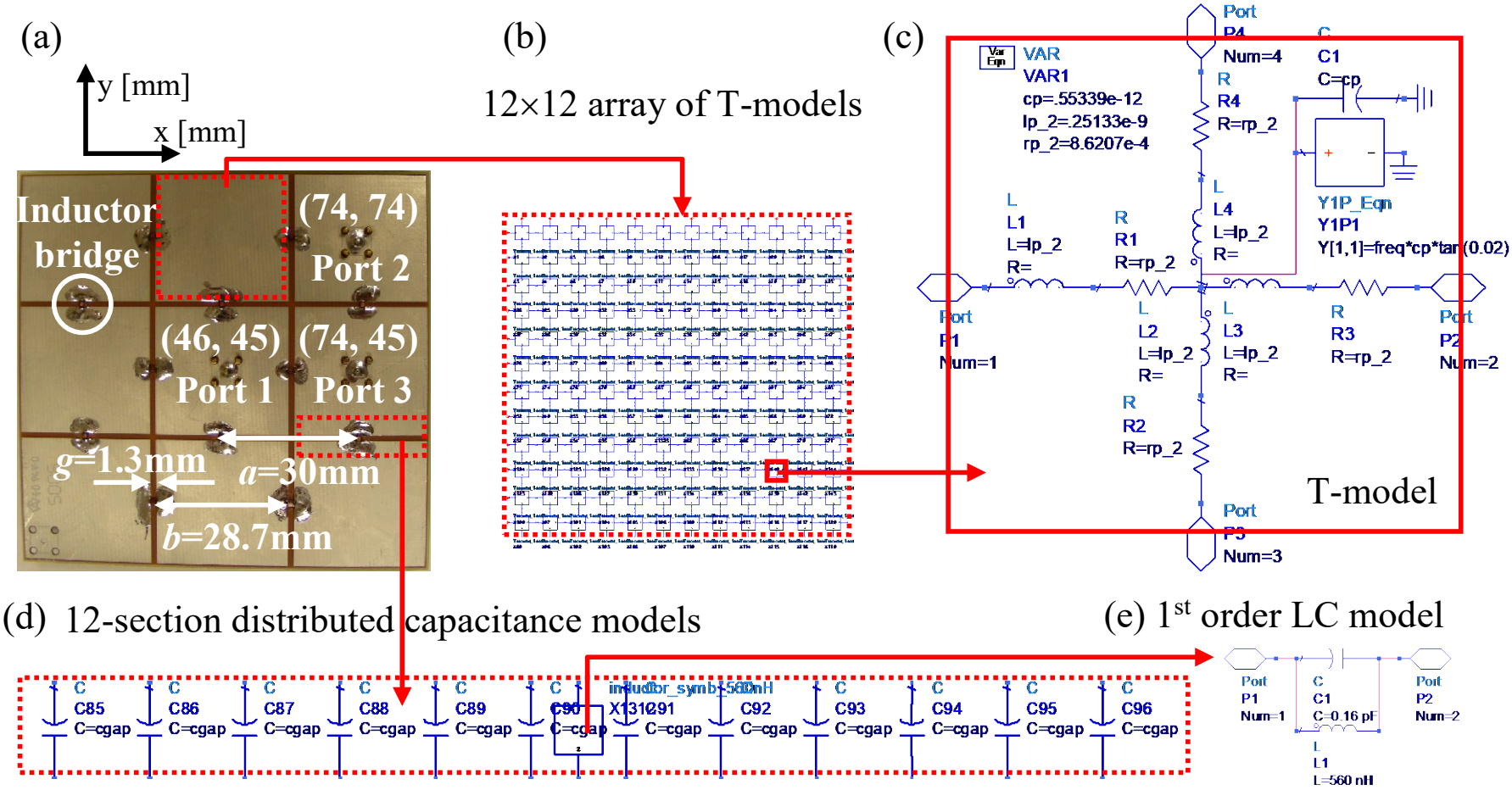


EBG Structure



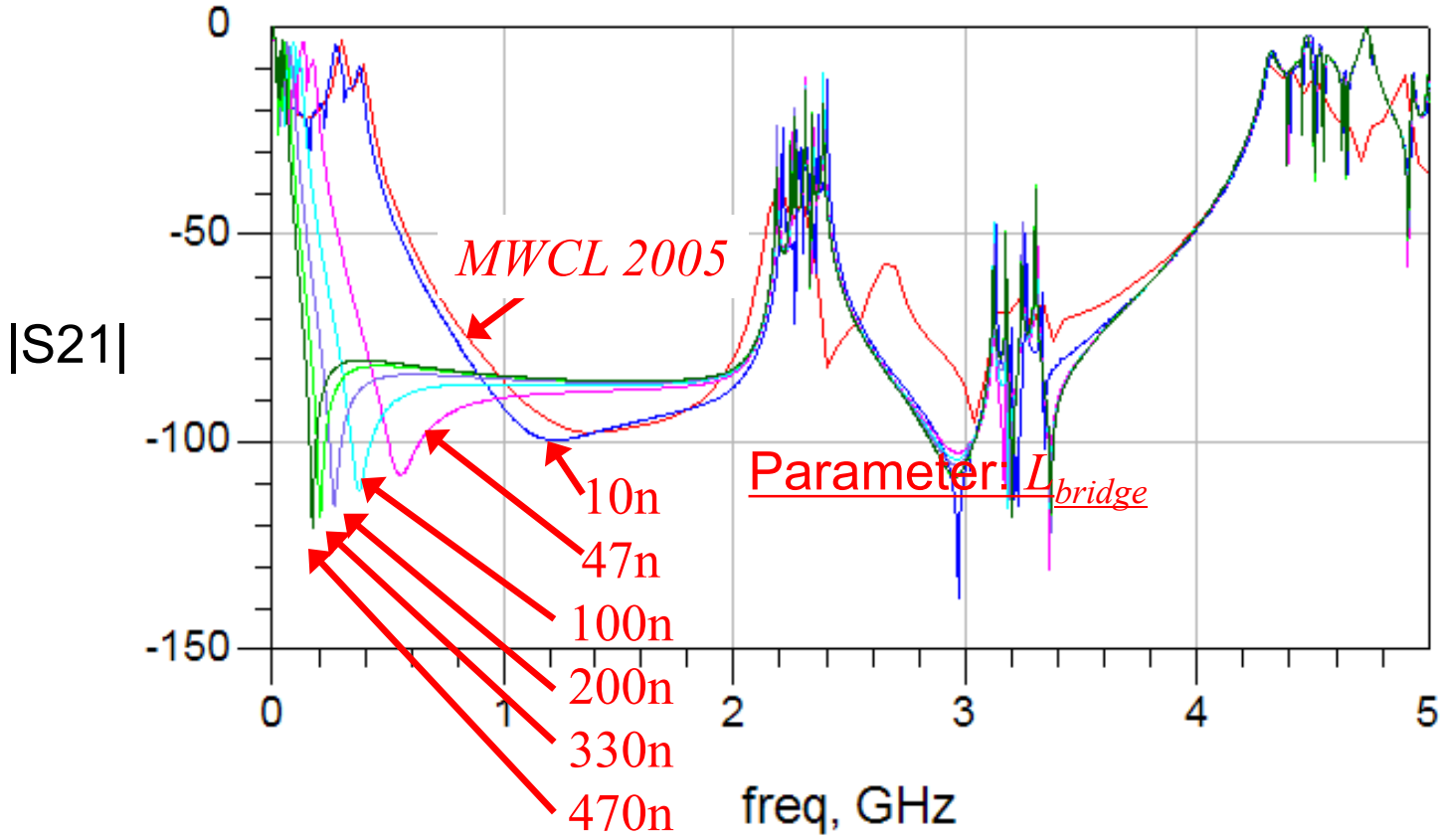
Methods of Cut-off Frequency Enhancements	Dominant Circuit Level Components in Fig.	Cut-off Frequency ($f_{lowpass\_cutoff}$) [MHz]	High Frequency Limitation of EBG Structure
Method 1: Conventional Planar-type EBG Structure	L_P, L_{bridge} (=L_{MSL}), and C_P	$\left[\pi\sqrt{C_P\left(L_P+L_{MSL}\right)}\right]^{-1}$	1st Resonant Frequency of Patch at $c/\left(2b\sqrt{\varepsilon_r}\right)$
Method 2: Increasing Bridge Inductance using Series Lumped Chip Inductors	L_P, L_{bridge} (=L_{chip}), and C_P	$\left[\pi\sqrt{C_P\left(L_P+L_{chip}\right)}\right]^{-1}$	1st Resonant Frequency of Patch at $c/\left(2b\sqrt{\varepsilon_r}\right)$
Method 3: Increasing Patch Capacitance using Shunt Lumped Chip Capacitors	L_P, L_{bridge}, $L_{parasitics}$, C_P, and C_{chip}	$\left[\pi\sqrt{C_P'\left(L_P+L_{bridge}\right)}\right]^{-1}$	Parallel Resonant Frequency of C_P and $L_{parasitics}$ at $1/\left(2\pi\sqrt{C_P L_{parasitics}}\right)$

Verification: ADS Simulation



Simulation Results

– EBG Structure with 90x90 mm^2 Ground Plane Area



Thermal Management

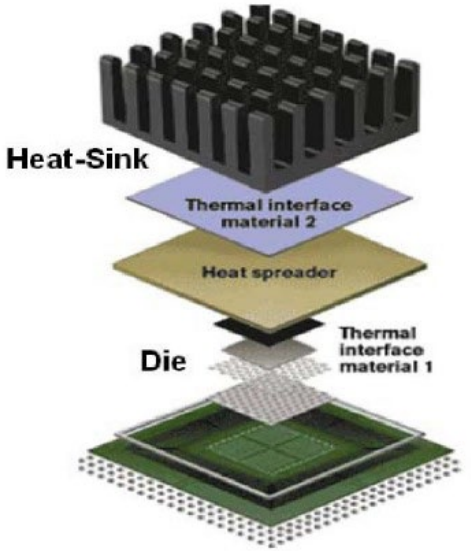
Manage heat within a system to ensure efficient and safe operation.

Thermal Management Techniques

- Air Cooling, Liquid Cooling, and Two Phase Cooling
- Conduction Cooling

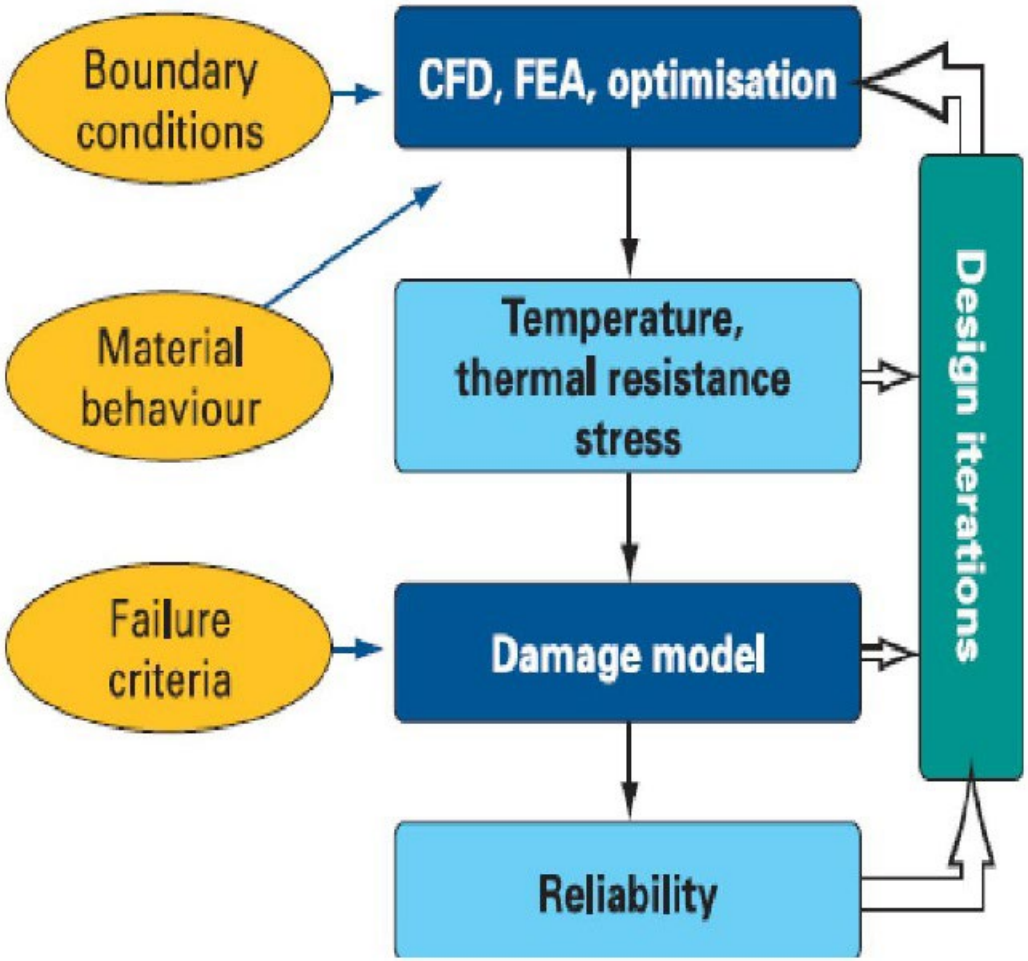
Passive Cooling Technology

- Thermal Interface Materials
- Heat Spreaders
- Heat Sinks



Source: C.Bailey, "Thermal Management Technologies for Electronic Packaging: Current Capabilities and Future Challenges for Modelling Tools", 2008 10th Electronics Packaging Technology Conference, 2008.

Thermal Management



*C.Bailey, "Thermal Management Technologies for Electronic Packaging: Current Capabilities and Future Challenges for Modelling Tools", 2008 10th Electronics Packaging Technology Conference, 2008.

Thermal Management

*Passive Technology Materials**

Material	Thermal conductivity	CTE 10^{-6}/K	Price/
CVD diamond	>1300	2.0	High
Aluminium Nitride	260	4.0	Medium
Cubic boron nitride	200-250	1	High
Silicon Carbide	200	2.8	Medium
Alumina	30	5	Low
Copper	400	16	Low
Aluminium	200	23	Low
Molybdenum	138	5.1	Low
Copper Molybdenum	165-215	6.8-9.5	Medium
Copper Tungsten	175-235	6.5-9	Medium

*C.Bailey, "Thermal Management Technologies for Electronic Packaging: Current Capabilities and Future Challenges for Modelling Tools", 2008 10th Electronics Packaging Technology Conference, 2008.

Electrical-Thermal AC Analysis

Electrical Analysis:

$$\nabla \times \left(\frac{1}{\mu_r} \nabla \times \mathbf{E} \right) - {k_0}^2 \epsilon_r \mathbf{E} = -j k_0 Z_0 \mathbf{J}$$

- Waveguide port boundary condition
- Absorbing boundary condition

Thermal Analysis:

$$\nabla \cdot k \nabla T = -P$$

$$T = T_c \qquad \text{on } \Gamma_{\text{tc}}$$

$$k \frac{\partial T}{\partial n} = -h(T - T_a) \qquad \text{on } \Gamma_{\text{conv}}$$

Electrical-Thermal DC Analysis

Electrical Analysis:

$$\nabla \cdot \sigma \nabla \phi = 0$$

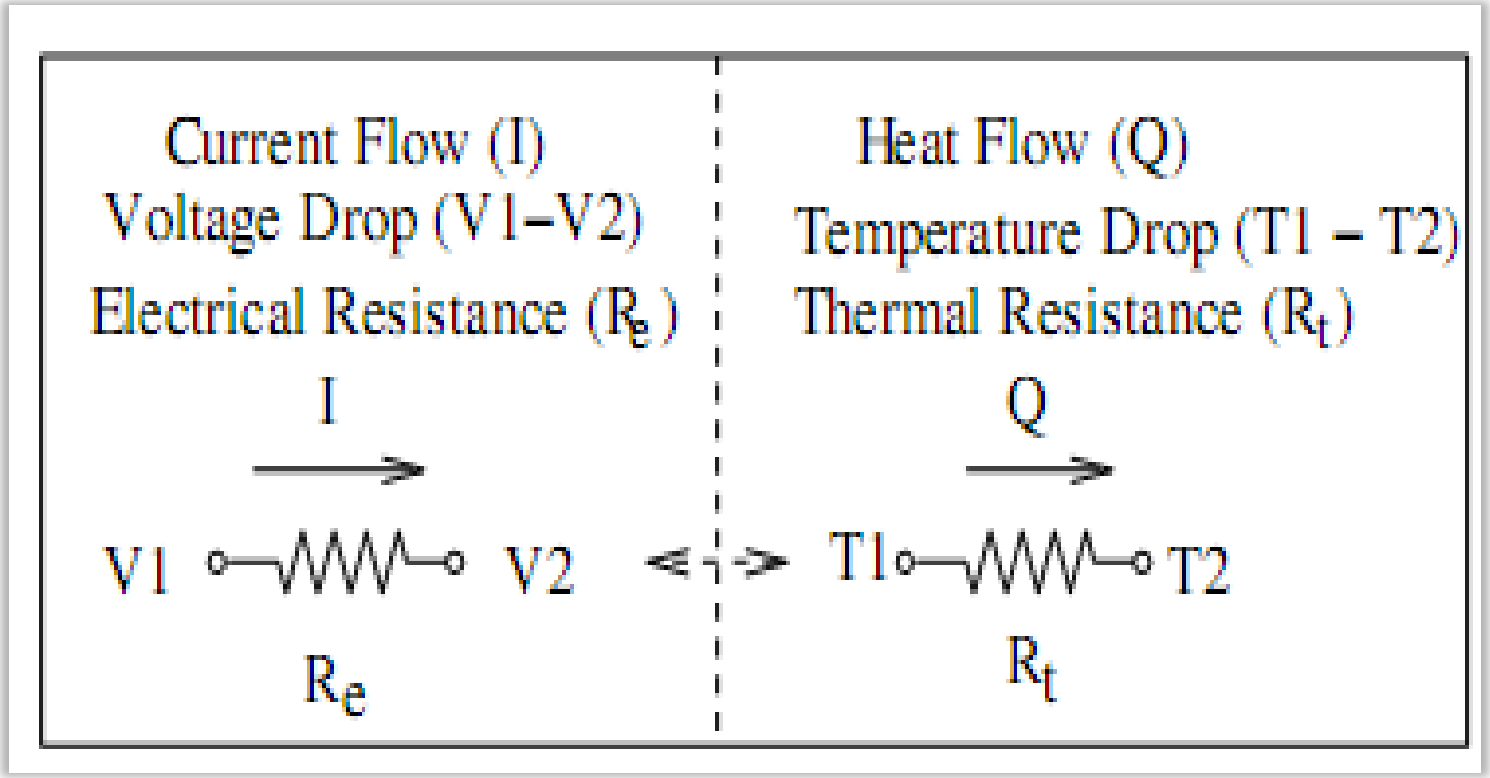
$$\phi = \phi_c \quad \text{on } \Gamma_{\text{vc}}$$
$$\sigma \frac{\partial \phi}{\partial n} = \frac{\phi}{RS} \quad \text{on } \Gamma_{\text{load}}$$

Thermal Analysis:

$$\nabla \cdot k \nabla T = -P$$

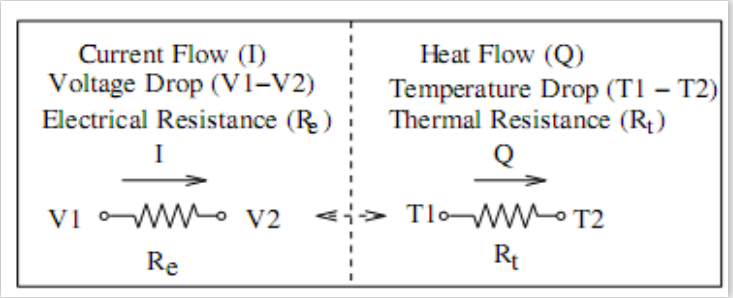
$$T = T_c \quad \text{on } \Gamma_{\text{tc}}$$
$$k \frac{\partial T}{\partial n} = -h(T - T_a) \quad \text{on } \Gamma_{\text{conv}}$$

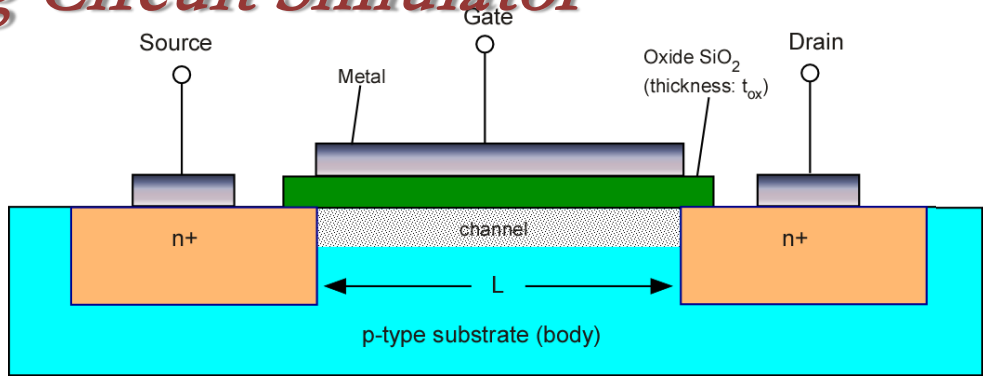
Electrical-Thermal Isomorphism

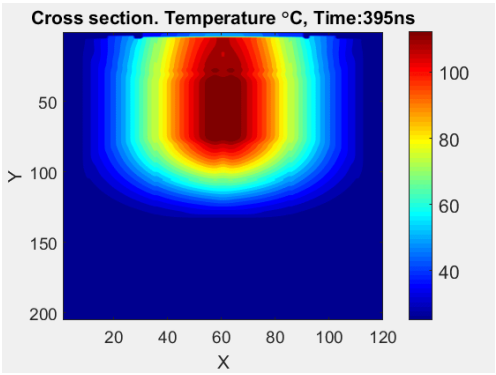


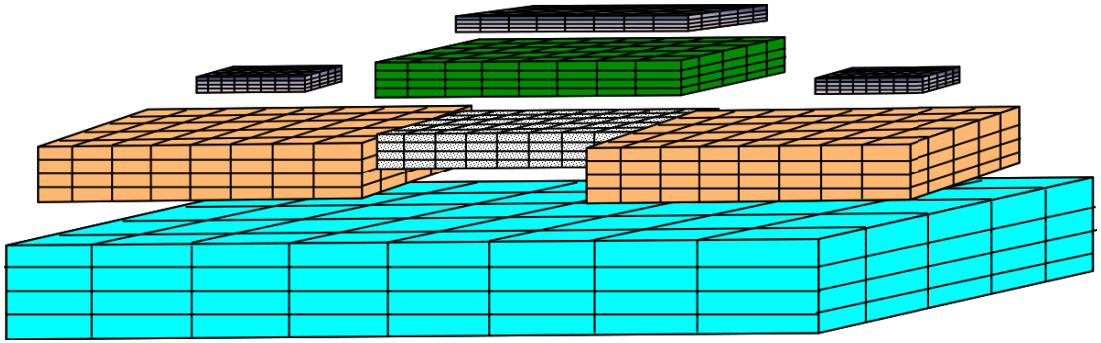
Thermal/Electrical Co-Simulation

*Thermal Modeling Using Circuit Simulator**



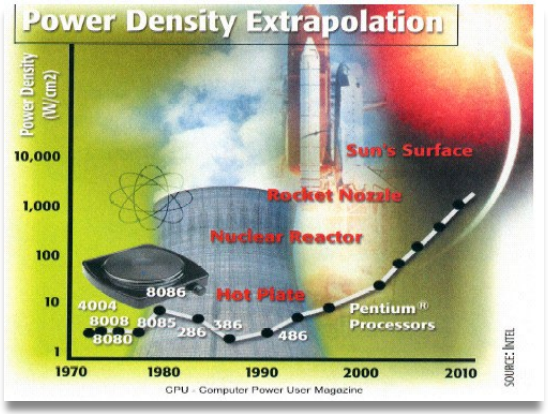


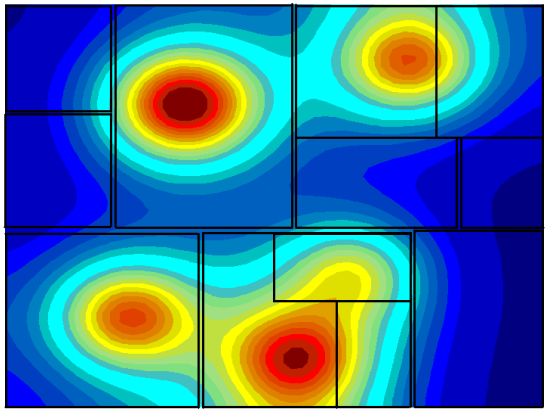




* Klokotov, D., Schutt-Aine, J.E., "Latency Insertion Method (LIM) for Electro-Thermal Analysis of 3-D Integrated Systems at Pre-Layout Design Stages", IEEE Trans. Compon., Packag. Manuf. Technol., vol: 3 , no. 7, pp. 1138-1147, July 2013

Electro-Thermal Analysis. Motivation

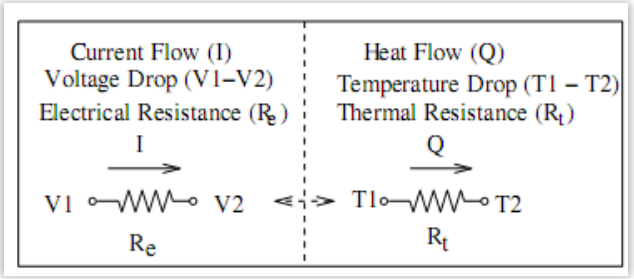




- 3D integration technologies
  - 3D stacked IC designs
  - Increased power density
  - Heat removal difficulties
- Design challenges due to thermal issues
  - Electrical reliability (electro-migration)
  - Power delivery (IR drop)
  - Signal propagation (RC delay)
  - Memory retention time (Leakage)
- Lack of suitable CAD tools
  - Thermal-aware design at the earliest stages
  - Using the floor plan and early power distribution analysis (know the current distribution – want to use that information)

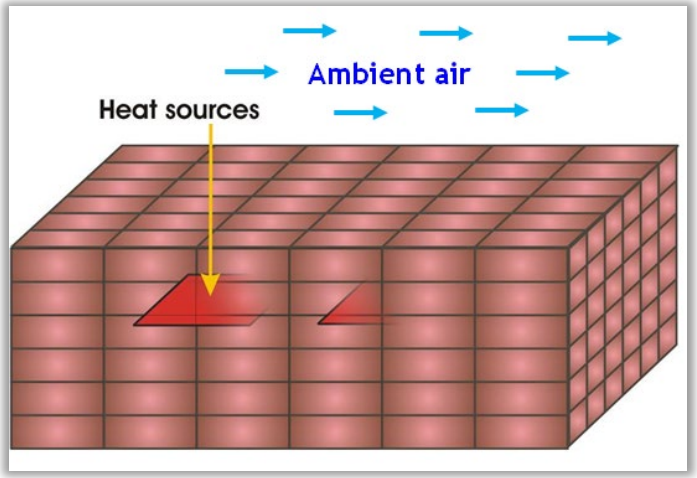
Temperature distribution in IC structure

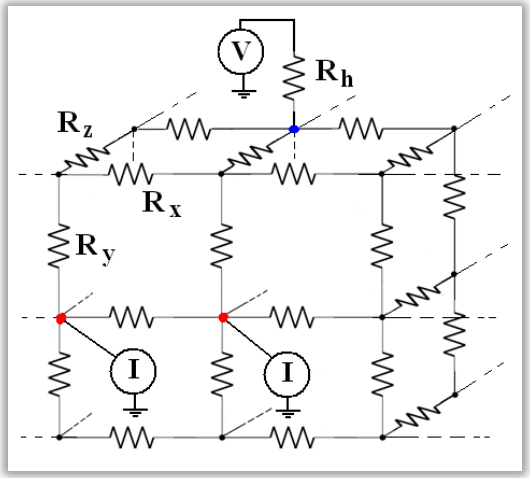
- **Modeling methodology**
  - Use thermal – electrical analogy
  - Thermal problem → electrical circuit
  - Bulk of the material → 3D Resistive network
  - Heat sources → Constant current sources
  - Convective boundaries → Effective resistances
  - Ambient temperature → Constant voltage sources



$$R_x = \frac{\Delta x}{kA}\left[\frac{^oC}{W}\right]$$

$$R_h = \frac{1}{h_e A}\left[\frac{^oC}{W}\right]$$



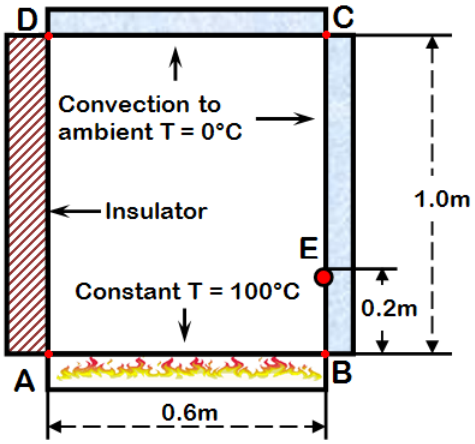


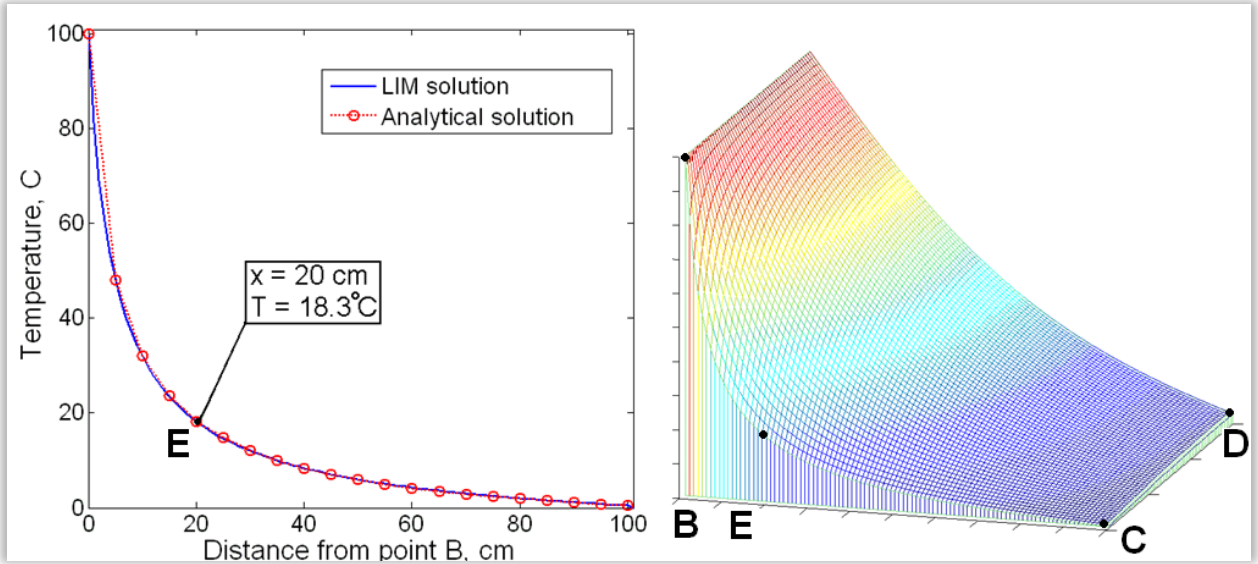
Apply circuit solver

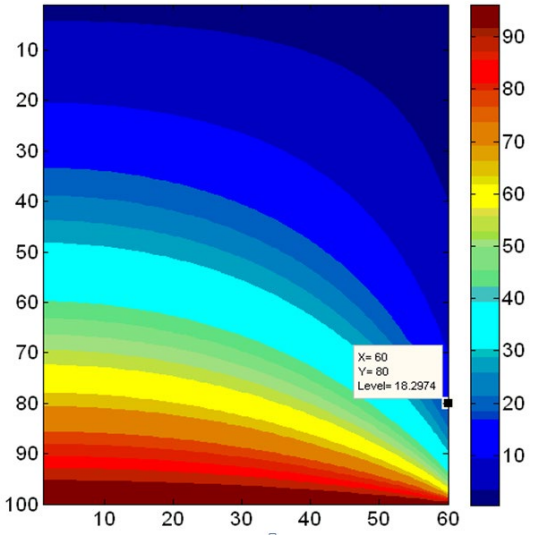
- **Solve the resulting network for node voltages**
  - A major issue – the SIZE of the model

Benchmark Thermal Problem

- 2D benchmark problem (NAFEMS)
  - Simple geometry
  - Has all typical components
  - There is analytical solution
  - Target temperature at E is 18.3 °C

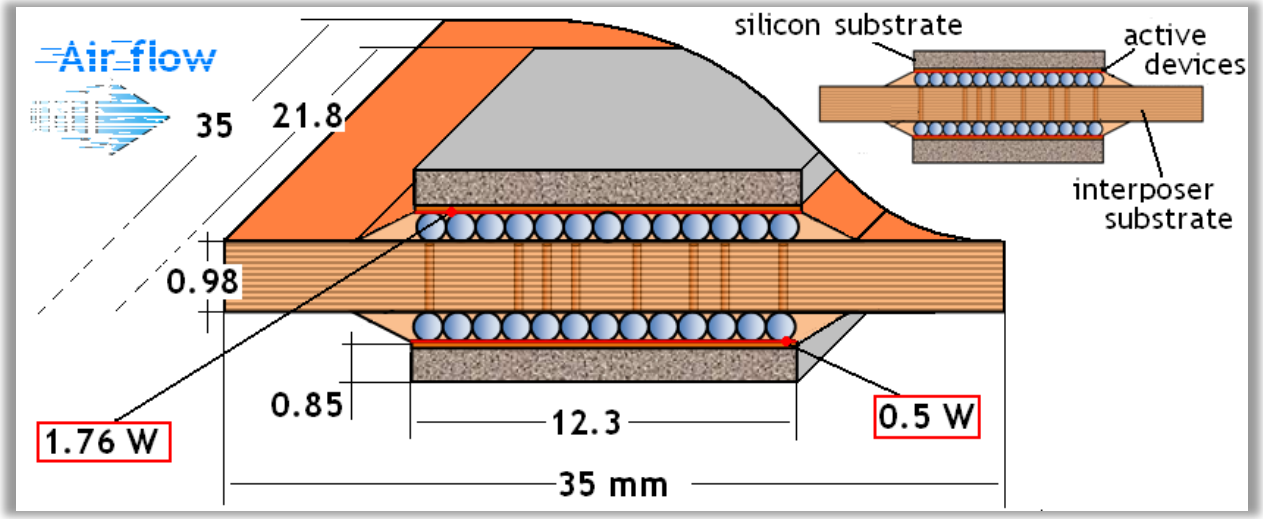


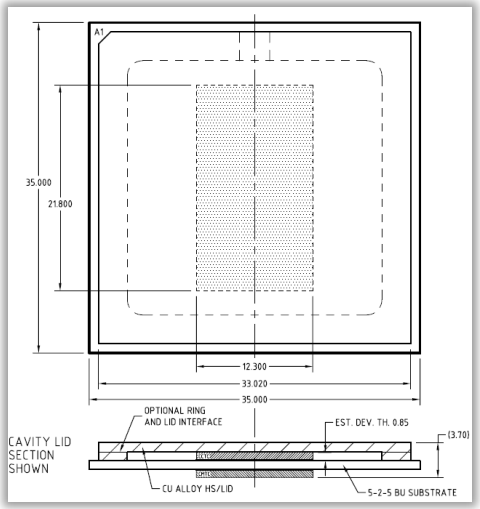




[10] Davies, G.A.O. and Fenner, R. T. and Lewis, R. W., *Background to benchmarks*, NAFEMS, 1993

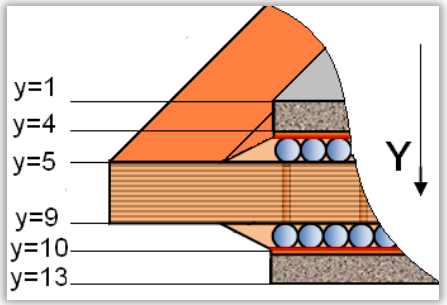
3D Structure. Chip-Interposer-Chip





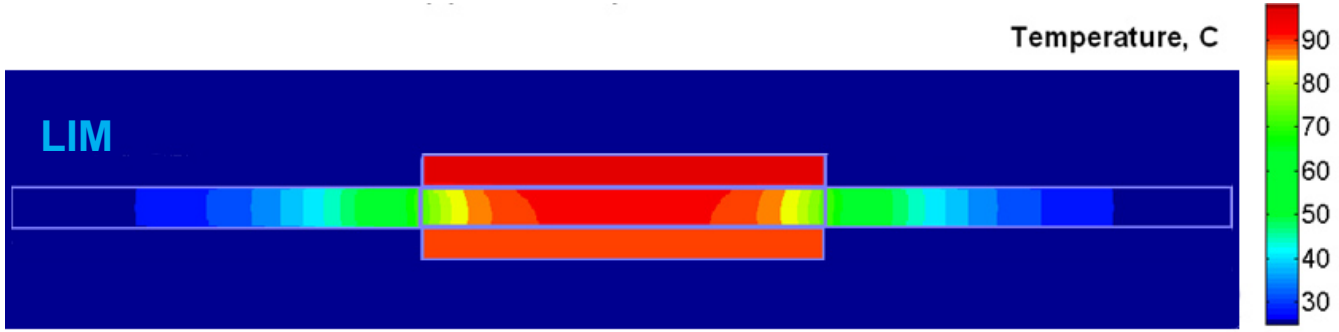
- How hot does the system get ?
- How much heat is transferred from the top chip (controller) to the bottom (memory) ?
- If the via density or distribution is changed, how does that affect the temperature distribution ?
- How much heat can be dissipated through the interposer substrate ?

Model parameters	
Unit cell size (cube)	Δx = 0.2833 mm
Number of nodes	135,089
Number of branches	326,168
Total number of elements	**461,257**

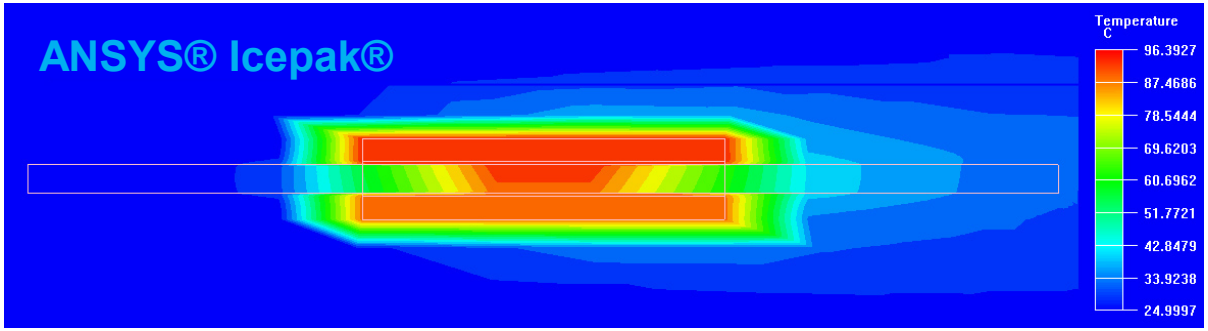


Results of the simulation

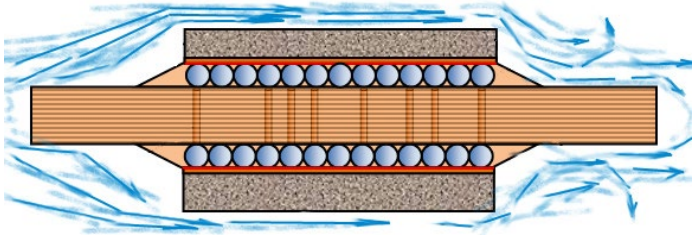
- LIM simulation results in a symmetric temperature profile



- Icepak result is not symmetric

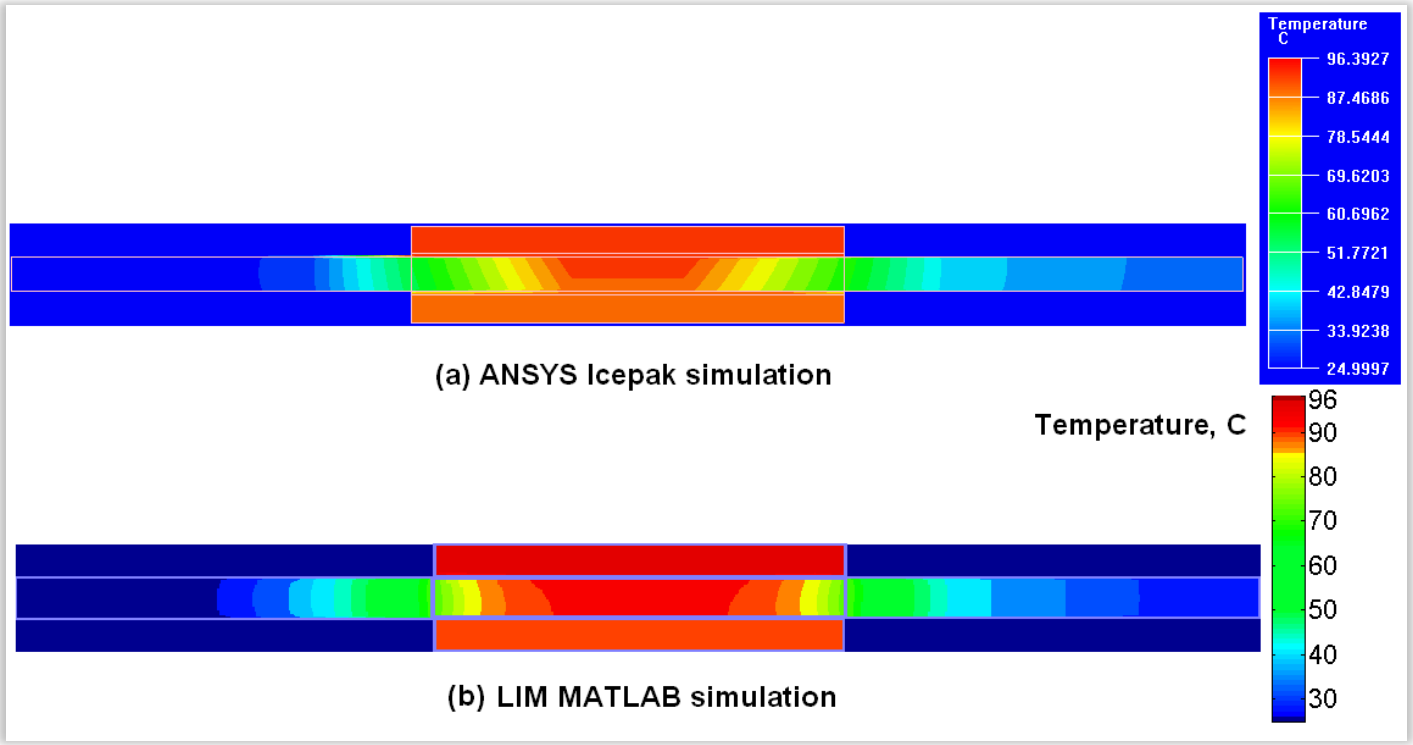


- We need to account for non-uniform cooling



Results with non-uniform cooling

- Cross section of the 3D structure (center cut)
  - Comparison between two pictures from different tools
  - Looking for correct temperature range and general distribution (color maps used by the tools are not exactly the same)
  - In general, very good correlation is observed

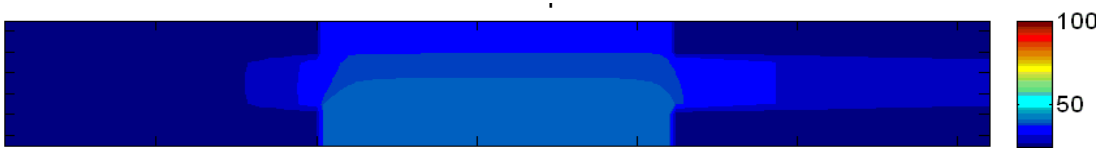


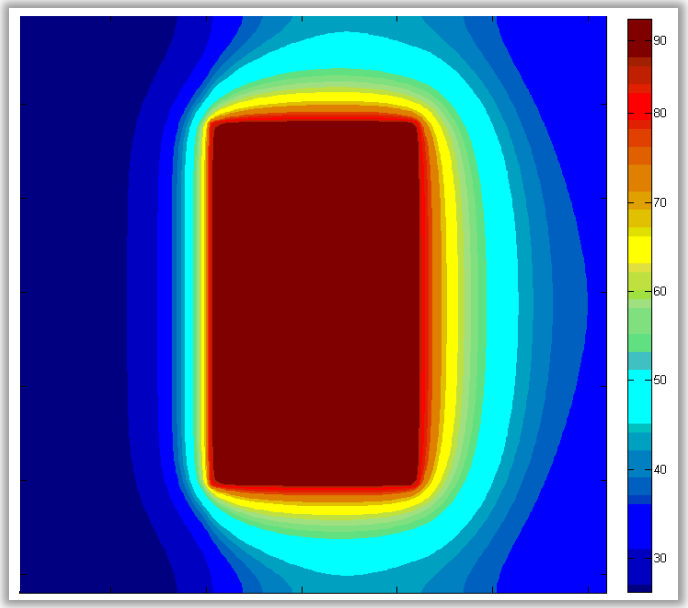
More Results

- Can look at two scenarios

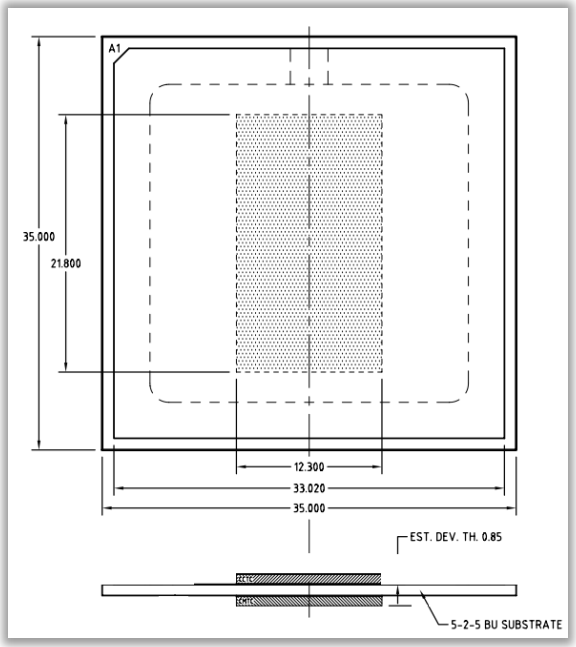
Controller chip is ON

Controller chip is OFF





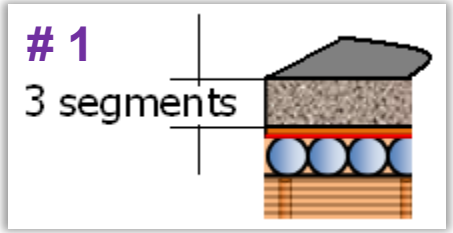
Steady-state temperature profile. Top view of the structure

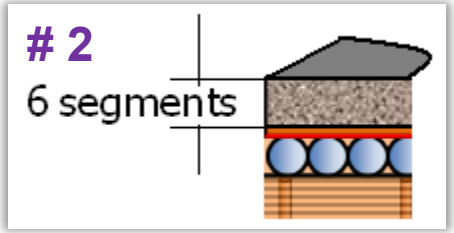


- In our 3D model we can observe any cross-section of the structure

Model Size Issues

- Mesh density considerations
  - coarse mesh results in errors in heat flux calculation
  - geometry of the structure
  - structure of the underlying PDN
  - sizes of elements of interest (TSVs, solder balls, etc.)





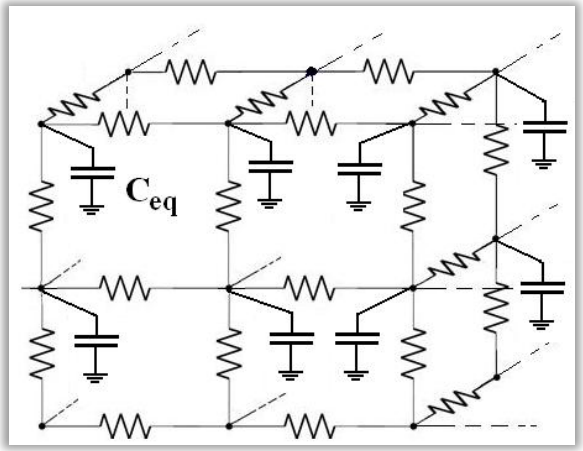
#	Elements	Run time LIM (C++)	Run time LIM (MATLAB)	Run time HSPICE 2010
1	461,257	7	16	27 (total)
2	3,514,400	65	154	949 (total)

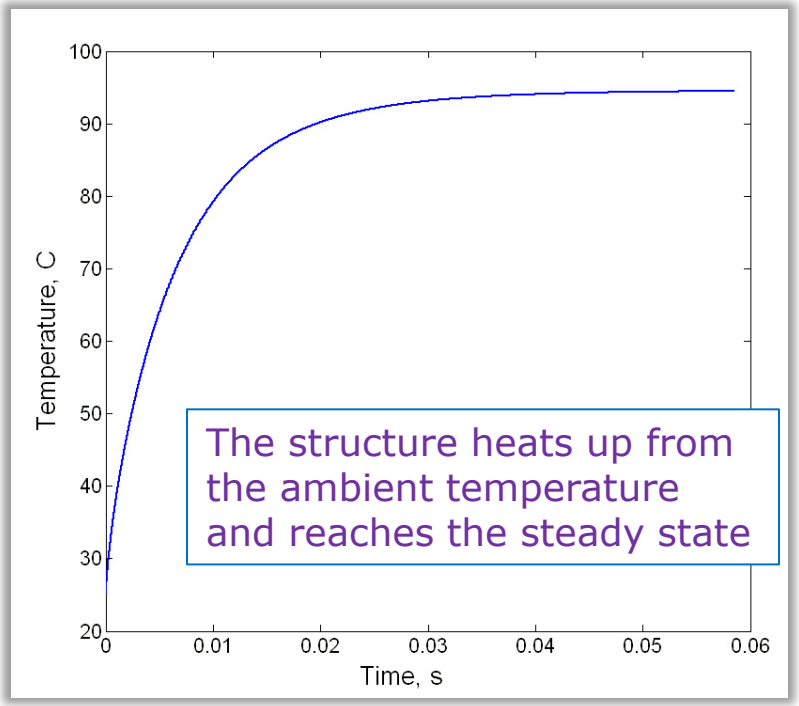
- Typically the size of the equivalent circuit is very large
- Traditional solvers (SPICE) do not scale well with the size of the model

Transient results

- Transient analysis is naturally performed by the LIM
- Insert the actual capacitance instead of fictitious

$$C_{eq} = c_p \cdot \rho \Delta x^3 \left[\frac{W \cdot s}{^oC} \right]$$





- Dynamic heat management through workload distribution
- Cooling management