ECE 451
Packaging Technologies

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Outline

Motivation & Challenges

- Requirements for system-level integration
- Competing technologies and approaches
- More than Moore, SoC vs SoP

Commercial Technologies

- Packaging technologies
- 3D ICs and TSV
- Silicon interposers

Research

- EBG Technology
- On-Chip Oscilloscope
- Multiphysics Modeling (Electro-Thermal Simulations)
System-Level Integration (Microelectronic Packaging)

Semiconductor
* Unprecedented Innovations in CMOS, Si-Ge, Copper Wiring
* Fundamental technical Limits

Electronic Systems
* Computers, telecom & Consumer Products Merge
* Portable, Wireless, & Internet Accessible
* Very Low Cost & Very High Performance

Microelectronic Packaging
* High Cost, Low Performance, Low Reliability
* Lack of Skilled Human Resources
Packaging Challenges

- Package is bottleneck to system performance
- Package cost is increasing percentage of system cost
- Package limits IC technology
- On-chip system can outperform package capability
Advantages of SOC

* Fewer Levels of Interconnections
* Reduced Size and Weight
* Merging of Voice, Video, Data,...

Arguments against SOC

* Challenges too Big
* Legal issues
Challenges for SOC

* Different Types of Devices
* Single CMOS Process for RF and Digital
* Design Methodology not available
* EDA Tools cannot handle level of complexity
* Intellectual Property
* Signal Integrity
* High-Power Requirements of PA
System on a Chip (SOC)
SOC vs SOP

System on Chip

Silicon substrate

Spiral Inductor

Voltage Controlled Oscillator
(UIUC-CAD group – 1999)

System on Package

Passive Components

Ceramic substrate

Triple-band GSM/EDGE Power Amp Module
(RF Design Magazine – 4/02)
## SOP vs SOC

<table>
<thead>
<tr>
<th>Product Category</th>
<th>SOP</th>
<th>SOC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low cost consumer products (&lt;$200)</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>Portable products ($200-$2000)</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Single processor products ($1-$5K)</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>High Performance Products (&gt;5K)</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Automotive and Space Applications</td>
<td>YES</td>
<td>NO</td>
</tr>
</tbody>
</table>
Traditional Design Flow

IC Technology selection
  → Active circuit synthesis
  → Layout tape-out

Package/module selection
  → Passive integration (filters, switches,...)
  → I/O Pad design

Placement routing
  → PC board selection
  → Antenna
Co-Design Flow

IC Design Flow
- IC Technology Selection
  - Routing and I/O
    - Passive implementation: filters, switches, etc...
      - Matching networks
      - Decoupling network/Power distribution
        - Layout
          - RF Simulation

Package Design Flow
- Package Technology Selection
  - Pad placement & I/O
    - Layout
      - Antenna Integration

PCB Design Flow
- PCB Technology Selection
  - Component placement
    - Layout
      - Routing
        - RF Simulation
Dual-in-Line (DIP) Package

- Mounted on PWB in pin-through-hole (PTH) configuration
- Chip occupies less than 20% of total space
- Lead frame with large inductance
# Package Types

<table>
<thead>
<tr>
<th></th>
<th>DIP</th>
<th>QFP</th>
<th>CSP</th>
<th>Flip Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Top View</strong> (showing chip topackage connection)</td>
<td><img src="image1" alt="DIP" /></td>
<td><img src="image2" alt="QFP" /></td>
<td><img src="image3" alt="CSP" /></td>
<td><img src="image4" alt="Flip Chip" /></td>
</tr>
<tr>
<td><strong>Plane View</strong> (showing package to board connection)</td>
<td><img src="image1" alt="DIP" /></td>
<td><img src="image2" alt="QFP" /></td>
<td><img src="image3" alt="CSP" /></td>
<td><img src="image4" alt="Flip Chip" /></td>
</tr>
<tr>
<td>Chip Size (mm × mm)</td>
<td>5 × 5</td>
<td>16 × 16</td>
<td>25 × 25</td>
<td>36 × 36</td>
</tr>
<tr>
<td>Chip Perimeter (mm)</td>
<td>20</td>
<td>64</td>
<td>100</td>
<td>144</td>
</tr>
<tr>
<td>Number of I/Os</td>
<td>64</td>
<td>500</td>
<td>1600</td>
<td>3600</td>
</tr>
<tr>
<td>Chip Pad Pitch (µm)</td>
<td>312</td>
<td>128</td>
<td>625</td>
<td>600</td>
</tr>
<tr>
<td>Package Size (in × in)</td>
<td>3.3 × 1.0</td>
<td>2.0 × 2.0</td>
<td>1.0 × 1.0</td>
<td>1.4 × 1.4</td>
</tr>
<tr>
<td>Lead Pitch (mils)</td>
<td>100</td>
<td>16</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>Chip Area (mm²)</td>
<td>25</td>
<td>256</td>
<td>625</td>
<td>1296</td>
</tr>
<tr>
<td>Feature Size (µm)</td>
<td>2.0</td>
<td>0.5</td>
<td>0.25</td>
<td>0.125</td>
</tr>
<tr>
<td>Gates/Chip</td>
<td>30K</td>
<td>300K</td>
<td>2M</td>
<td>10M</td>
</tr>
<tr>
<td>Max Frequency (MHz)</td>
<td>5</td>
<td>80</td>
<td>320</td>
<td>1280</td>
</tr>
<tr>
<td>Power Dissipation (W)</td>
<td>0.5</td>
<td>7.5</td>
<td>30</td>
<td>120</td>
</tr>
<tr>
<td>Chip Pow Dens (W/cm²)</td>
<td>2.9</td>
<td>4.8</td>
<td>9.3</td>
<td>2.0</td>
</tr>
<tr>
<td>Pack Pow Dens (W/cm²)</td>
<td>0.024</td>
<td>0.3</td>
<td>4.8</td>
<td>9.8</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>5</td>
<td>3.3</td>
<td>2.2</td>
<td>1.5</td>
</tr>
<tr>
<td>Supply Current (A)</td>
<td>0.1</td>
<td>2.3</td>
<td>13.6</td>
<td>80</td>
</tr>
</tbody>
</table>
## Substrate Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Surface roughness (μm)</th>
<th>$10^4 \tan\delta$ at 10 GHz</th>
<th>$\varepsilon_r$</th>
<th>Thermal conductivity K (W/cm²/°C)</th>
<th>Dielectric strength (kV/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Air (dry)</td>
<td>N/A</td>
<td>~0</td>
<td>1</td>
<td>0.00024</td>
<td>30</td>
</tr>
<tr>
<td>Alumina: 99.5%</td>
<td>0.05-0.25</td>
<td>1-2</td>
<td>10.1</td>
<td>0.37</td>
<td>$4 \times 10^3$</td>
</tr>
<tr>
<td></td>
<td>96%</td>
<td>5-20</td>
<td>9.6</td>
<td>0.28</td>
<td>$4 \times 10^3$</td>
</tr>
<tr>
<td></td>
<td>85%</td>
<td>30-50</td>
<td>15</td>
<td>0.2</td>
<td>$4 \times 10^3$</td>
</tr>
<tr>
<td>Sapphire</td>
<td>0.005-0.025</td>
<td>0.4-0.7</td>
<td>9.4,11.6</td>
<td>0.4</td>
<td>$4 \times 10^3$</td>
</tr>
<tr>
<td>Glass, typical</td>
<td>0.025</td>
<td>20</td>
<td>5</td>
<td>0.01</td>
<td>-</td>
</tr>
<tr>
<td>Polyimide</td>
<td>-</td>
<td>50</td>
<td>3.2</td>
<td>0.002</td>
<td>4.3</td>
</tr>
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<th>Dielectric strength (kV/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Irradiated polyolefin</td>
<td>1</td>
<td>2.3</td>
<td>0.001</td>
<td>~300</td>
<td></td>
</tr>
<tr>
<td>Quartz (fused) i.e. SiO2</td>
<td>0.006-0.025</td>
<td>1</td>
<td>3.8</td>
<td>0.01</td>
<td>$10 \times 10^3$</td>
</tr>
<tr>
<td>Beryllia</td>
<td>0.05-1.25</td>
<td>1</td>
<td>6.6</td>
<td>2.5</td>
<td>-</td>
</tr>
<tr>
<td>Rutile</td>
<td>0.25-2.5</td>
<td>4</td>
<td>100</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Ferrite/garnet</td>
<td>0.25</td>
<td>2</td>
<td>13-16</td>
<td>0.03</td>
<td>$4 \times 10^3$</td>
</tr>
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<th>Dielectric strength (kV/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR4 circuit board</td>
<td>~6</td>
<td>100</td>
<td>4.3-4.5</td>
<td>0.005</td>
<td>-</td>
</tr>
<tr>
<td>RT-duroid 5880</td>
<td>0.75-1 4.25-8.75</td>
<td>5-15</td>
<td>2.16-2.24</td>
<td>0.0026</td>
<td>-</td>
</tr>
<tr>
<td>RT-duroid 6010</td>
<td>0.75-1 4.25-8.75</td>
<td>10-60</td>
<td>10.2-10.7</td>
<td>0.0041</td>
<td>-</td>
</tr>
<tr>
<td>AT-1000</td>
<td>-</td>
<td>20</td>
<td>10.0-13.0</td>
<td>0.0037</td>
<td>-</td>
</tr>
<tr>
<td>Cu-flon</td>
<td>-</td>
<td>4.5</td>
<td>2.1</td>
<td>-</td>
<td>-</td>
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<th>Thermal conductivity $K$ (W/cm²/°C)</th>
<th>Dielectric strength (kV/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si (high resistivity)</td>
<td>0.025</td>
<td>10-100</td>
<td>11.9</td>
<td>0.9</td>
<td>300</td>
</tr>
<tr>
<td>GaAs</td>
<td>0.025</td>
<td>6</td>
<td>12.85</td>
<td>0.3</td>
<td>350</td>
</tr>
<tr>
<td>InP</td>
<td>0.025</td>
<td>10</td>
<td>12.4</td>
<td>0.4</td>
<td>350</td>
</tr>
<tr>
<td>SiO2 (on chip)</td>
<td>-</td>
<td>-</td>
<td>4.0-4.2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>LTCC (typical green tape 951)</td>
<td>0.22</td>
<td>15</td>
<td>7.8</td>
<td>3</td>
<td>400</td>
</tr>
</tbody>
</table>
Ceramic Substrate
Stacked Wire Bonds
Ball Bonding for Flip Chip
Flip Chip Pin Grid Array (FC-PGA)
3D Packaging

3D Packaging

Key concepts

- Wires
  - shorter
  - lots of it

- Heterogeneous integration
  - Analog and digital
  - Technologies (GaAs and Si?)

3D Industry

- Samsung
  - 16Gb NAND flash (2Gx8 chips) Wide Bus DRAM
- Micron
  - Wide Bus DRAM
- Intel
  - CPU + Memory
- OKI
  - CMOS Sensor
- Xilinx
  - 4 die 65 nm interposer
- Raytheon/Ziptronix
  - PIN Detector Device
- IBM
  - RF Silicon Circuit Board/ TSV Logic & Analog
- Toshiba
  - 3D NAND
Through-Silicon Vias


TSV Density: $10/cm^2 - 10^8/cm^2$
Through-Silicon Vias (TSV)

Advantages

- Make use of third dimension
- Several orders of magnitude (10/cm² to 10⁸/cm²)
- Minimize interconnection length
- More design flexibility

Issues

- 3D Infrastructure & supply chain
- I/O Standardization
- EMI
- Thermal management and reliability

From Koyanagi et al., IEEE Proceedings, Feb 2009
TSV Pitch ≠ Area / Number of TSVs

- TSV pitch example
  - 1024 bit busses require a lot of space with larger TSVs
  - They connect to the heart and most dense area of processing elements
  - The 45nm bus pitch is ~100 nm; TSV pitch is > 100x greater

Through-Silicon Vias (TSV)

- Via First
- Via Last
- Via at Front End (FEOL)
- Via at Mid line
- Via at Back end (BEOL)

Through-Silicon Vias (TSV)

TSV-Based Products

STMicro CMOS image sensor in WLP/TSV package

Sony Video / DSC camera with BSI CMOS image sensors

Elpida’s 3D TSV stacked DRAM memory

There are currently about 15 different 3D-IC pilot lines worldwide
3D-IC and TSV

• Stacking of chips makes heat transfer through the z-direction difficult.
• Lossy silicon substrate makes coupling between adjacent TSVs strong.
• TSV noise can be easily coupled to the adjacent TSV through conductive silicon substrate.
• 3D IC yields are much lower than 2D-IC.
• Difficult to detect TSV and MOS failures.

Solution: Use 2.5D integration.
2.5D Integration

• 2.5D-IC emerges as a temporary solution
• In 2.5D-IC, several chips are stacked on interposer only homogeneous chip stacking is used.
• Fine-pitch metal routing is necessary because it increase I/O counts
• For this purpose, an interposer is used where small width and small space metal routing is possible.
• Silicon substrate is usually used for an interposer because on-silicon metallization process is mature and fine-pitch metal routing is possible
Silicon Interposers

Silicon Interposers

Source: Jong-Min Yook, Dong-Su Kim, and Jun-Chul Kim, "Double-sided Si-Interposer with Embedded Thin Film Devices", 2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013), pp 757-760.
Silicon Interposers

Source: Jong-Min Yook, Dong-Su Kim, and Jun-Chul Kim, "Double-sided Si-Interposer with Embedded Thin Film Devices", 2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013), pp 757-760.
HI – The Interconnect Challenge

“There are many solutions and techniques for improving transistors; options for improving interconnects are very few…”

Challenges
- Signal/power integrity
- Thermal effects
- IR Drop
- Power dissipation
- High I/O count
- Reliability
- Security
- Environment
- Architecture
Integration Components

- Transistors
- Nonlinear
- SPICE
- Scaling with tech

- Interconnects
- Linear
- EM Tools
- Scaling with $\lambda$

- Transmission lines, sensors
- Linear+Nonlinear
- EM Extraction, SPICE, IBIS,…
- Scaling with $\lambda$
Co-Design for HI

- Focus on minimizing energy and delay
- Identify and address conflicting requirements,
- Take advantage of novel interconnect technologies
- Leverage from AI methodologies
- Address design and computational complexity

Source: Zuken
Chiplets and HI

• Multilevel Power Distribution
  - Chiplets advantageous
  - Boundary between chip and package is blurred
  - Concurrent design is necessity
  - SI/PI, multilevel frequencies
  - System-level verification challenging
Codesign for Chiplets

Source: IEEE-EPS HIR Roadmap
Chiplets – Package Model

C4 landing pad

inter-chiplet I/O

side view

C4

CL1

CL2

uBGA

Substrate landing pad

PW

GD

BGA

signal

PW

GD

BGA

Chiplet boundary

Interposer top view

Core pin map

Uni-lateral inter-chiplet I/O

Bi-lateral inter-chiplet I/O

Uni-lateral inter-chiplet I/O

Bi-lateral inter-chiplet I/O

extern al IO

C or e

interposer

substrate

Under-fill

chiplets

signal

inter-chiplet I/O
I/O Channel Design

• D2D Interfaces
  - Bunch of Wires (BoW)
  - Universal Chiplet Interconnect Express (UCIe)
  - Initial specifications released
  - Development still under way
  - Focus on best practices for SI/PI

BOW Slice – Source: [1]

[1] Shahab Ardalan, Ramin Farjadrad, Mark Kuemerle, Ken Poulton, Suresh Subramaniam, Bapiraju Vinnakota, "Chiplet Communication Link: Bunch of Wires (BoW)", IEEE Micro, Jan/Feb 2021
Intelligent/Active Interposers

- **Components**
  - Neural TSVs
  - Neuroprimitives
  - Smart materials
  - Reconfigurable devices

- **Viable Platforms for**
  - Tunable PDN
  - HI of logic, memory
  - PLL, equalizers
Multi-Physics Co-Design

- TSV
- Interposers
- BGA
- EMIB
- Chiplets

Design Optimizer

- 3D Design Flow
- Multiphysics Algorithms
- Multidomain Algorithms
- Interface/Integrator

Architecture

- Logic
- Memory
- Analog
- RF

Enablers

Driver/Application

- Multicore
- Accelerators

Constraints

- Bandwidth
- Thermal
- Power
- Signal Integrity
- I/O
- Security
- Reliability
- Environment
Multiphysics & MOR

Electrical

Thermal

Power

I/O

Model-Order Reduction

MOR

E

T

P

I

MOR

MOR

Model-Order Reduction
AI/ML for System-Level

- Chiplet arrangement
- Package geometry
- I/O interface standards (AIB)
- etc.

- Eye width/height
- Jitter
- Noise
- etc.