ECE 451
Advanced Microwave Measurements

Signal Integrity

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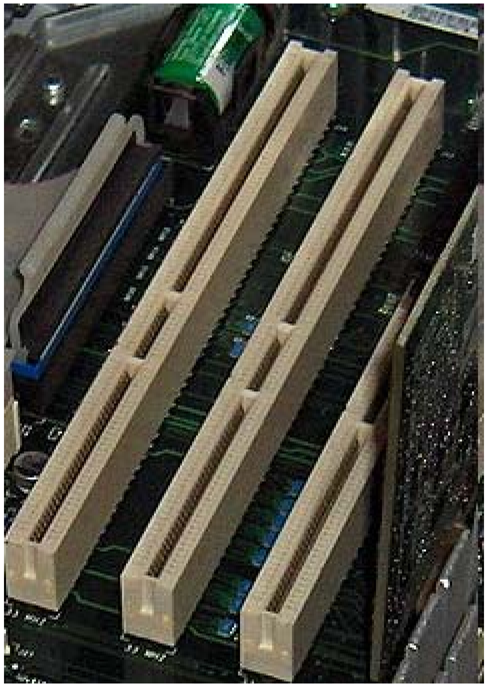
Signal Integrity

- **Attenuation & Loss (skin effect, on-chip loss)**
- **Crosstalk (interconnect proximity, coupling)**
- **Dispersion (frequency dependence of parameters)**
- **Reflection (unmatched loads, reactive loads, ISI)**
- **Distortion (nonlinear loads)**
- **Interference & Radiation (EMI/EMC)**
- **Rise time degradation**
- **Clock skew (different electrical path lengths)**

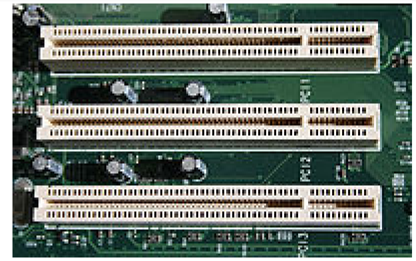
PCI



- **PC Interface**
  - For external cards
  - Graphics, Network, Sound, etc…
  - Parallel

Conventional PCI

PCI Local Bus

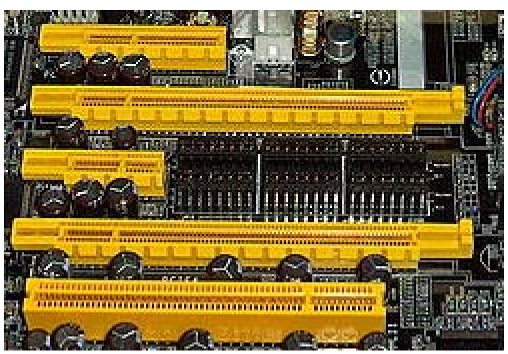


Three 5V 32-bit PCI expansion slots on a motherboard

Year created:	July 1993
Created by:	Intel
Superseded by:	PCI Express (2004)
Width:	32 or 64 bits
Number of devices:	1 per slot
Capacity	133 MB/s
Style:	Parallel
Hotplugging?	Optional
External?	no

PCI-Express

- **Computer Expansion Card Standard**
  - ➢ Replaced older PCI
  - ➢ Based on serial links
  - ➢ Capacity up to 1 Gb/s
  - ➢ V3.0 scheduled for 2010



PCI Express	
PCI Express logo	
Year created:	2004
Created by:	Intel
Width:	1 bit
Number of devices:	1 per slot
Capacity	Per lane: ▪ **v1.x**: 250 MB/s ▪ **v2.0**: 500 MB/s ▪ **v3.0**: 1 GB/s
Style:	Serial
Hotplugging?	Depends on form factor
External?	Yes, with External PCI Express

Universal Serial Bus (USB)

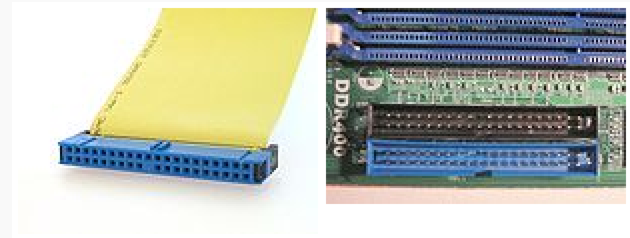
USB *Universal Serial Bus*	
CERTIFIED USB™ Original USB Logo	
Year created:	January 1996
Created by:	Intel, Compaq, Microsoft, Digital, IBM, Northern Telecom
Width:	1 bit
Number of devices:	127 per host controller
Capacity	12 or 480 Mbit/s (1.5 to 60 MByte/s)
Style:	Serial
Hotplugging?	Yes
External?	Yes

- **Interfaces devices to computers**
  - No rebooting
  - Low power
  - No need for external power supply
  - 480 Mb/s

IDE

- **Expansion Card Standard**
  - ➢ Replaced older PCI
  - ➢ Based on serial links
  - ➢ Capacity up to 1 Gb/s
  - ➢ V3.0 scheduled for 2010

AT Attachment with Packet Interface



ATA connector on the left, with two motherboard ATA connectors on the right.

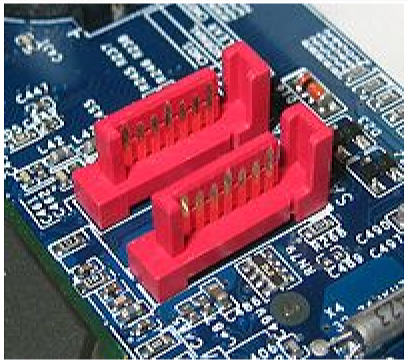
Type	Internal storage device connector	
Production history		
Designer	Western Digital, subsequently amended by many others	
Designed	1986	
Superseded by	Serial ATA (2003)	
Specifications		
Hot pluggable	No	
External	No	
	Width	16 bits
	Bandwidth	16 MB/s originally later 33, 66, 100 and 133 MB/s
	Max devices	2 (master/slave)
	Protocol	Parallel
Cable	40 or 80 wires ribbon cable	
Pins	40	
Pin out		

Serial - ATA

- **Storage interface**
  - Replaces older parallel ATA or IDE
  - Based on serial links
  - Capacity up to 3 Gb/s
  - Hot swapping capability

	SATA 1.5Gb/s	SATA 3Gb/s
Frequency	1500 MHz	3000 MHz
Bits/clock	1	1
8b10b encoding	80%	80%
bits/Byte	8	8
Real speed	150 MB/s	300 MB/s

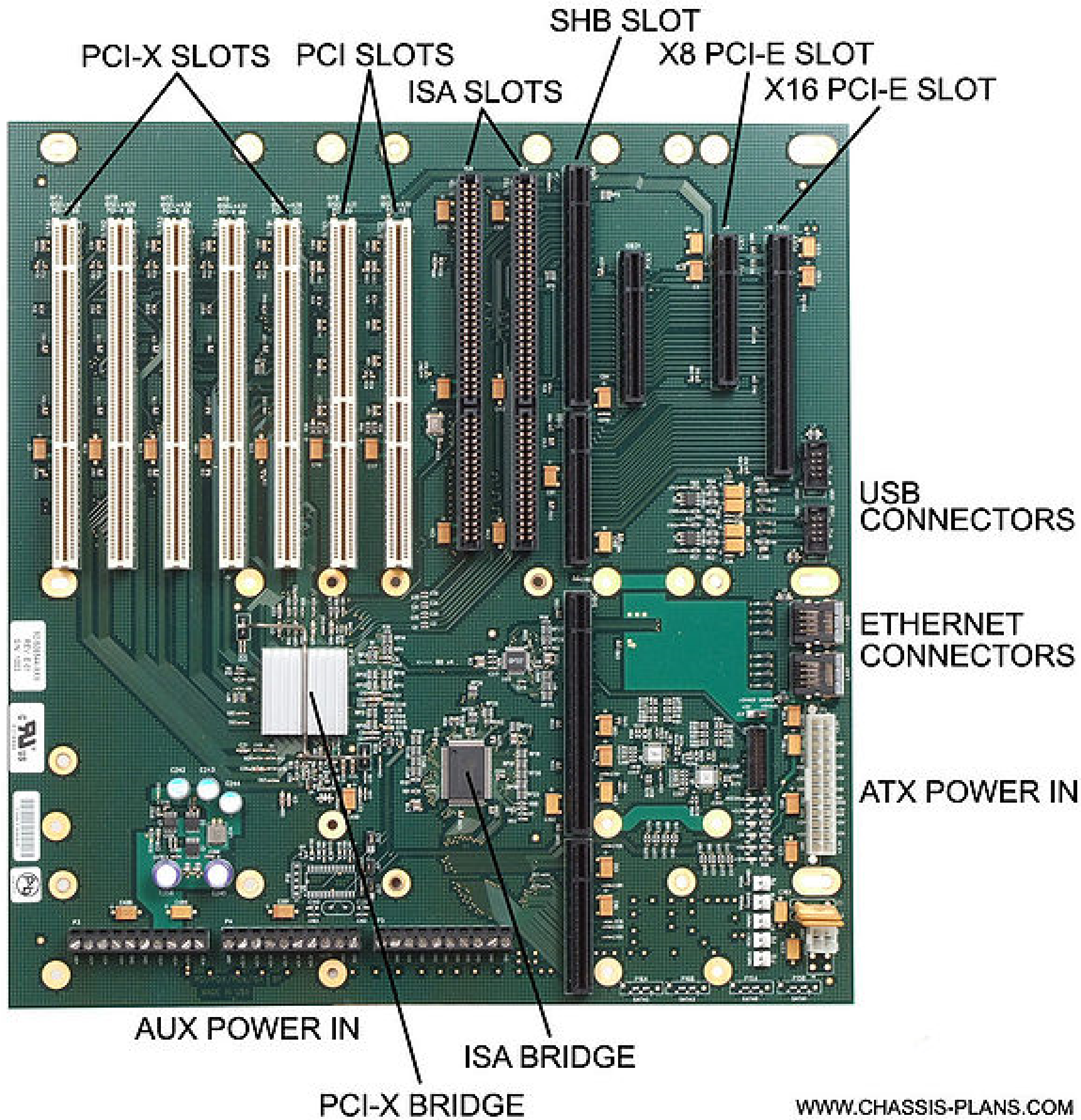
SATA
Serial ATA



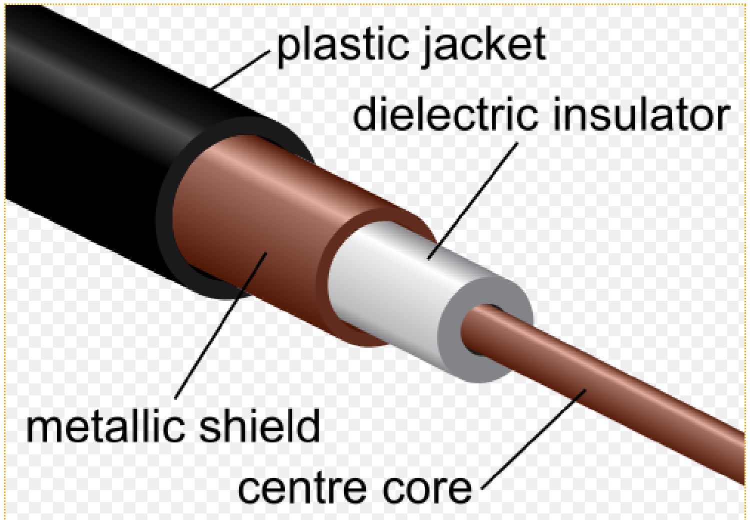
First generation (1.5 Gbit/s) SATA ports on a motherboard

Year created:	2003
Number of devices:	1
Style:	Serial
Hotplugging?	Yes, with support of other system components
External?	Yes, with eSATA

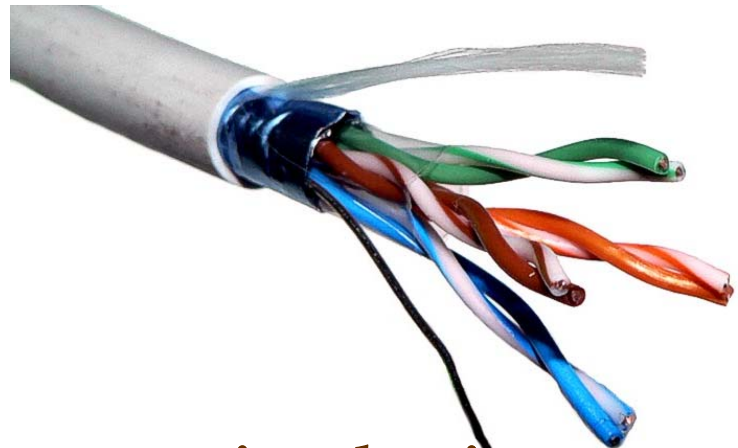
Motherboards and Backplanes



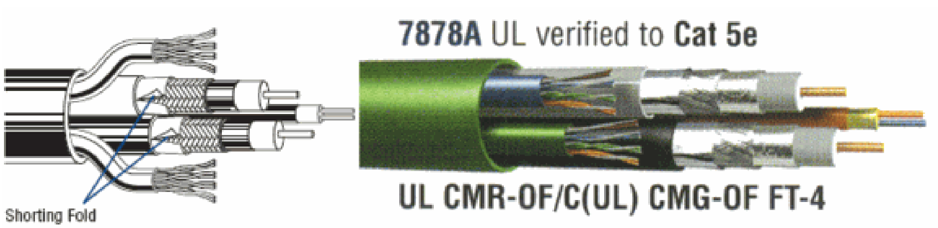
Cables and Transmission Lines

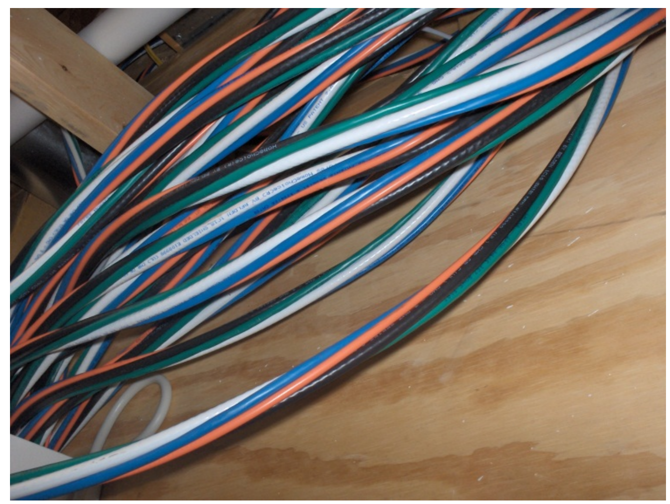


coaxial



twisted pairs





Cable Specifications

Table of RG standards

type	approx. impedance	core	dielectric			overall diameter		braid	velocity factor	comments
			type	[in]	[mm]	in	mm			
RG-6/U	75 Ω	1.0 mm	Solid PE	0.185	4.7	0.332	8.4	double	0.75	Low loss at high frequency for cable television, satellite television and cable modems
RG-6/UQ	75 Ω		Solid PE			0.298	7.62	quad		This is "quad shield RG-6". It has four layers of shielding; regular RG-6 only has one or two
RG-8/U	50 Ω	2.17 mm	Solid PE	0.285	7.2	0.405	10.3			Thicknet (10base5) and amateur radio
RG-9/U	51 Ω		Solid PE			0.420	10.7			Thicknet (10base5)
RG-11/U	75 Ω	1.63 mm	Solid PE	0.285	7.2	0.412	10.5		0.66	Used for long drops and underground conduit
RG-58/U	50 Ω	0.9 mm	Solid PE	0.116	2.9	0.195	5.0	single	0.66/0.78	Used for radiocommunication and amateur radio, thin Ethernet (10base2) and NIM electronics. Common.
RG-59/U	75 Ω	0.81 mm	Solid PE	0.146	3.7	0.242	6.1	single	0.66	Used to carry baseband video in closed-circuit television, previously used for cable television. Generally it has poor shielding but will carry an HQ HD signal or video over short distances.
RG-62/U	92 Ω		Solid PE			0.242	6.1	single	0.84	Used for ARCNET and automotive radio antennas.
RG-62A	93 Ω		ASP			0.242	6.1	single		Used for NIM electronics
RG-174/U	50 Ω	0.48 mm	Solid PE	0.100	2.5	0.100	2.55	single	0.66	Common for wifi pigtails: more flexible but higher loss than RG58; used with LEMO 00 connectors in NIM electronics.
RG-178/U	50 Ω	7×0.1 mm (Ag pltd Cu clad Steel)	PTFE	0.033	0.84	0.071	1.8	single	0.69	
RG-179/U	75 Ω	7×0.1 mm (Ag pltd Cu)	PTFE	0.063	1.6	0.098	2.5	single	0.67	VGA RGBHV
RG-213/U	50 Ω	7×0.0296 in Cu	Solid PE	0.285	7.2	0.405	10.3	single	0.66	For radiocommunication and amateur radio, EMC test antenna cables. Typically lower loss than RG58. Common.
RG-214/U	50 Ω	7×0.0296 in	PTFE	0.285	7.2	0.425	10.8	double	0.66	
RG-218	50 Ω	0.195 in Cu	Solid PE	0.660 (0.680?)	16.76 (17.27?)	0.870	22	single	0.66	Large diameter, not very flexible, low loss (2.5dB/100' @ 400 MHz), 11kV dielectric withstand.
RG-223	50 Ω	2.74mm	PE Foam	0.285	7.24	0.405	10.29	Double		

Computer Interconnections

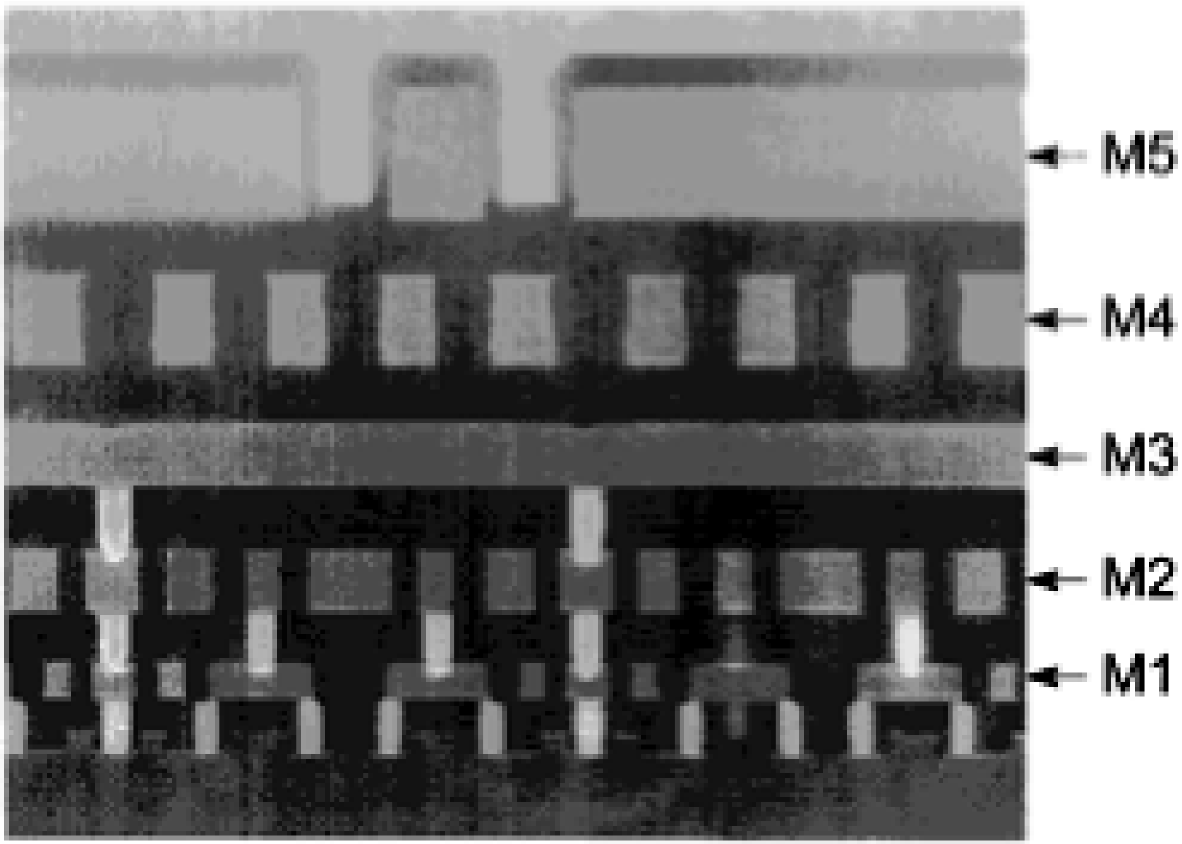
Name	Raw bandwidth (Mbit/s)	Transfer speed (MB/s)	Max. cable length (m)	Power provided	Devices per Channel
SAS	3000	375	8	No	4
eSATA	3000	300	2 with eSATA HBA (1 with passive adapter)	No[18]	1 (15 with port multiplier)
SATA 300	3000	300	1	No	1 (15 with port multiplier)
SATA 150	1500	150	1	No	1 per line
PATA 133	1064	133	0.46 (18 inches)	No	2
FireWire 3200	3144	393	100; alternate cables available for 100 m+	15 W, 12–25 V	63 (with hub)
FireWire 800	786	98.25	100[19]	15 W, 12–25 V	63 (with hub)
FireWire 400	393	49.13	4.5[19][20]	15 W, 12–25 V	63 (with hub)
USB 2.0	480	60	5[21]	2.5 W, 5 V	127 (with hub)
USB 3.0*	5000	625	3[22]	4.5 W, 5 V	127 (with hub)[22]
Ultra-320 SCSI	2560	320	12	No	15 (plus the HBA)
Fibre Channel over copper cable	4000	400	12	No	126 (16777216 with switches)
Fibre Channel over optic fiber	10520	2000	2–50000	No	126 (16777216 with switches)
Infiniband 12X Quad-rate	120000	12000	5 (copper)[23][24] <10000 (fiber)	No	1 with Point to point Many with switched fabric

Semiconductor Technology Trends

	1997	2003	2006	2012
Chip size (mm^2)	300	430	520	750
Number of transistors (million)	11	76	200	1400
Interconnect width (nm)	200	100	70	35
Total interconnect length (km)	2.16	2.84	5.14	24

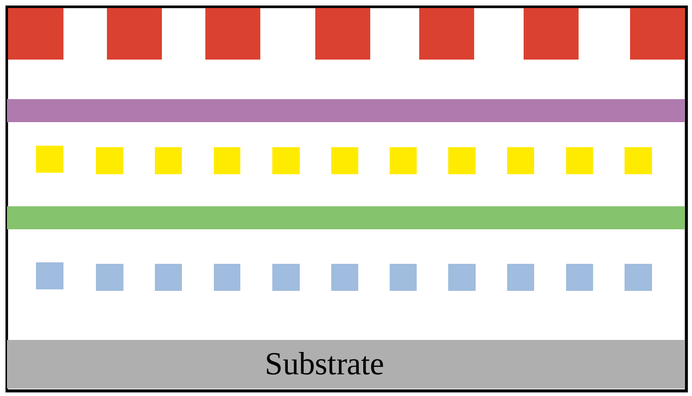
5-Layer Interconnect Technology 0.25 μm

Vertical parallel-plate capacitance	0.05 fF/μm^2
Vertical parallel-plate capacitance (min width)	0.03 fF/μm
Vertical fringing capacitance (each side)	0.01 fF/μm
Horizontal coupling capacitance (each side)	0.03



Source: M. Bohr and Y. El-Mansy - *IEEE TED Vol. 4, March 1998*

Integrated Circuit Wiring

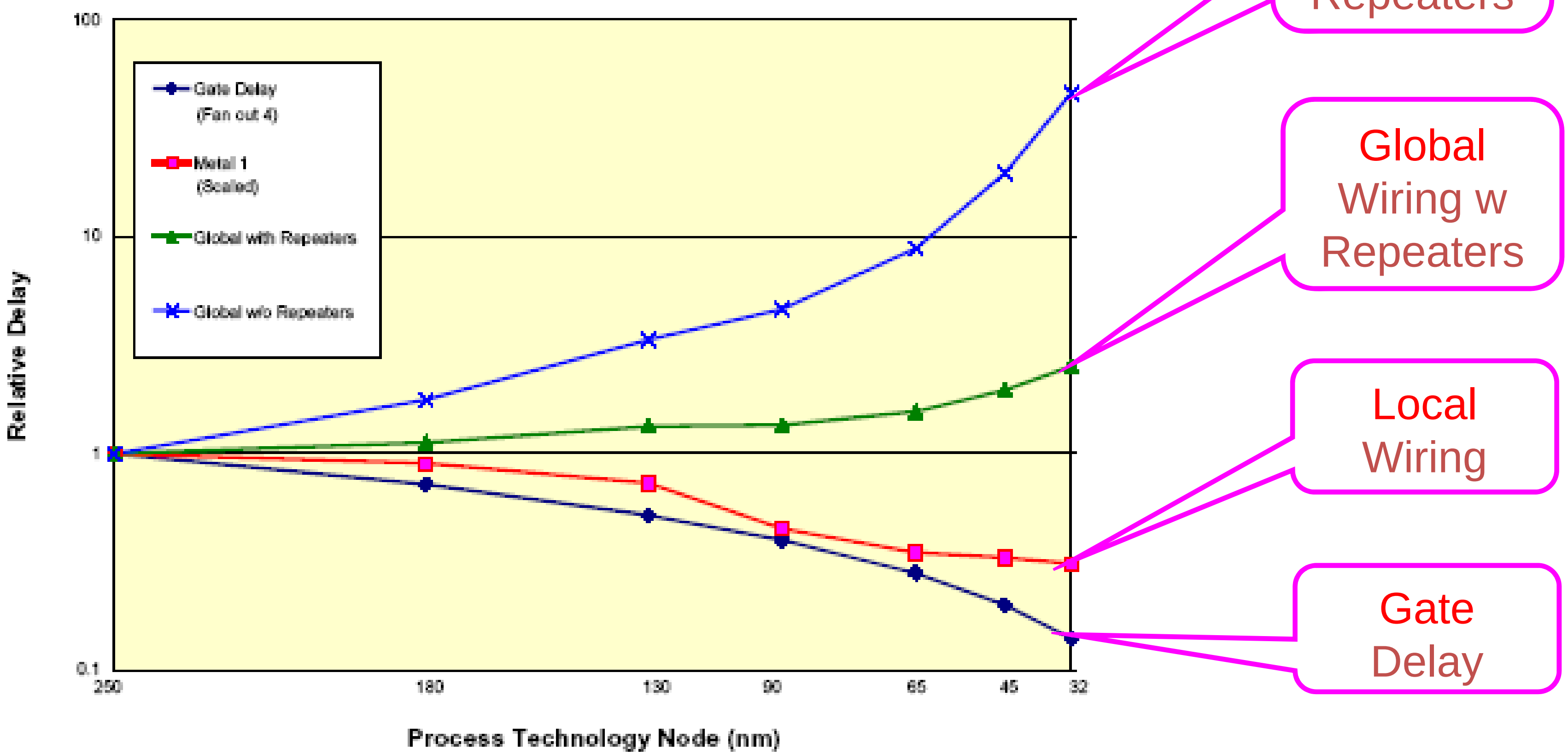


Vertical parallel-plate capacitance	0.05 fF/μm^2
Vertical parallel-plate capacitance (min width)	0.03 fF/μm
Vertical fringing capacitance (each side)	0.01 fF/μm
Horizontal coupling capacitance (each side)	0.03

Signal Delay Trend

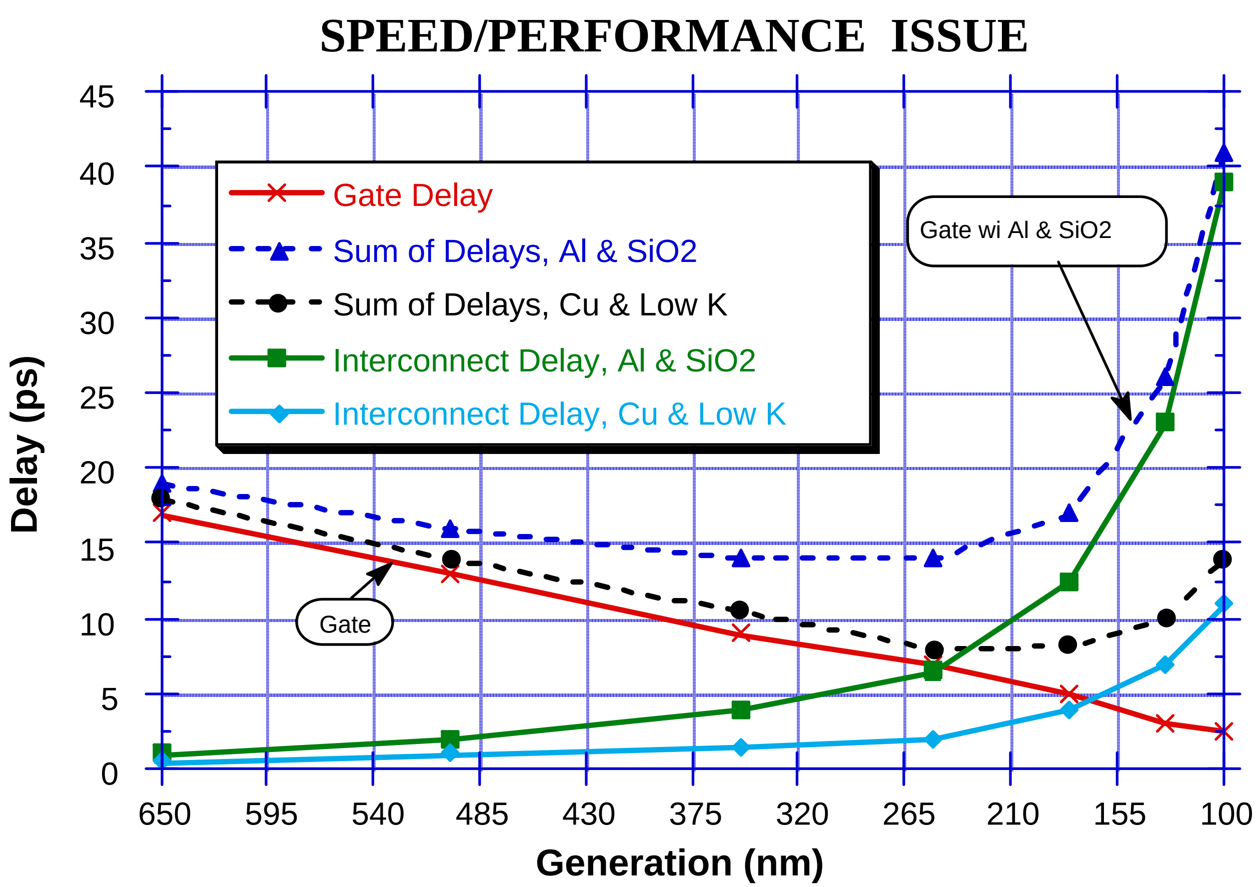
Signal Delay → *gates* delay / *interconnect* delay

Delay for Metal 1 and Global Wiring versus Feature Size



Source: ITRS roadmap 2004

The Interconnect Bottleneck



Al 3.0 $\mu\Omega$-cm
Cu 1.7 $\mu\Omega$-cm
SiO2 $\kappa = 4.0$
Low κ $\kappa = 2.0$
Al & Cu .8μ *Thick*
Al & Cu Line 43μ *Long*

Interconnect

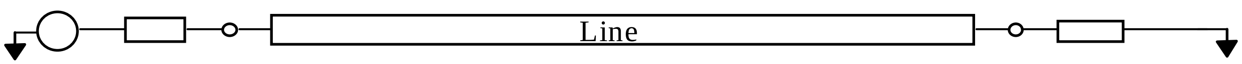
- Total interconnect length (m/cm^2) – active wiring only, excluding global levels will increases:

Year	2003	2004	2005	2006	2007	2008	2009
Total Length	579	688	907	1002	1117	1401	1559

- Interconnect power dissipation is more than 50% of the total dynamic power consumption in 130nm and will become dominant in future technology nodes

- Interconnect centric design flows have been adopted to reduce the length of the critical signal path

Chip-Level Interconnect Delay

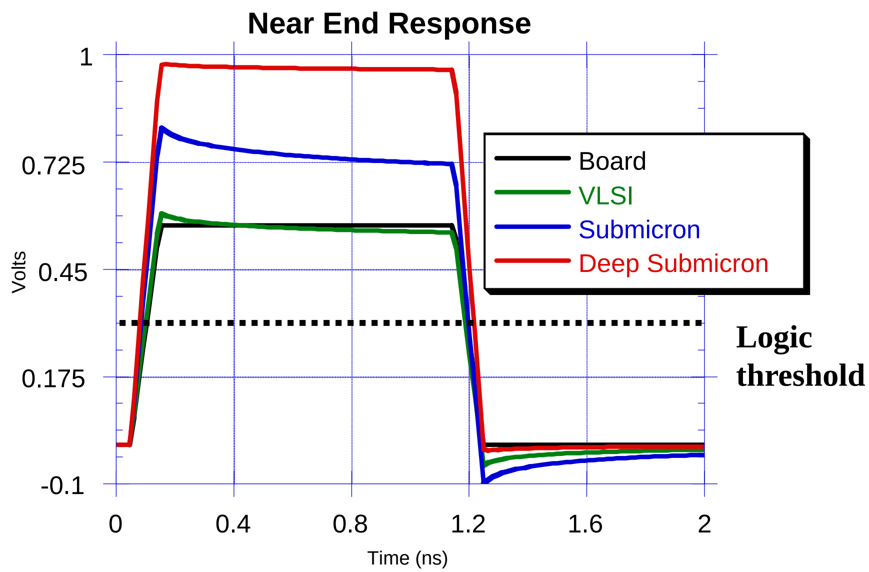


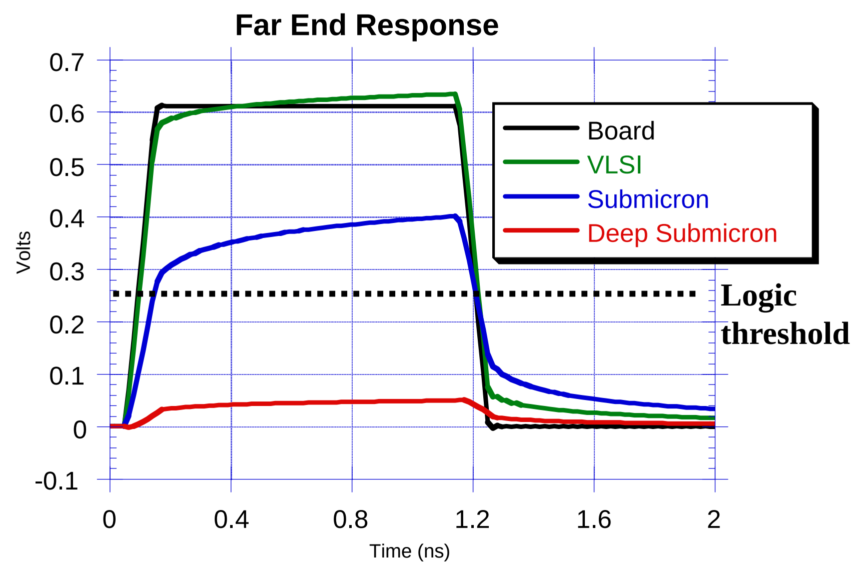
Pulse Characteristics:

- rise time: 100 ps
- fall time: 100 ps
- pulse width: 4ns

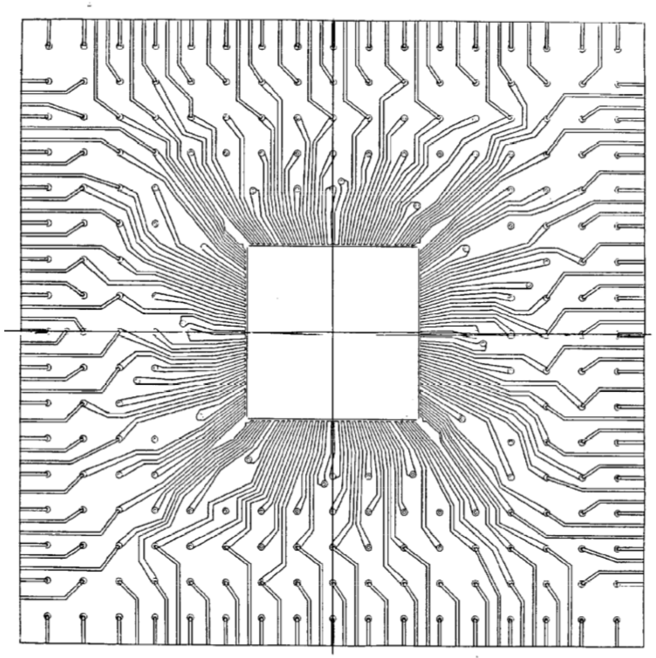
Line Characteristics

- length : 3 mm
- near end termination: 50 Ω
- far end termination 65 Ω

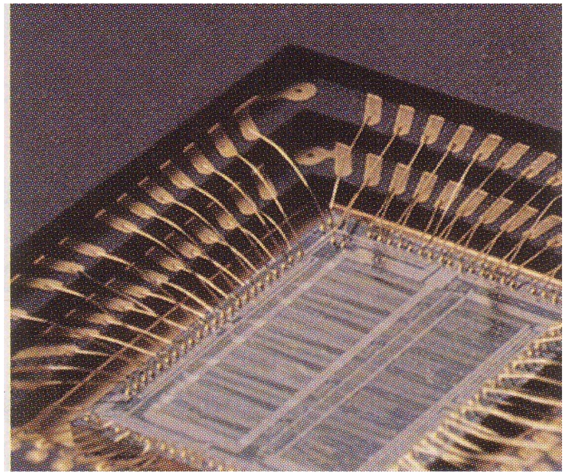




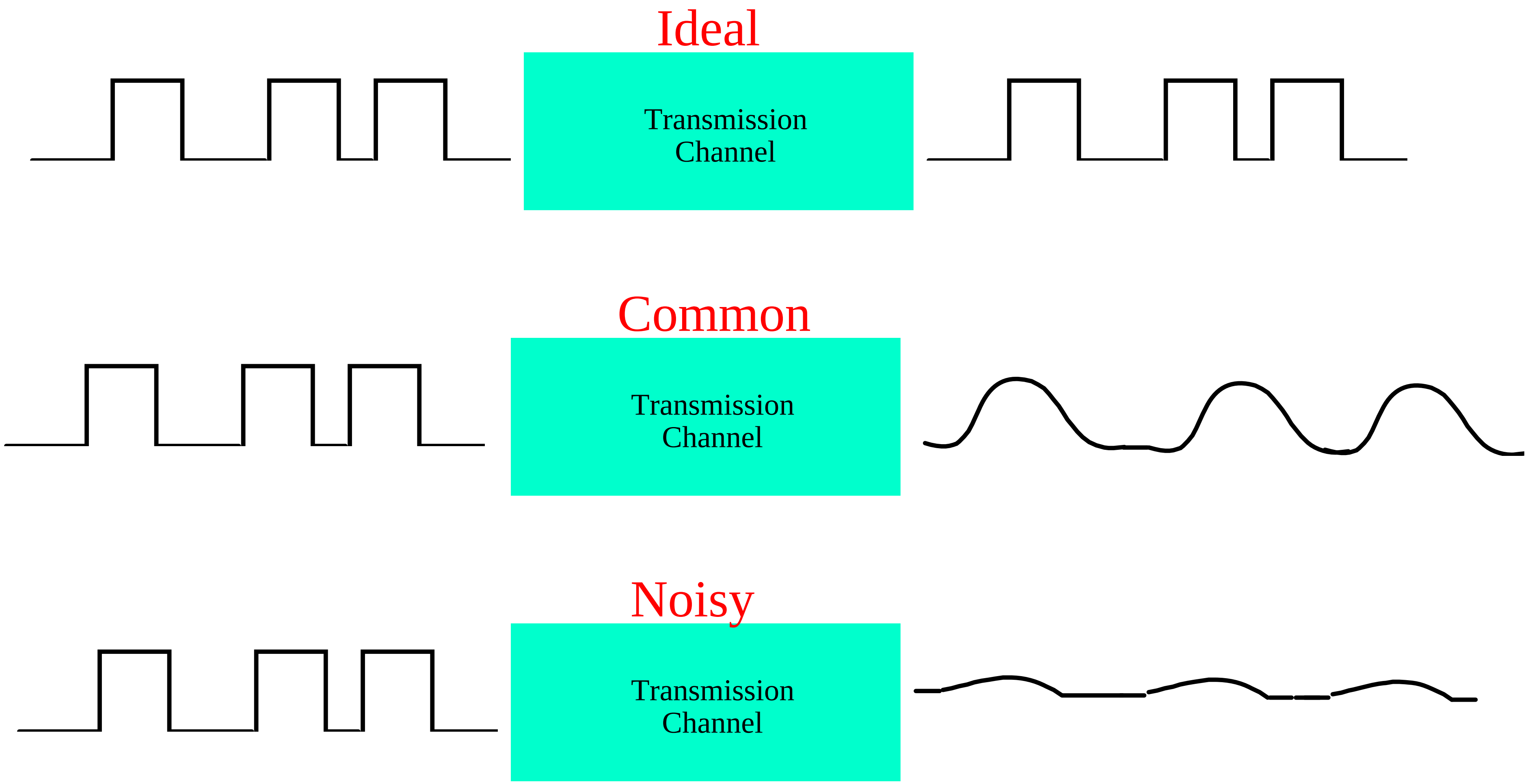
Package-Level Complexity



- Up to 16 layers
- Hundreds of vias
- Thousands of TLs
- High density
- Nonuniformity



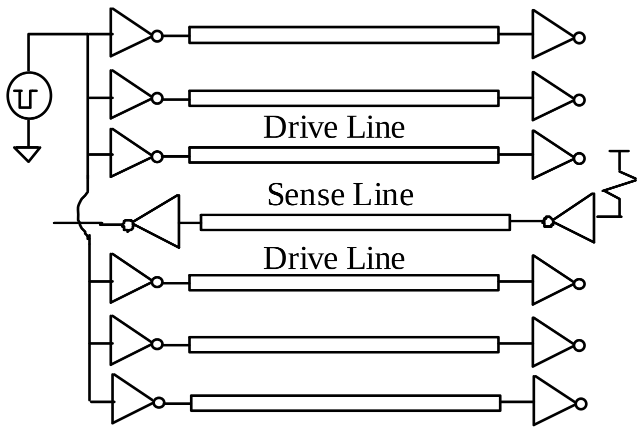
Signal Integrity

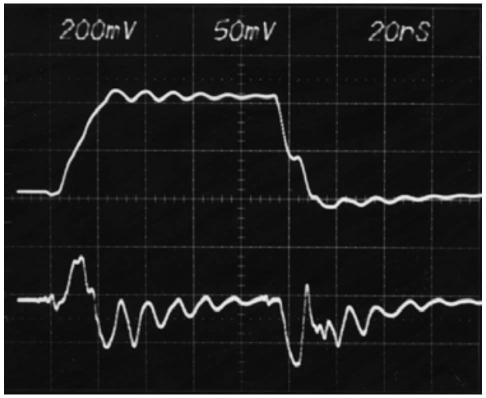


Interconnect Bottleneck

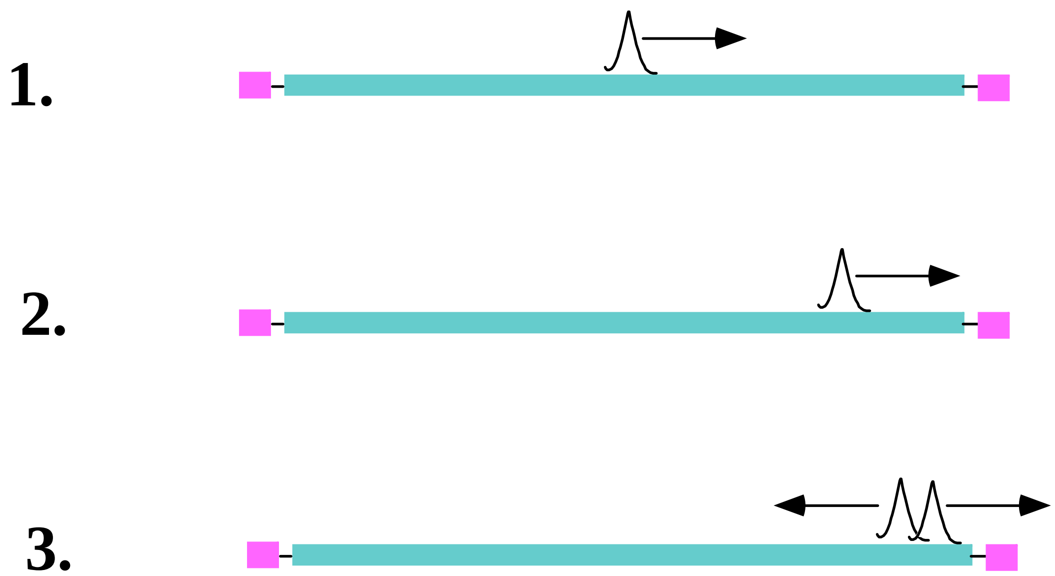
Signal Integrity

Crosstalk	**Dispersion**	**Attenuation**
Reflection	**Distortion**	**Loss**
Delta I Noise	**Ground Bounce**	**Radiation**

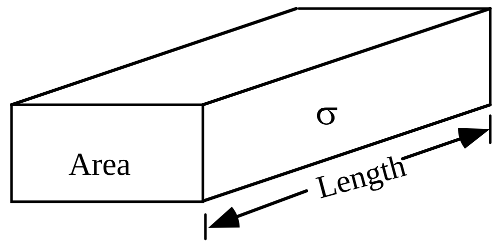




Reflection in Transmission Lines



Metallic Conductors



$$\text{Resistance}: R$$

$$R = \frac{\text{Length}}{\sigma\ \text{Area}}$$

Package level:

W=3 mils

R=0.0045 Ω/mm

Submicron level:

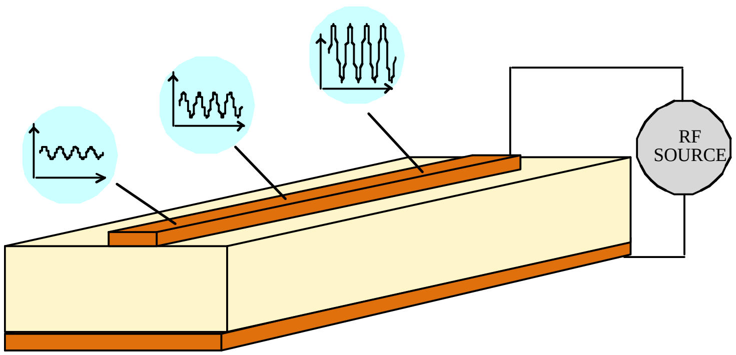
W=0.25 microns

R=422 Ω/mm

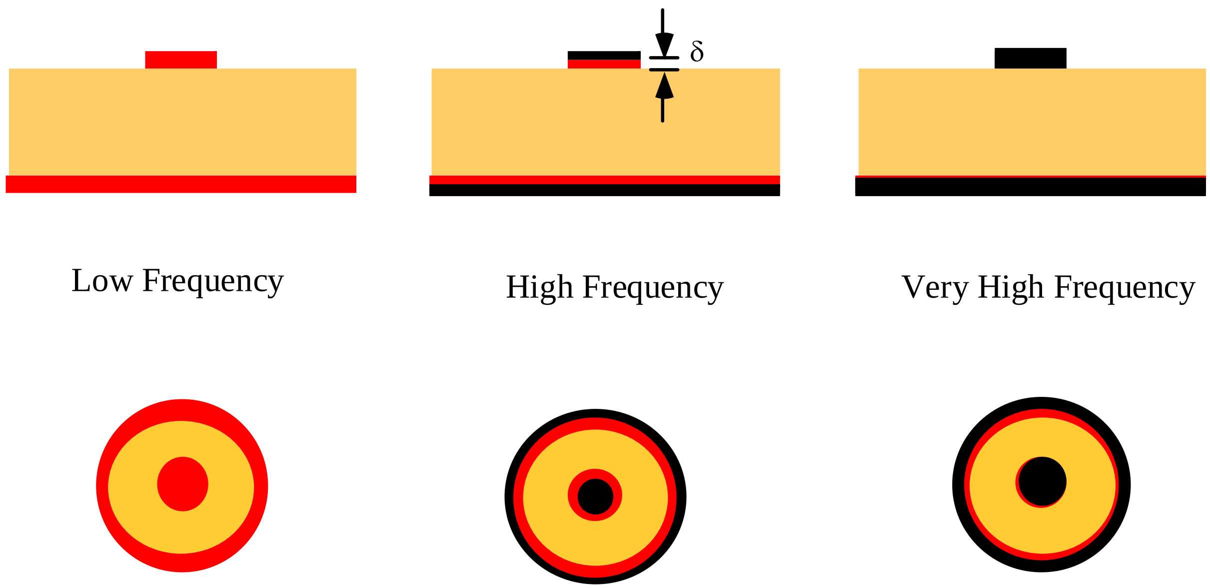
Metallic Conductors

Metal	Conductivity σ (Ω^{-1} m^{-1} $\times 10^{-7}$)
Silver	6.1
Copper	5.8
Gold	3.5
Aluminum	1.8
Tungsten	1.8
Brass	1.5
Solder	0.7
Lead	0.5
Mercury	0.1

Loss in Transmission Lines



Skin Effect in Transmission Lines



Skin Depth

$$\vec{E} = \hat{x}E_o e^{-\gamma z} = \hat{x}E_o e^{-\alpha z} e^{-j\beta z}$$ ← **Wave decay**

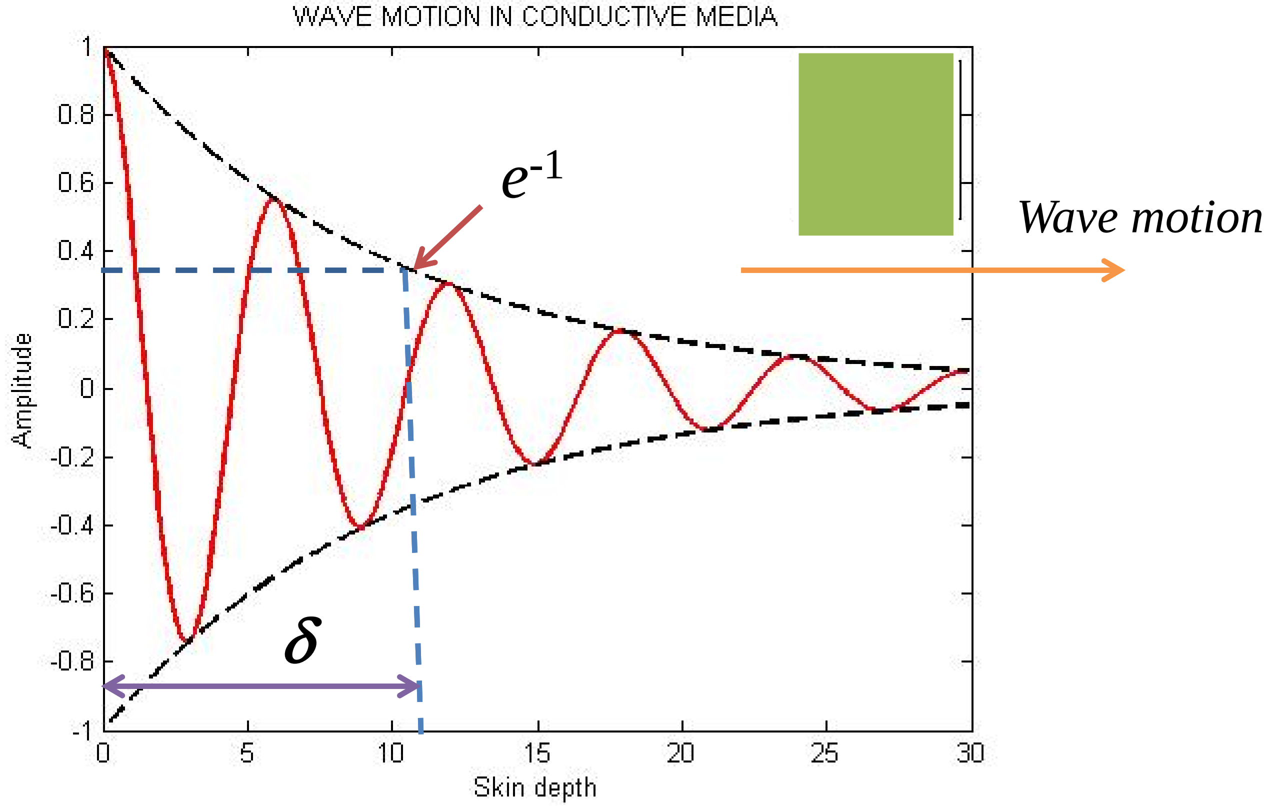
The decay of electromagnetic wave propagating into a conductor is measured in terms of the *skin depth*

Definition: skin depth δ is distance over which amplitude of wave drops by *1/e*.

$$\delta = \frac{1}{\alpha}$$

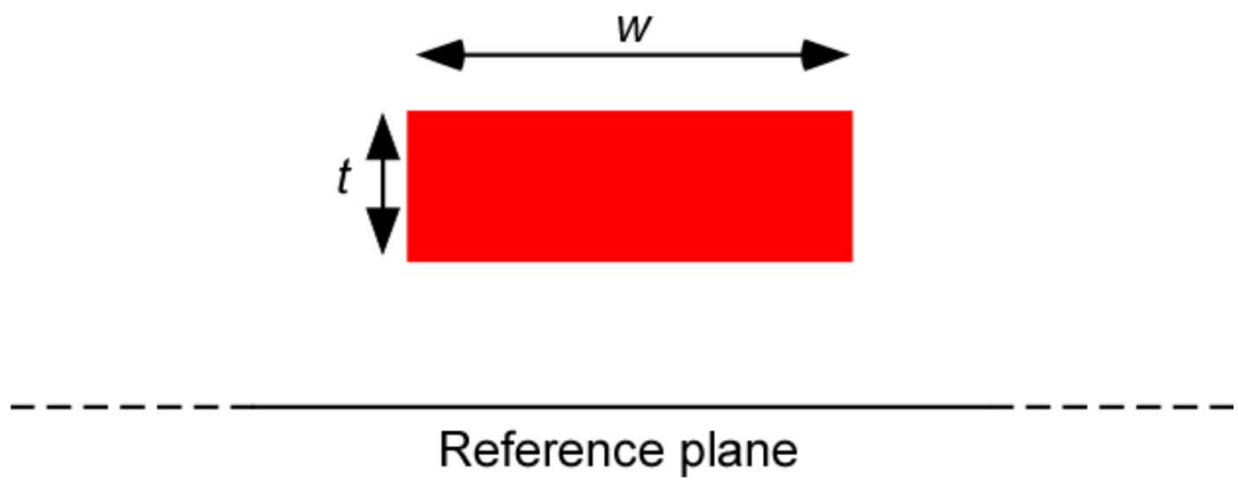
For good conductors: $$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}$$

Skin Depth



For perfect conductor, $\delta = 0$ and current only flows on the surface

DC Resistance

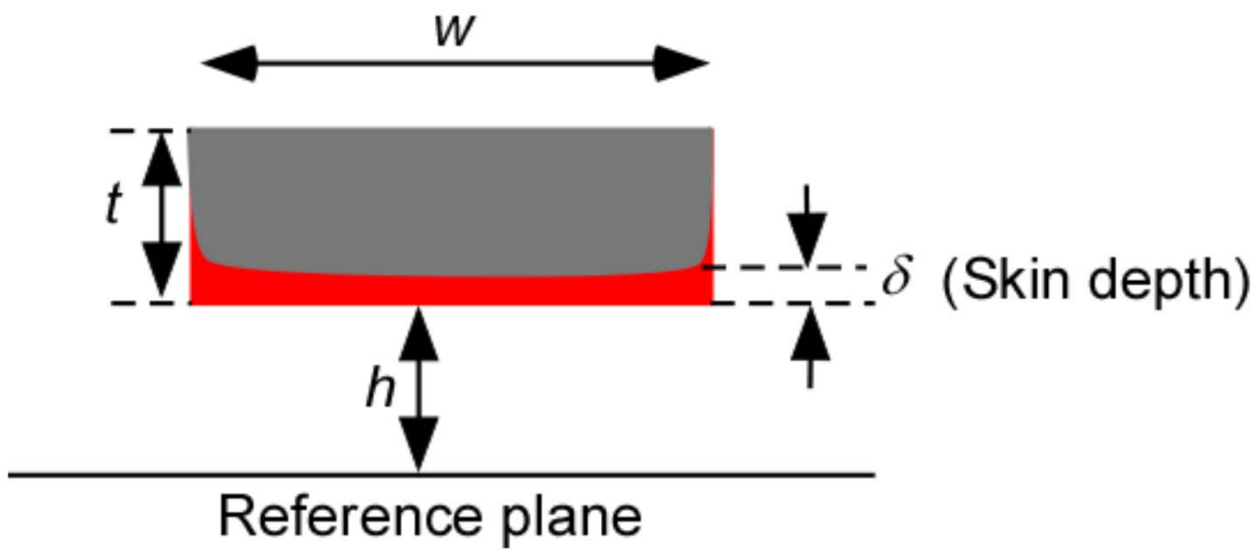


$$R_{dc} = \frac{l}{\sigma w t}$$

l: conductor length

σ: conductivity

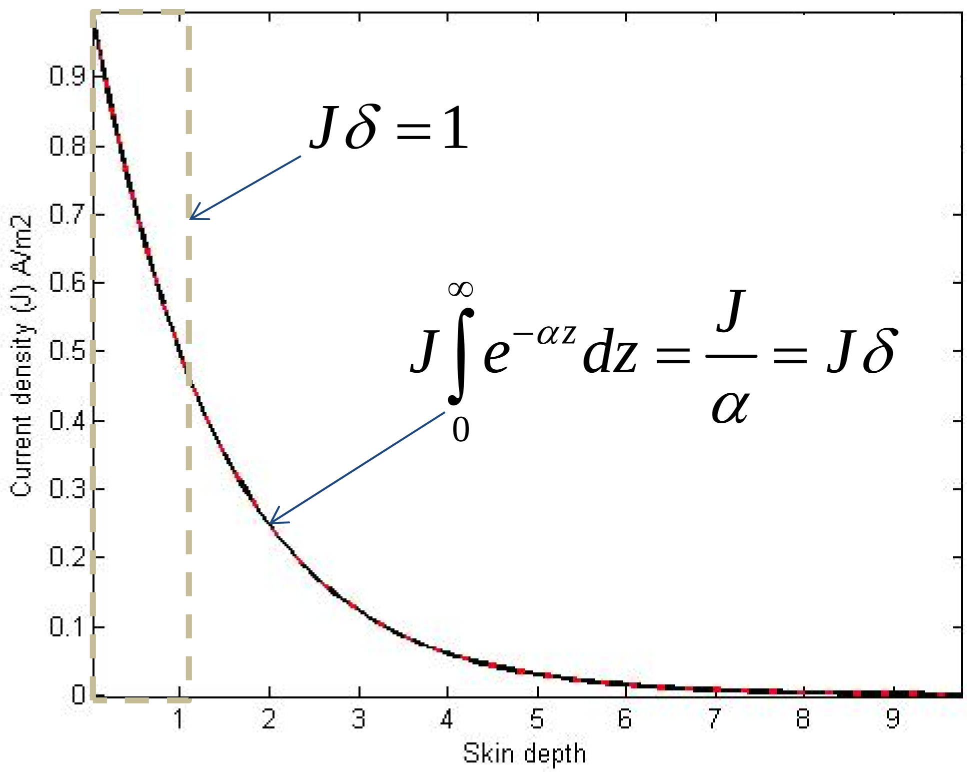
AC Resistance



$$R_{ac} = \frac{l}{\sigma w \delta} = \frac{l}{\sigma w \sqrt{2/\omega\mu\sigma}} = \frac{l}{w}\sqrt{\frac{\pi\mu f}{\sigma}}$$

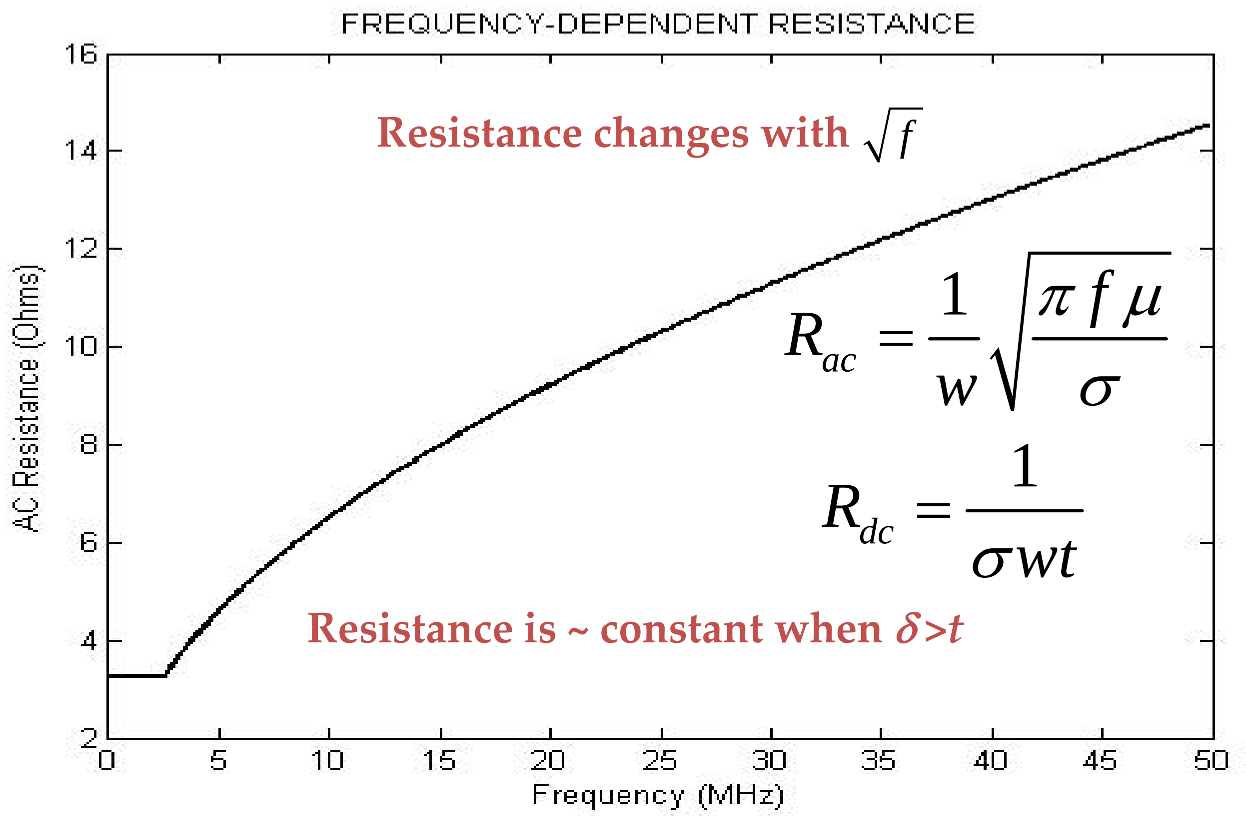
l: conductor length
σ: conductivity
f: frequency

Frequency-Dependent Resistance

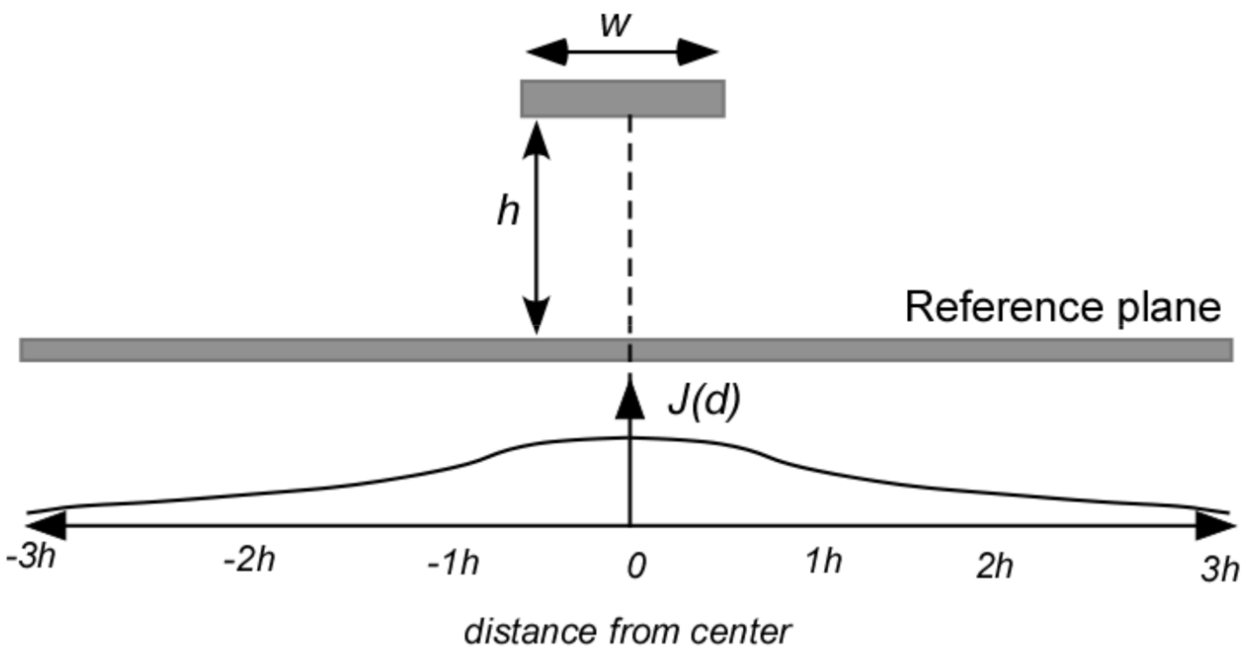


Approximation is to assume that all the current is flowing uniformly within a skin depth

Frequency-Dependent Resistance

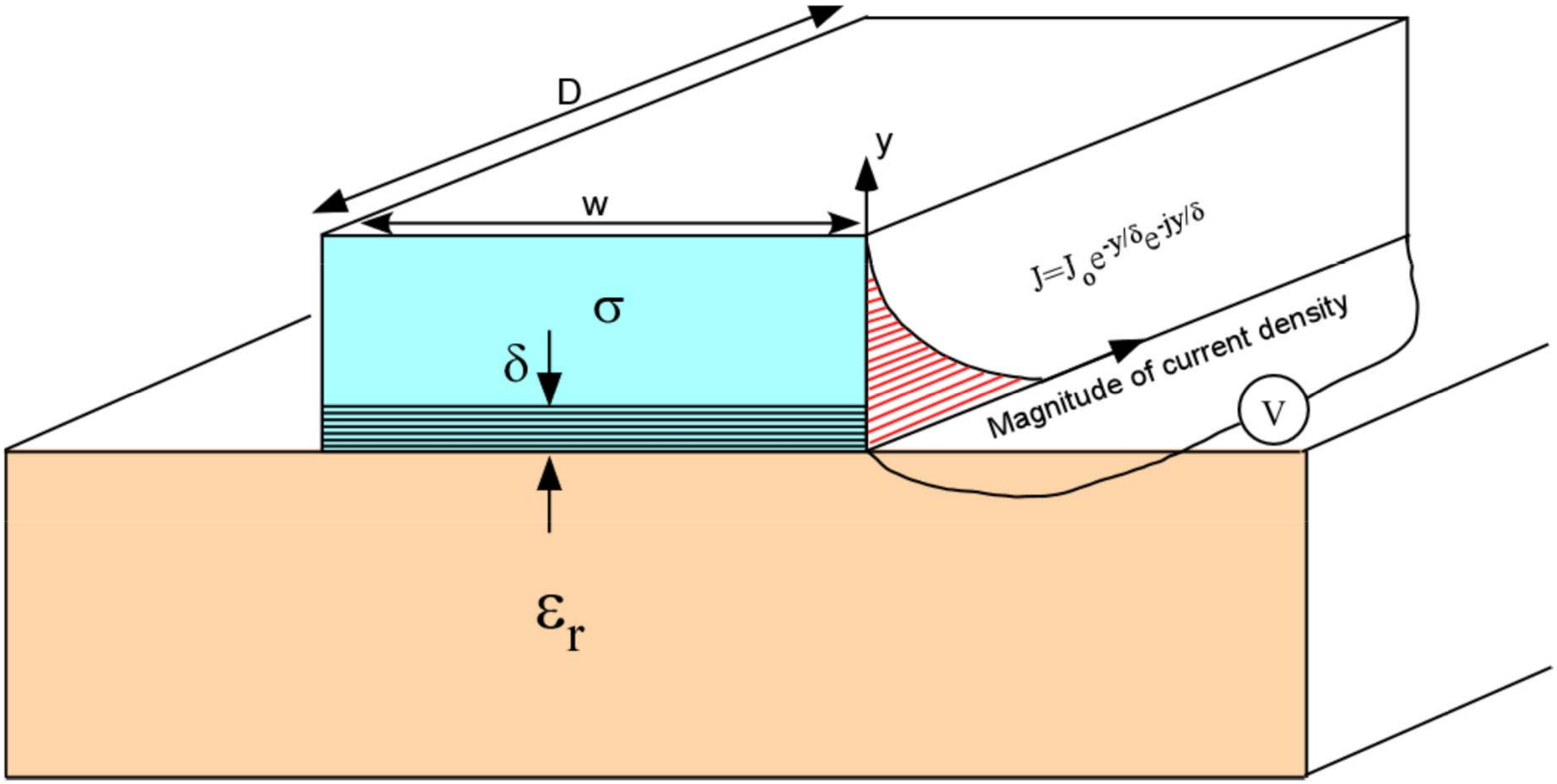


Reference Plane Current



$$R_{ac,ground} \approx \frac{l}{6h}\sqrt{\frac{\pi\mu f}{\sigma}}$$

Skin Effect in Microstrip



H. A. Wheeler, "Formulas for the skin effect," Proc. IRE, vol. 30, pp. 412-424,1942

Skin Effect in Microstrip

Current density varies as

$$J = J_o e^{-y/\delta} e^{-jy/\delta}$$

Note that the phase of the current density varies as a function of *y*

$$I = \int_0^\infty J_o w e^{-y/\delta} e^{-jy/\delta} dy = \frac{J_o w \delta}{1 + j}$$

$$\sigma E_o = J_o \Rightarrow E_o = \frac{J_o}{\sigma}$$

The voltage measured over a section of conductor of length *D* is:

$$V = E_o D = \frac{J_o D}{\sigma}$$

Skin Effect in Microstrip

The skin effect impedance is

$$Z_{skin} = \frac{V}{I} = \frac{J_o D}{\sigma} \frac{(1+j)}{J_o w \delta} = \frac{D}{w}(1+j)\sqrt{\pi f \mu \rho}$$

where $\rho = \dfrac{1}{\sigma}$ is the bulk resistivity of the conductor

$$Z_{skin} = R_{skin} + jX_{skin}$$

with

$$R_{skin} = X_{skin} = \frac{D}{w}\sqrt{\pi f \mu \sigma}$$

➔ Skin effect has reactive (inductive) component

Internal Inductance

The internal inductance can be calculated directly from the ac resistance

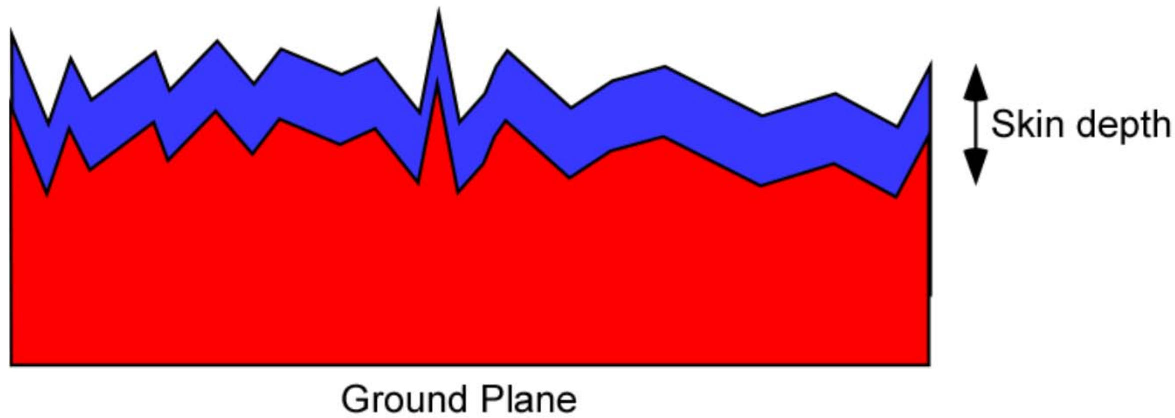
$$L_{\text{internal}} = \frac{R_{ac}}{\omega} = \frac{R_{skin}}{\omega}$$

➔ **Skin effect resistance goes up with frequency**

➔ **Skin effect inductance goes down with frequency**

Surface Roughness

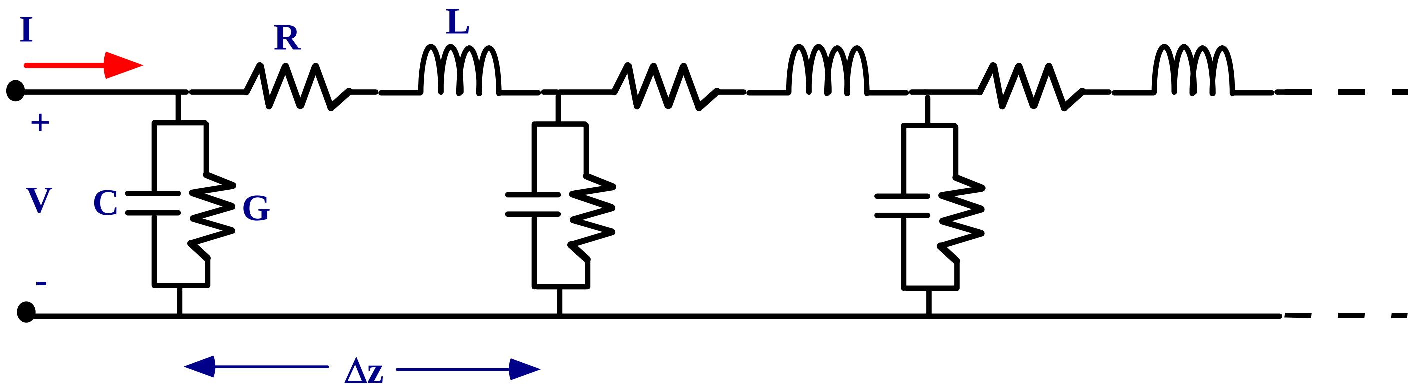
Copper surfaces are rough to facilitate adhesion to dielectric during PCB manufacturing



When the *tooth* height is comparable to the skin depth, roughness effects cannot be ignored

Surface roughness will increase ohmic losses

Lossy Transmission Line

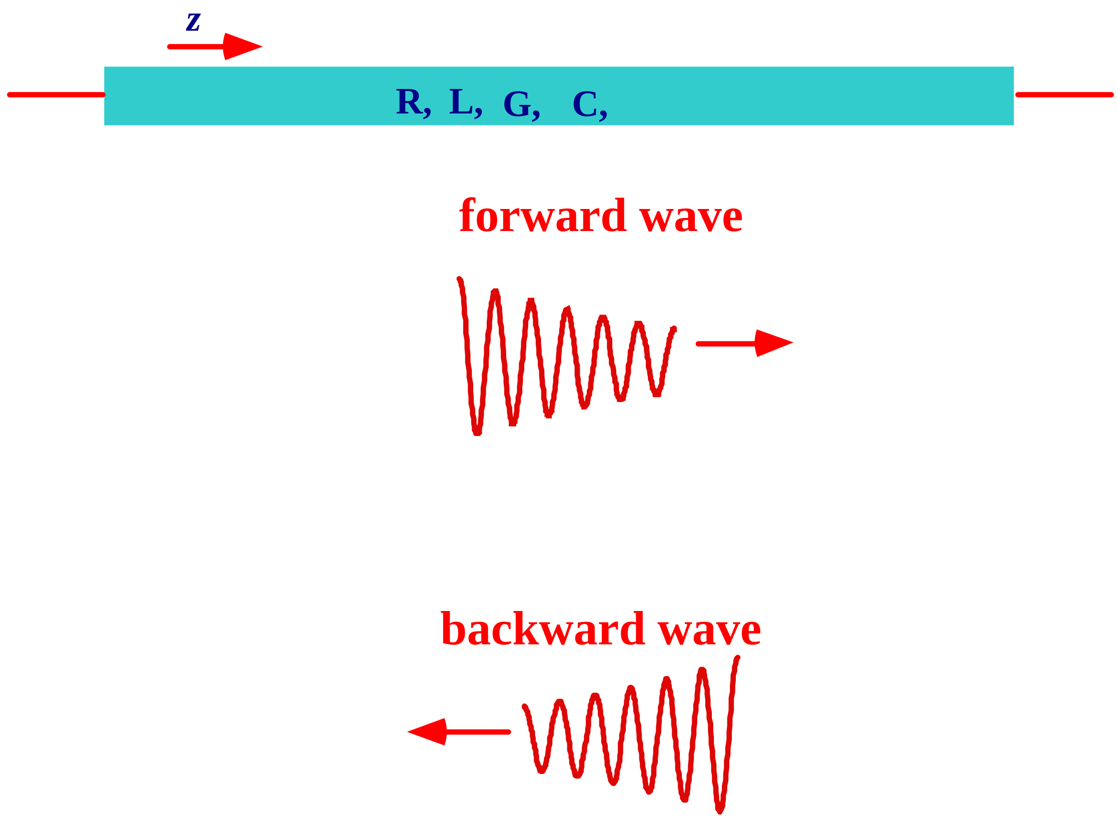


Telegraphers Equation

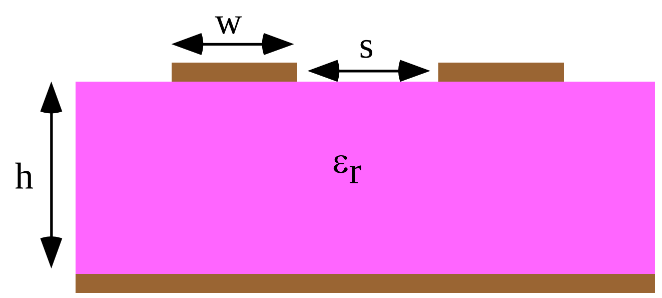
$$-\frac{\partial V}{\partial z} = (R + j\omega L)I = ZI$$

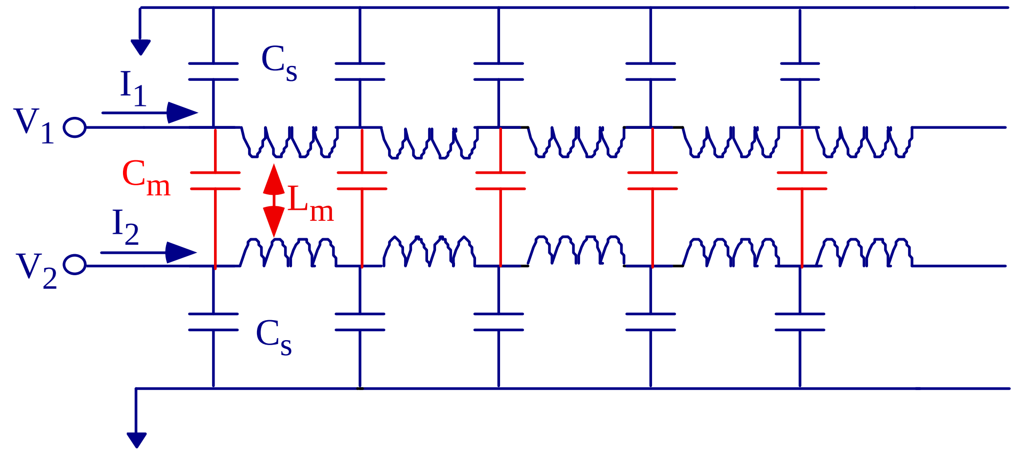
$$-\frac{\partial I}{\partial z} = (G + j\omega C)V = YV$$

Lossy Transmission Line

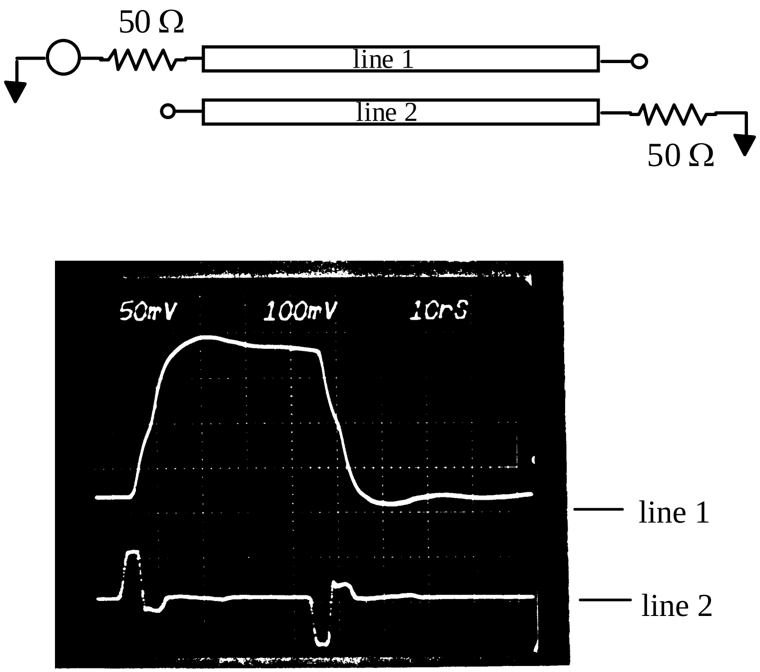


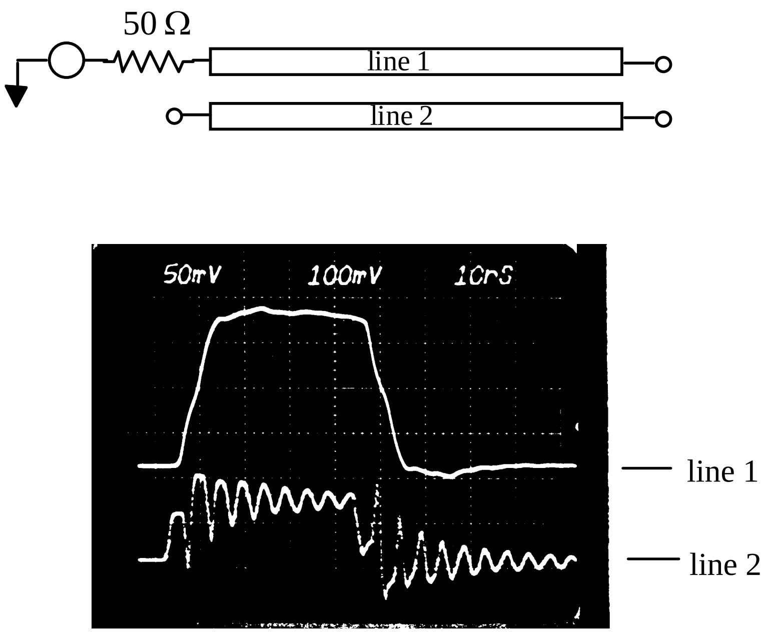
Coupled Lines and Crosstalk



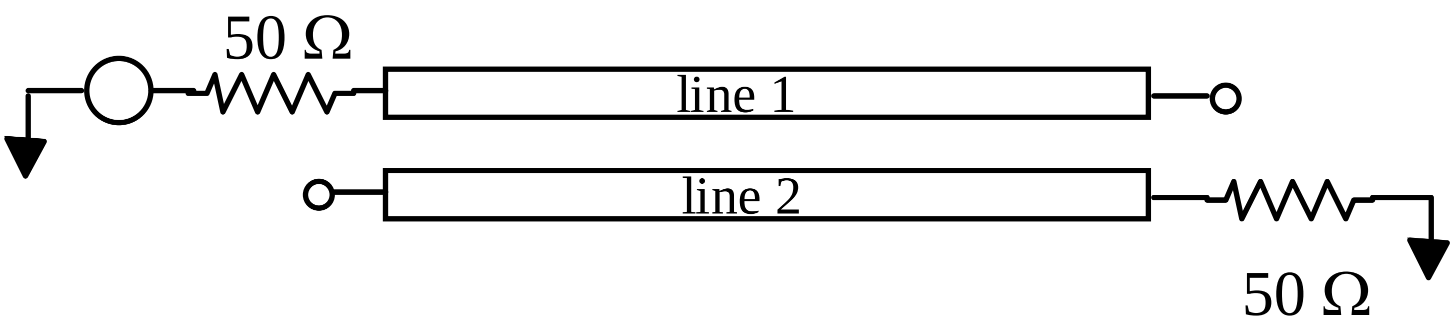


Crosstalk noise depends on termination

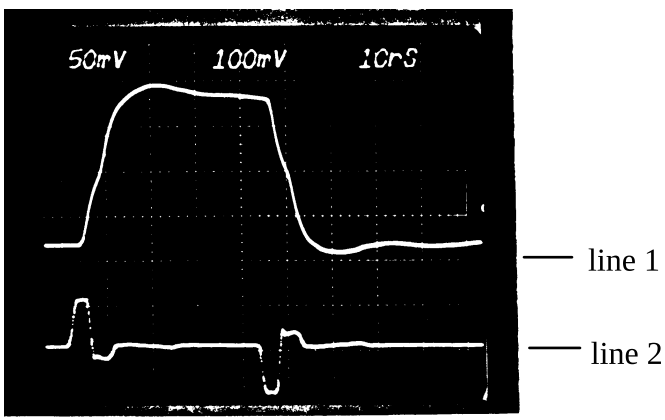




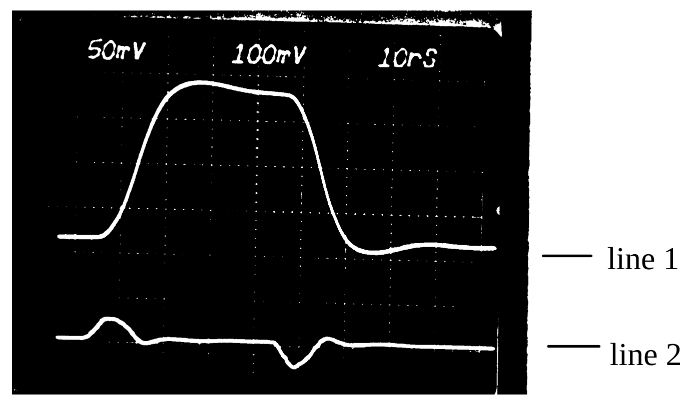
Crosstalk depends on signal rise time



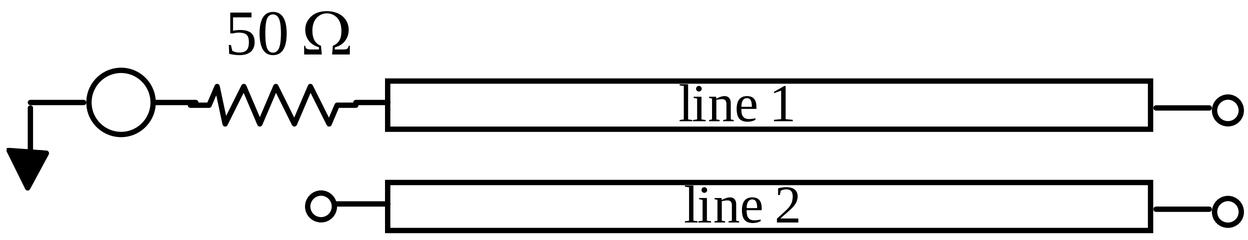
t_r = 1 ns



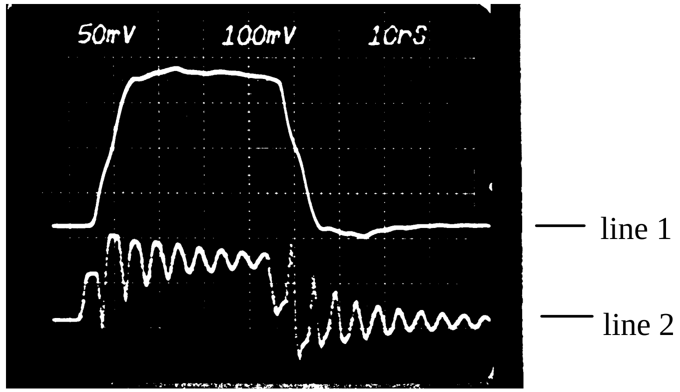
t_r = 7 ns



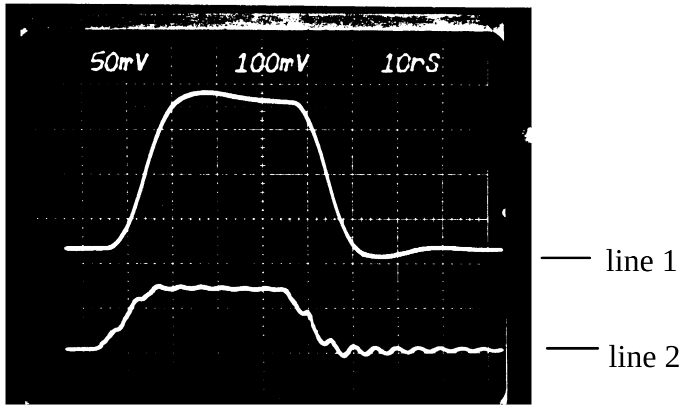
Crosstalk depends on signal rise time

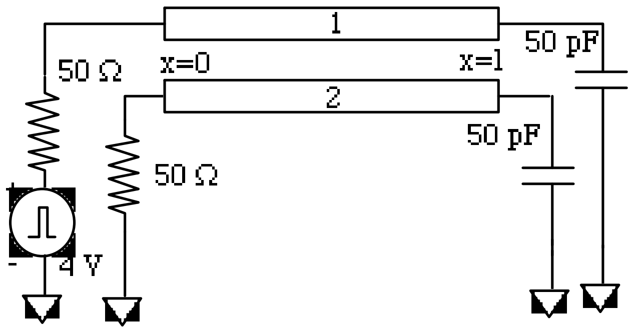


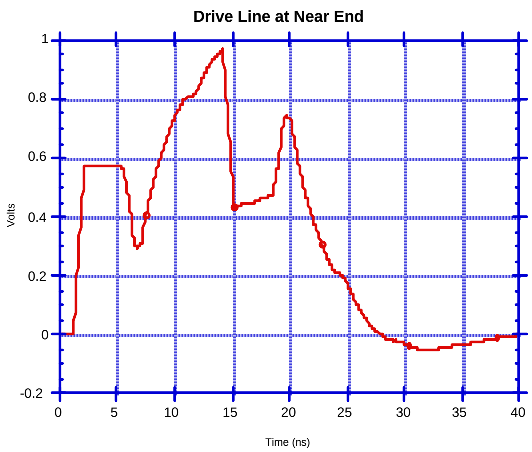
t_r = 1 ns



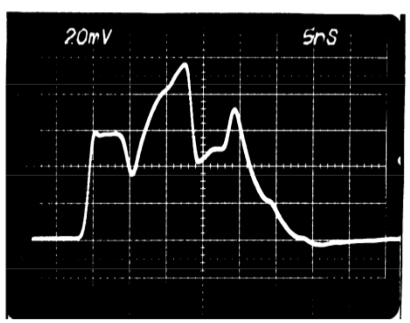
t_r = 7 ns

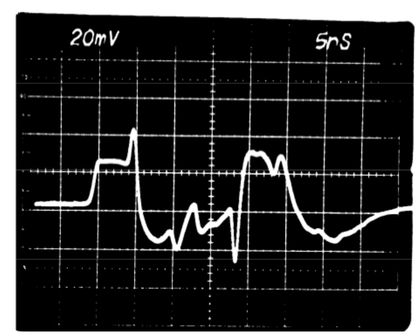



1
x=0
x=l
50 pF
2
50 Ω
50 pF
50 Ω
4 V

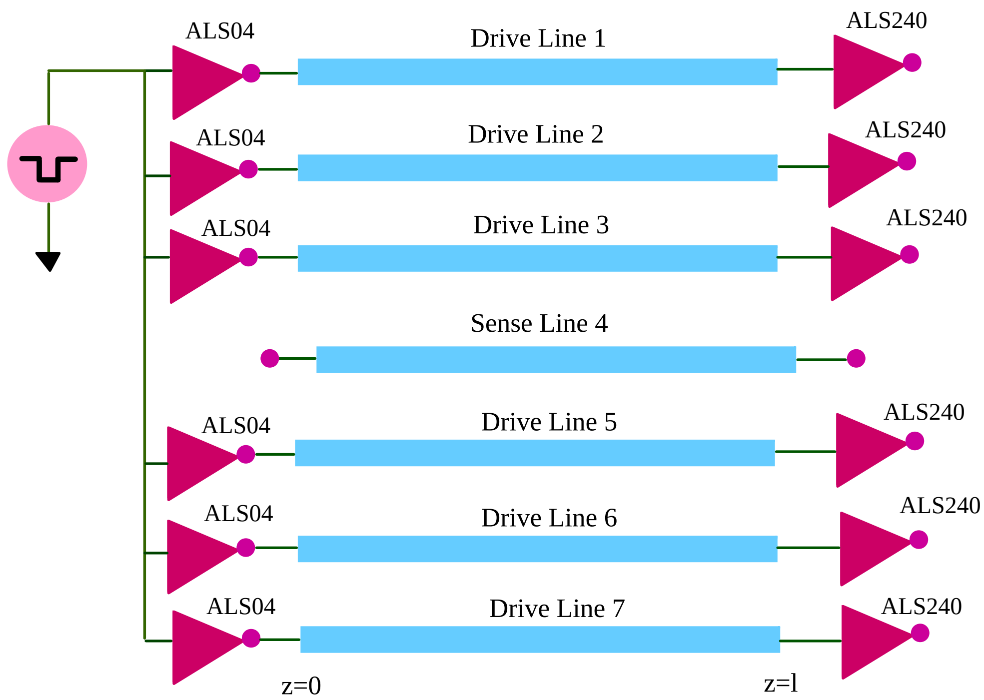

Drive Line at Near End
Volts
Time (ns)
1
0.8
0.6
0.4
0.2
0
-0.2
0
5
10
15
20
25
30
35
40


Sense Line at Near End
Volts
Time (ns)
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
0
5
10
15
20
25
30
35
40


20mV
5nS


20mV
5nS

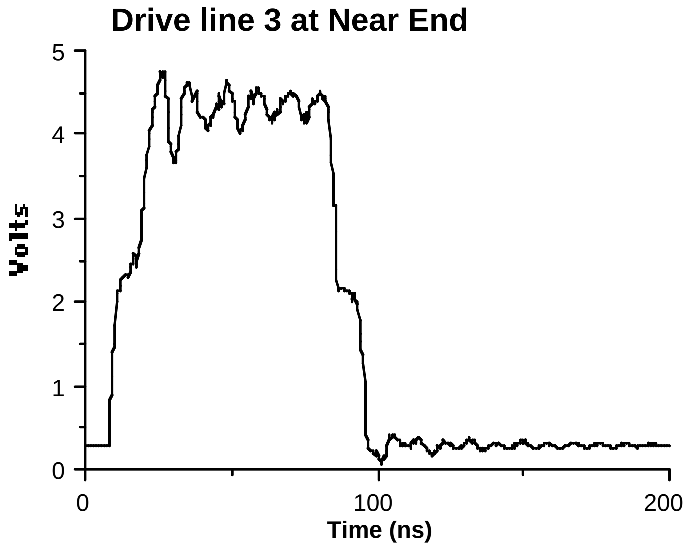
7-Line Coupled-Microstrip System

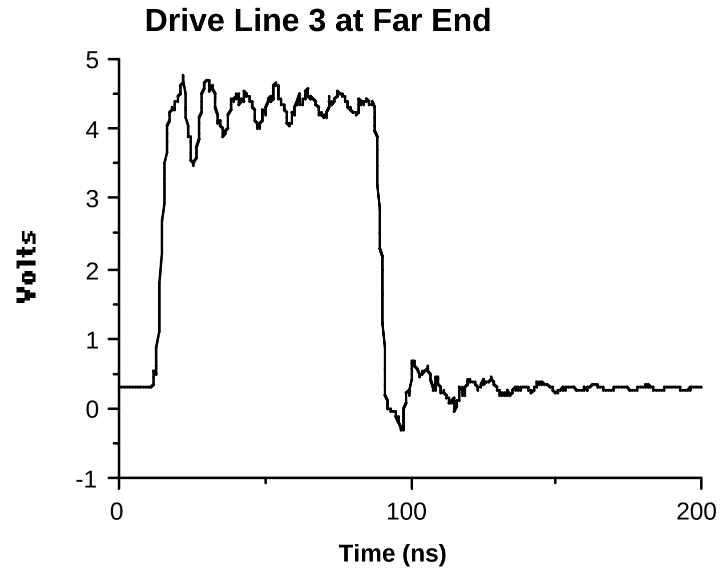


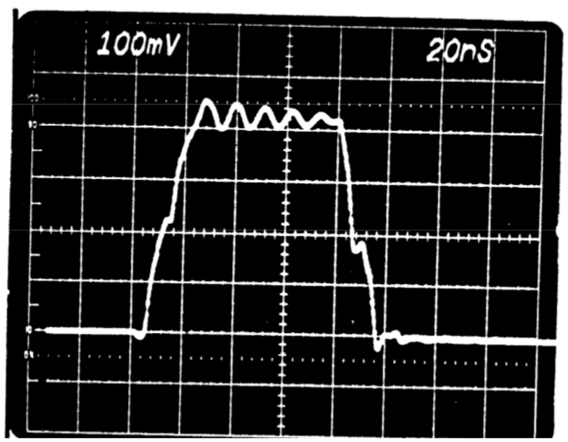
$$L_s = 312 \text{ nH/m}; \quad C_s = 100 \text{ pF/m};$$

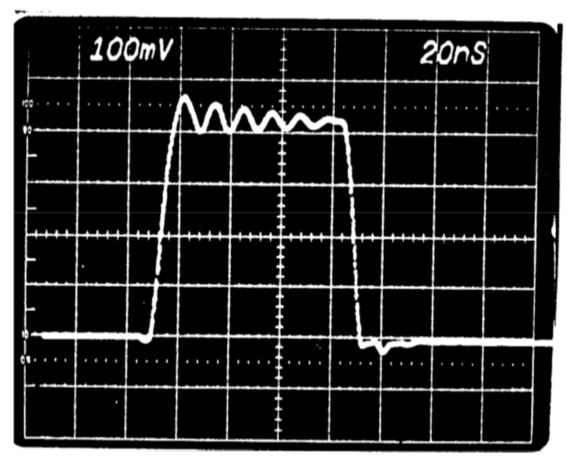
$$L_m = 85 \text{ nH/m}; \quad C_m = 12 \text{ pF/m}.$$

Drive Line 3

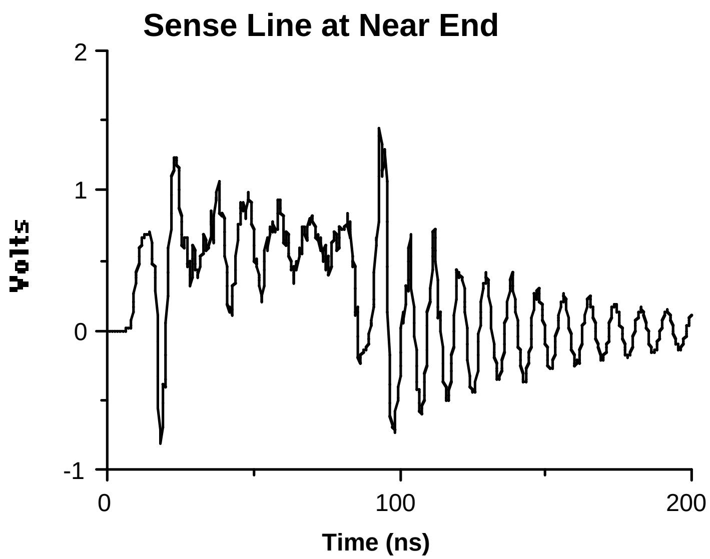

Drive line 3 at Near End
Volts
Time (ns)
0
1
2
3
4
5
0
100
200


Drive Line 3 at Far End
Volts
Time (ns)
-1
0
1
2
3
4
5
0
100
200

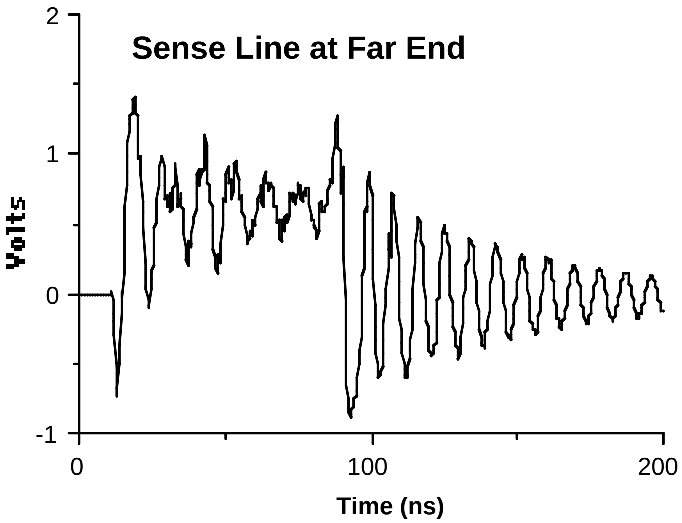

100mV
20nS


100mV
20nS

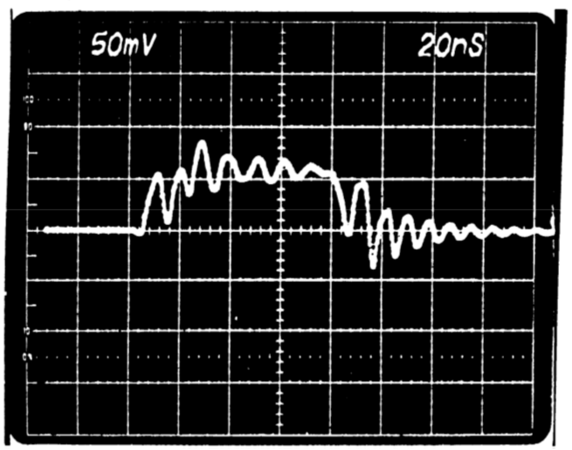
Sense Line



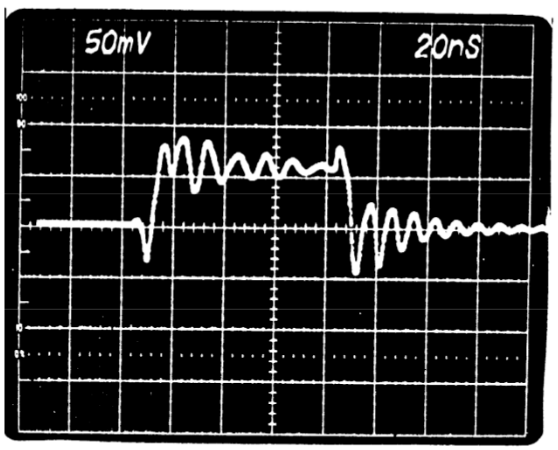
Sense Line at Near End
2
1
0
-1
Volts
0
100
200
Time (ns)



Sense Line at Far End
2
1
0
-1
Volts
0
100
200
Time (ns)

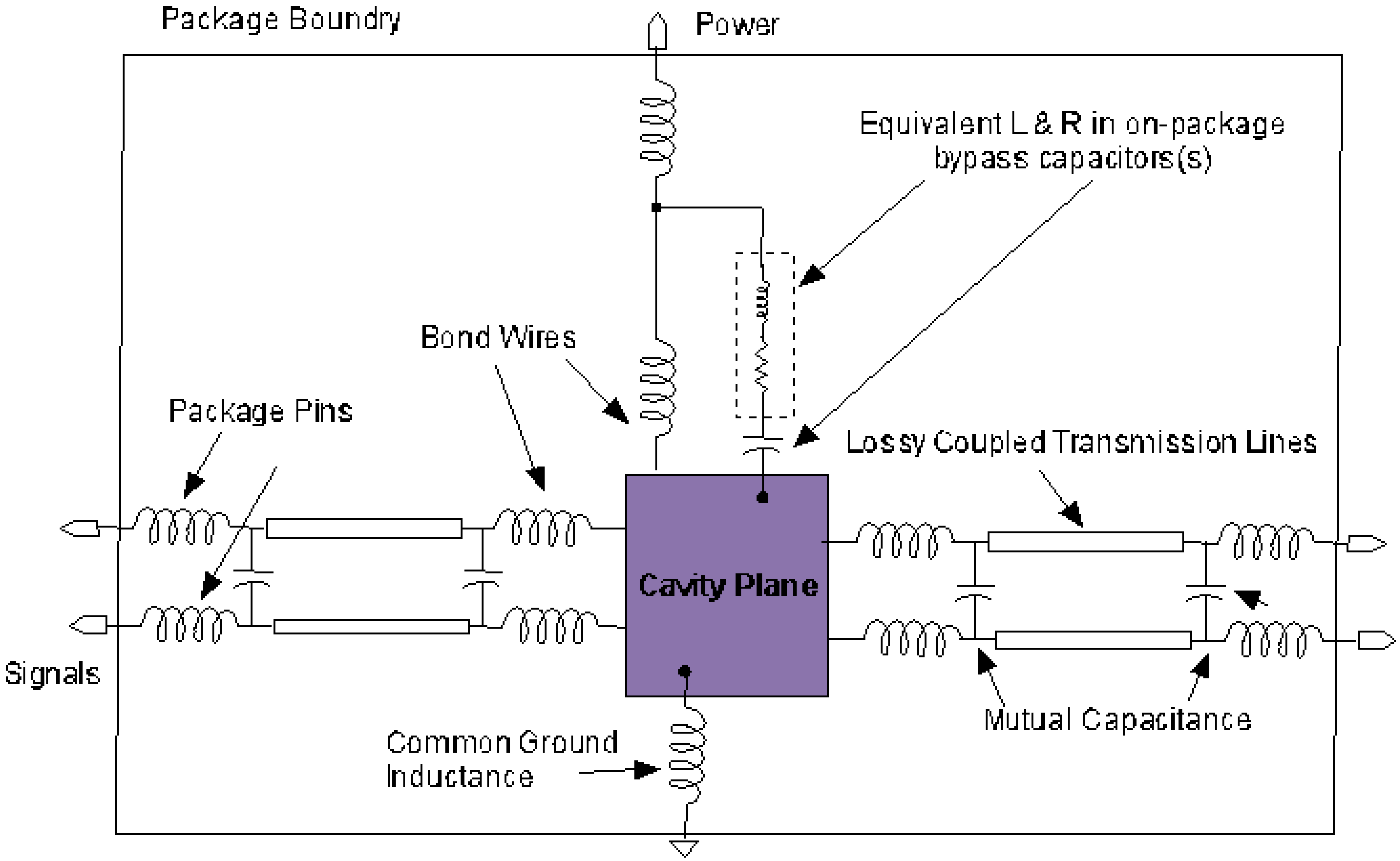


50mV
20nS

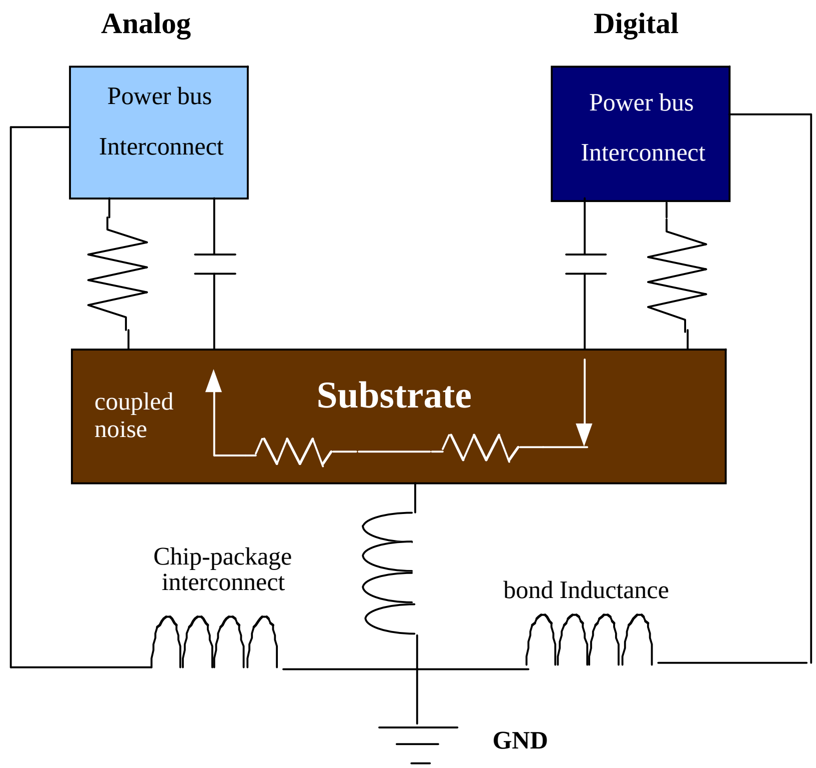


50mV
20nS

IC on Package



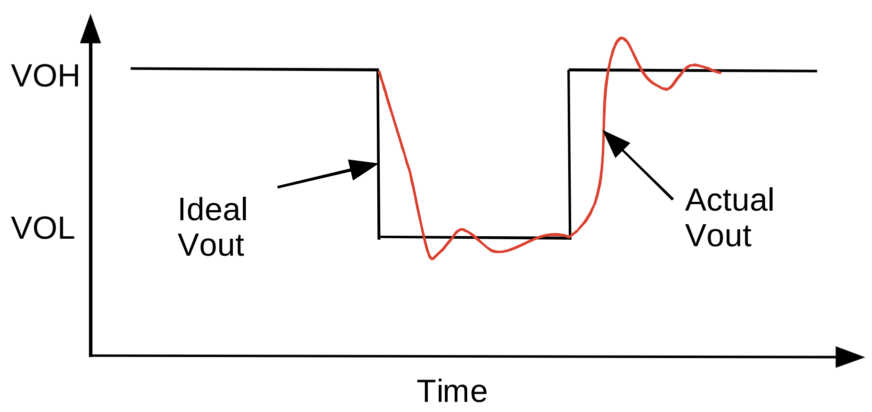
Mixed Signal Noise



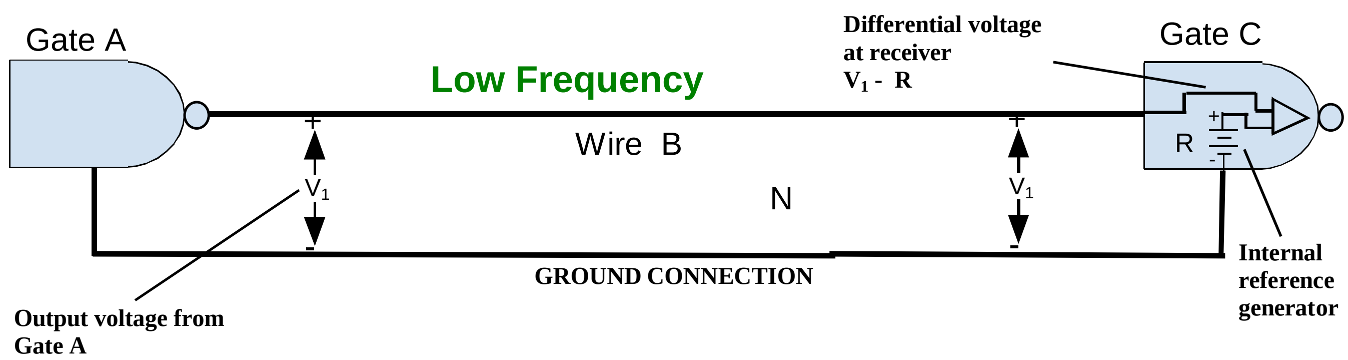
- Simultaneous switching and inductance (L_{eff})
- L_{eff} is f(current magnitude and direction)
- Interactions between noise generated by power/ground and signal paths

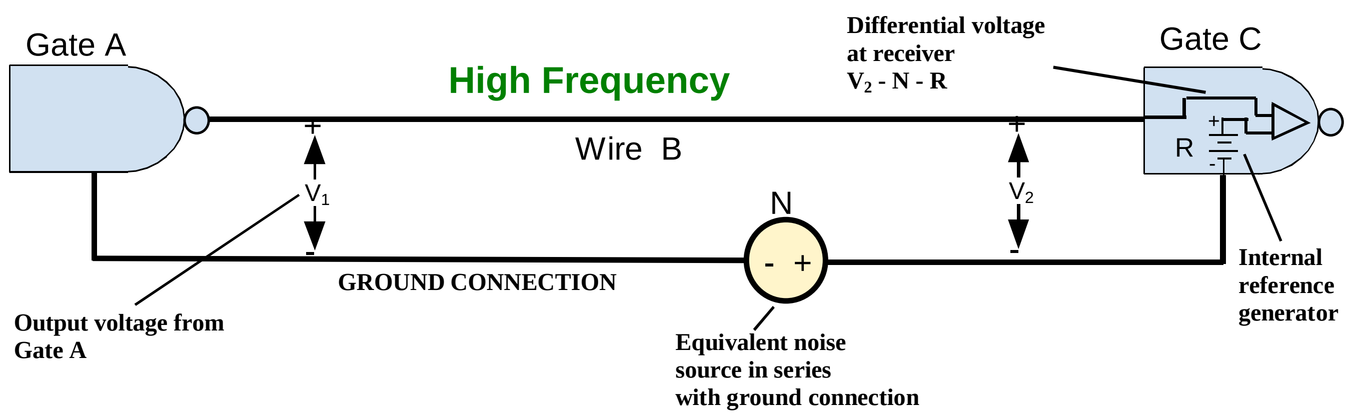
Power-Supply Noise

- Power-supply-level fluctuations
- Delta-I noise
- Simultaneous switching noise (SSN)
- Ground bounce



Power Distribution Problem

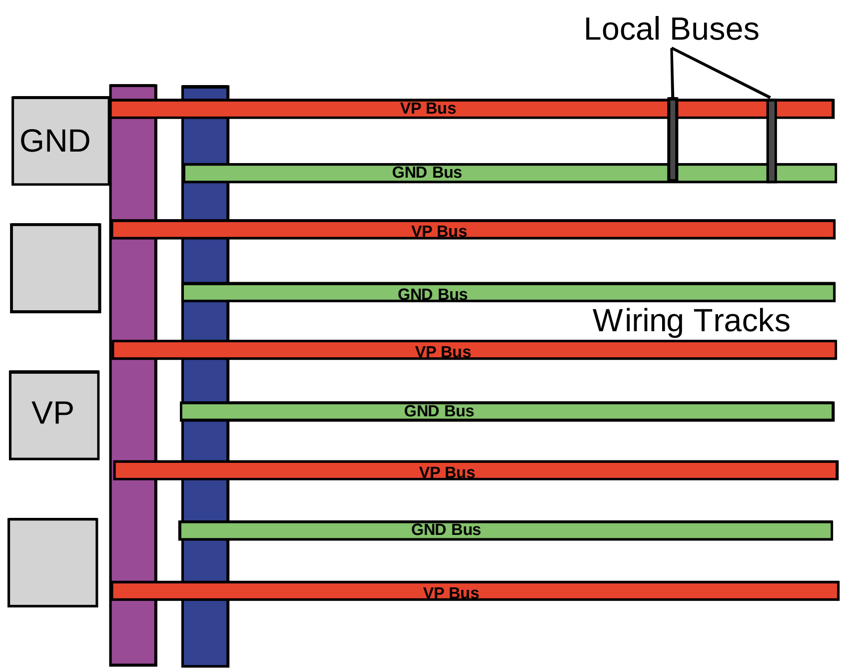




At high frequencies, Wire B is a transmission line and ground connection is no longer the reference voltage

On-Chip Power and Ground Distribution

- **Distribution Network for Peripheral Bonding**
  - Power and ground are brought onto the chip via bond pads located along the four edges
  - Metal buses provide routing from the edges to the remainder of the chip



Intersymbol Interference (ISI)

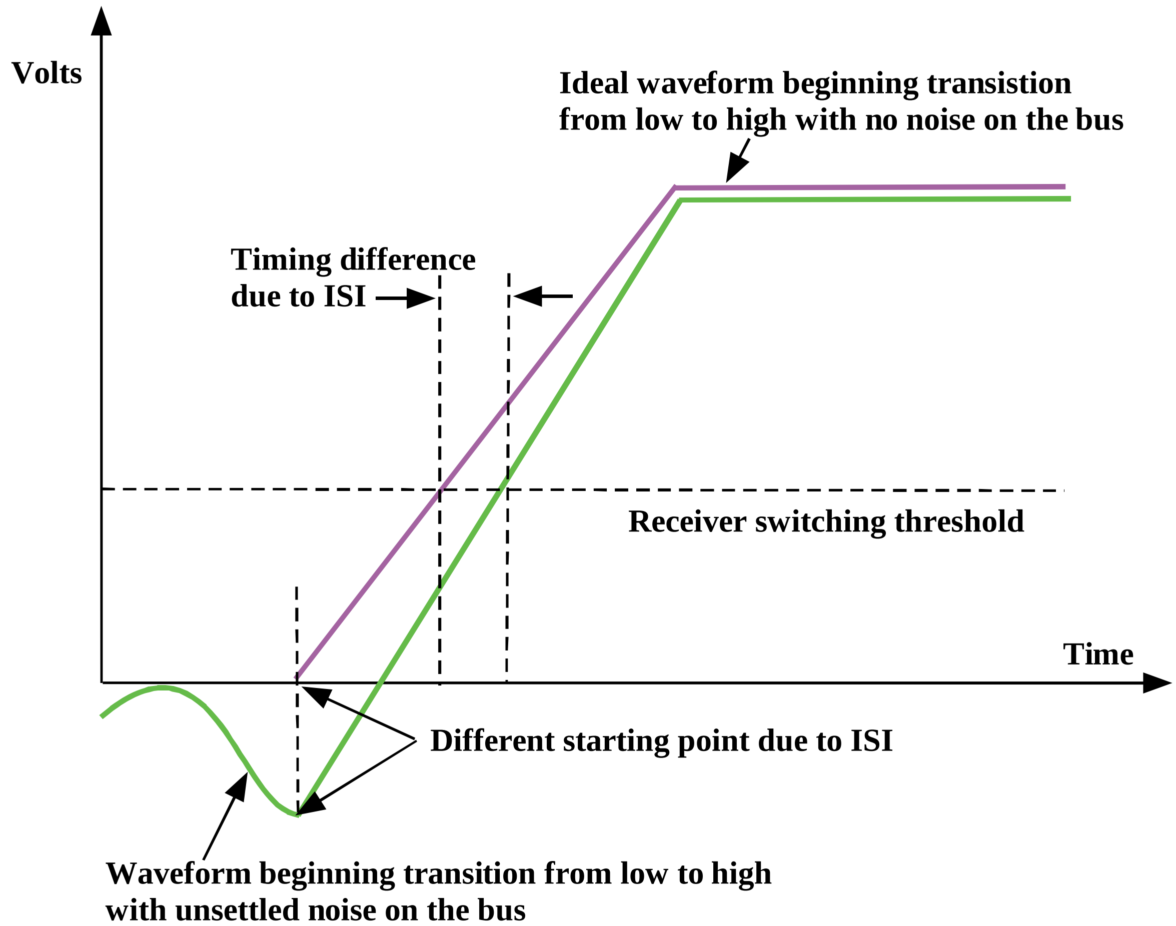
- **Signal launched on a transmission line can be affected by previous signals as result of reflections**

- **ISI can be a major concern especially if the signal delay is smaller than twice the time of flight**

- **ISI can have devastating effects**

- **Noise must be allowed to settled before next signal is sent**

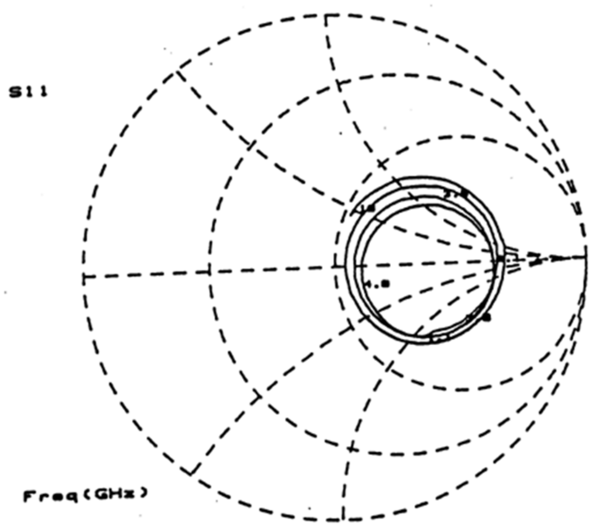
Intersymbol Interference



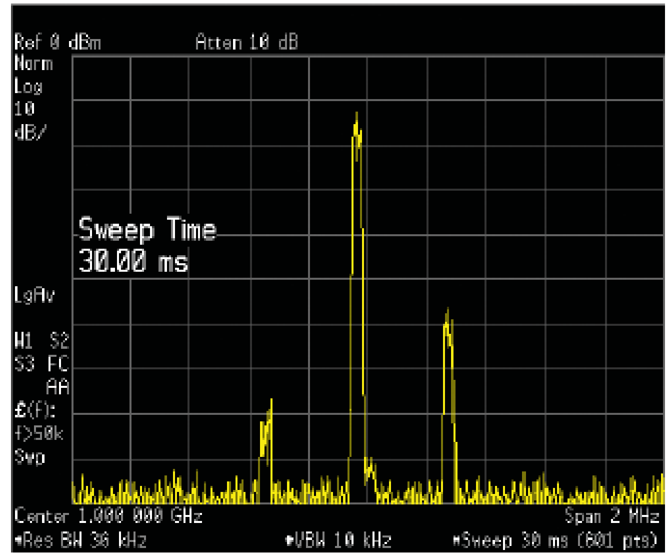
Minimizing ISI

- **Minimize reflections on the bus by avoiding impedance discontinuities**
- **Minimize stub lengths and large parasitics from package sockets or connectors**
- **Keep interconnects as short as possible (minimize delay)**
- **Minimize crosstalk effects**

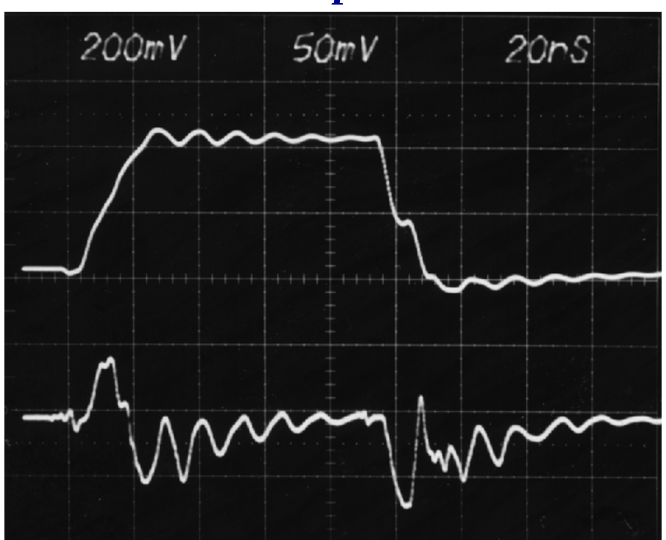
Measurements



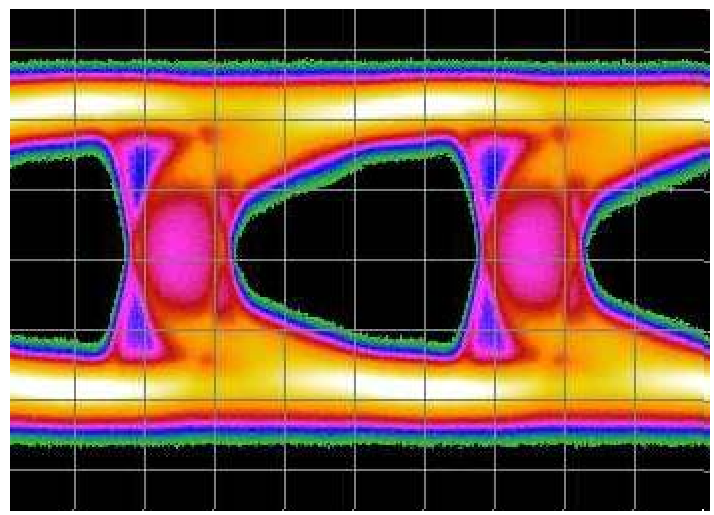
VNA: S-parameter



Spectrum Analyzer



Time-domain simulation



Eye diagram

Jitter Definition

Jitter is difference in time of when something was ideally to occur and when it actually did occur.

Some devices specify the amount of marginal jitter and total jitter that it can take to operate correctly. If the cable adds more jitter than the receiver's allowed marginal jitter and total jitter the signal will not be received correctly. In this case the jitter is measured as in the below diagram

- **Timing uncertainties in digital transmission systems**
- **Utmost importance because timing uncertainties cause bit errors**
- **There are different types of jitter**

Jitter Characteristics

- Jitter is a signal timing deviation referenced to a recovered clock from the recovered bit stream

- Measured in Unit Intervals and captured visually with eye diagrams

- Two types of jitter
  - Deterministic (non Gaussian)
  - Random

- The total jitter (TJ) is the sum of the random (RJ) and deterministic jitter(DJ)

Types of Jitter

- Deterministic Jitter (DDJ)
  - Data-Dependent Jitter (DDJ)
  - Periodic Jitter (PJ)
  - Bounded Uncorrelated Jitter (BUJ)

- Random Jitter (RJ)
  - Gaussian Jitter
  - $f^{-\alpha}$ Higher-Order Jitter

Jitter Effects

Bandwidth Limitations

- Cause intersymbol interference (ISI)
- ISI occurs if time required by signal to completely charge is longer than bit interval
- Amount of ISI is function of channel and data content of signal

Oscillator Phase Noise

- Present in reference clocks or high-speed clocks
- In PLL based clocks, phase noise can be amplified

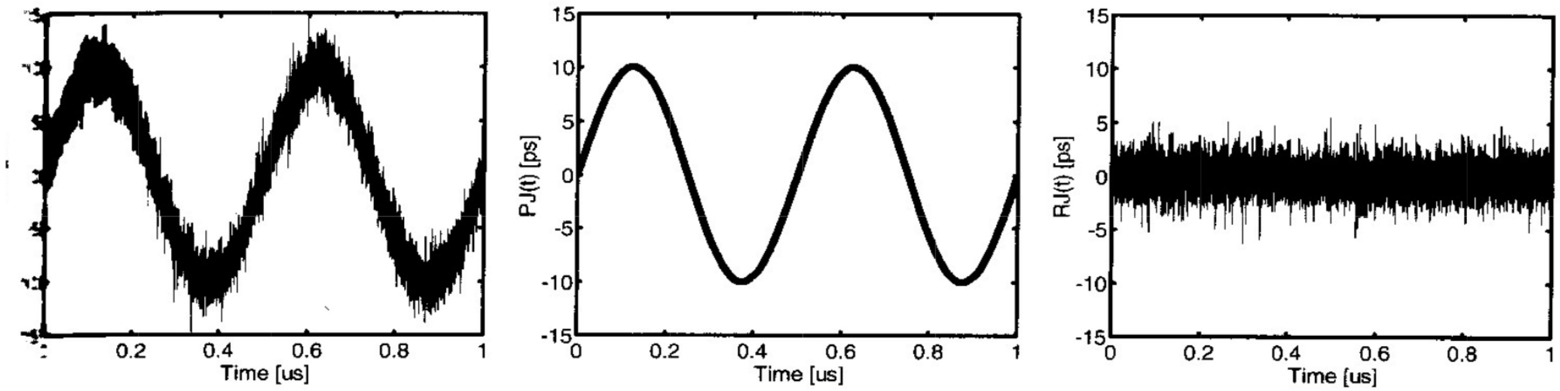
Jitter Statistics

- Most common way to look at jitter is in statistical domain
- Because one can observe jitter histograms directly on oscilloscopes
- No instruments to measure jitter time waveform or frequency spectrum directly

Jitter Histograms and Probability Density Functions (PDF)

- Built directly from time waveforms
- Frequency information is lost
- Peak-to-peak value depends on observation time

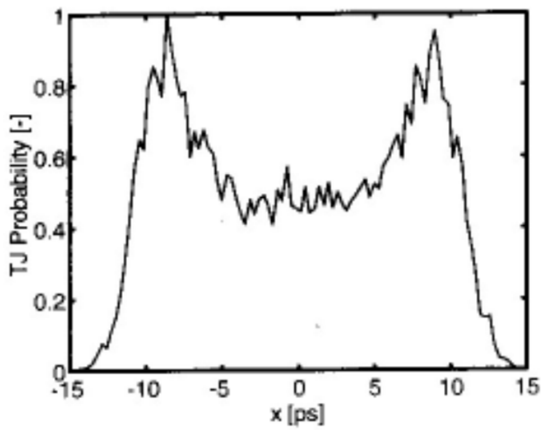
Total Jitter Time Waveform

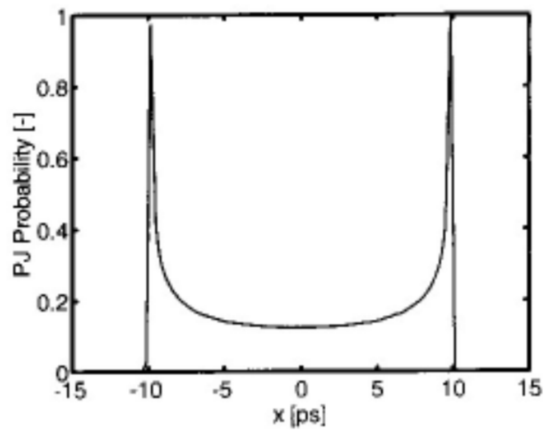


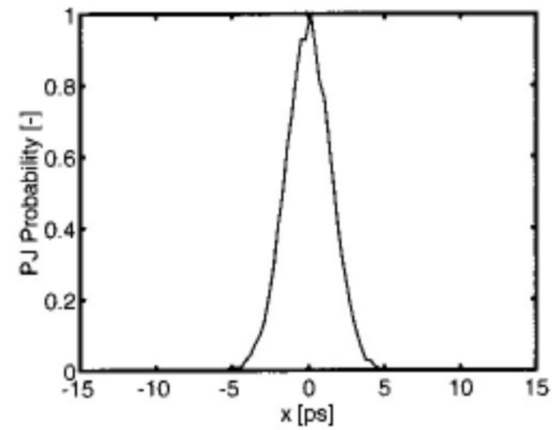
$$TJ(t) = PJ(t) + RJ(t)$$

The total jitter waveform is the sum of individual components

Jitter Statistics





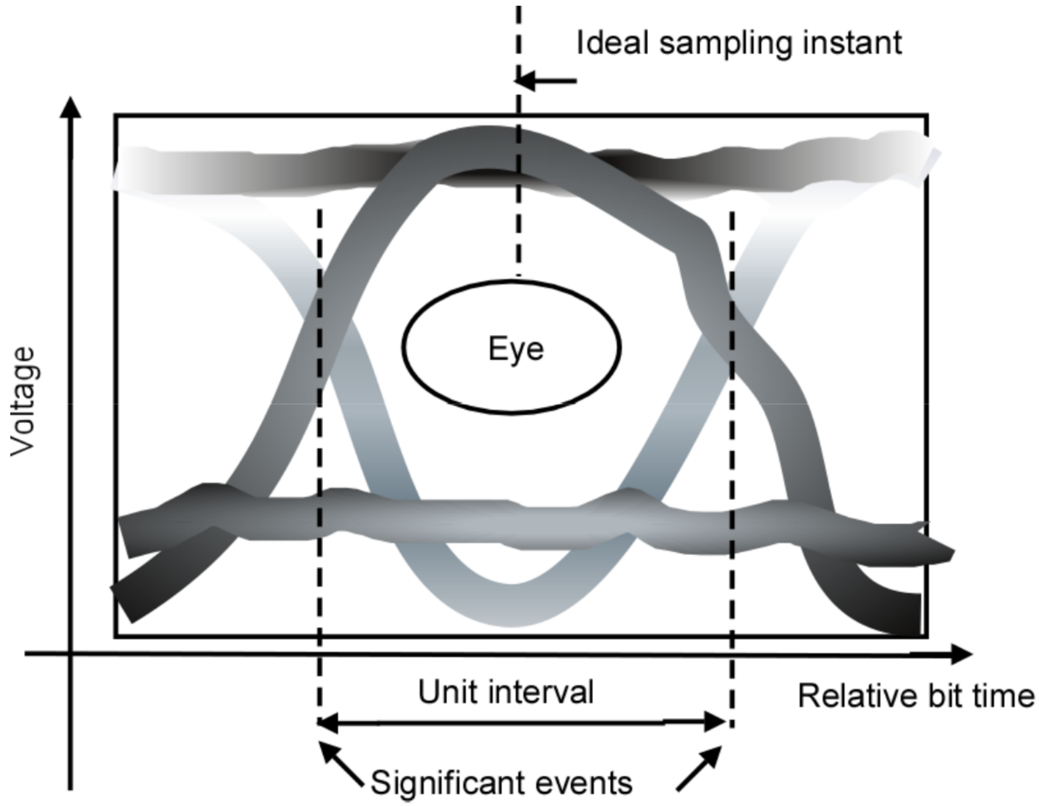


$$TJ(x) \quad = \quad PJ(x) \quad * \quad RJ(x)$$

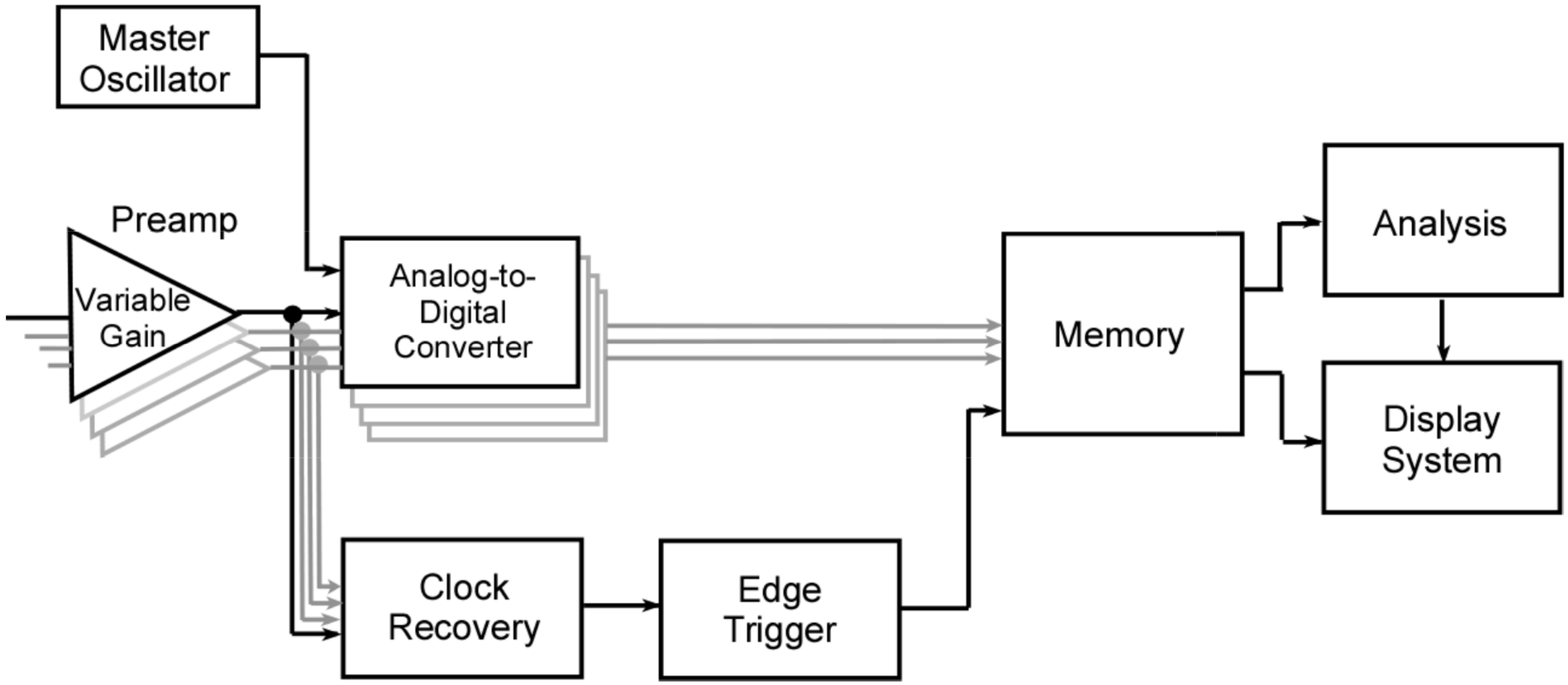
The total jitter PDF is the convolution of individual components

Eye Diagram

An eye diagram is a time-folded representation of a signal that carries digital information

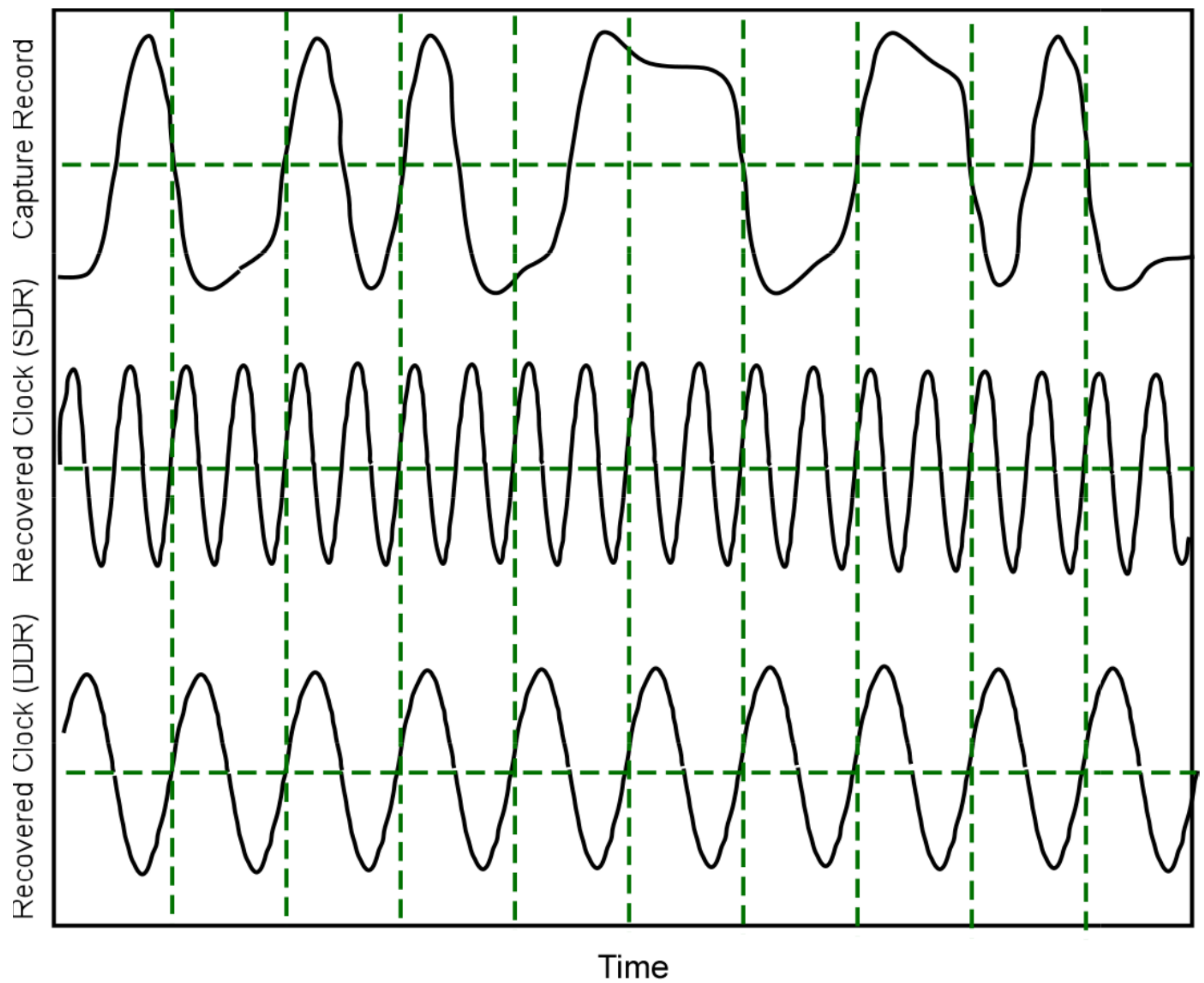


Eye Diagram Construction

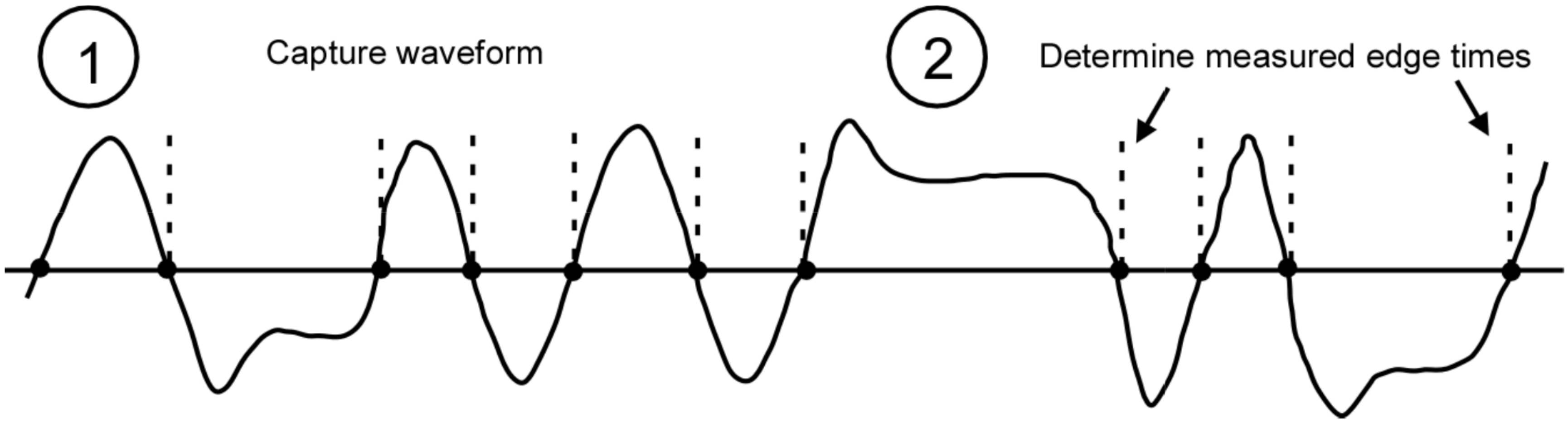


Eye diagram construction in real-time oscilloscope is based on hardware clock recovery and trigger circuitry

Eye Diagram Construction



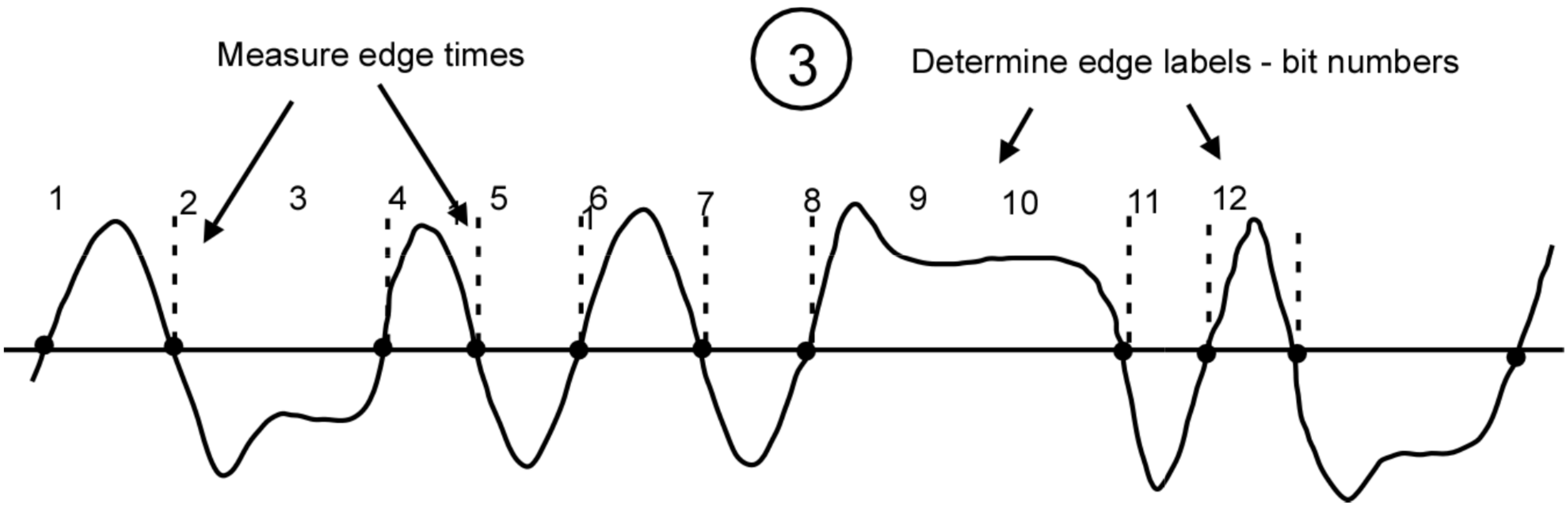
Eye Diagram Construction



1. Capture of the Waveform Record

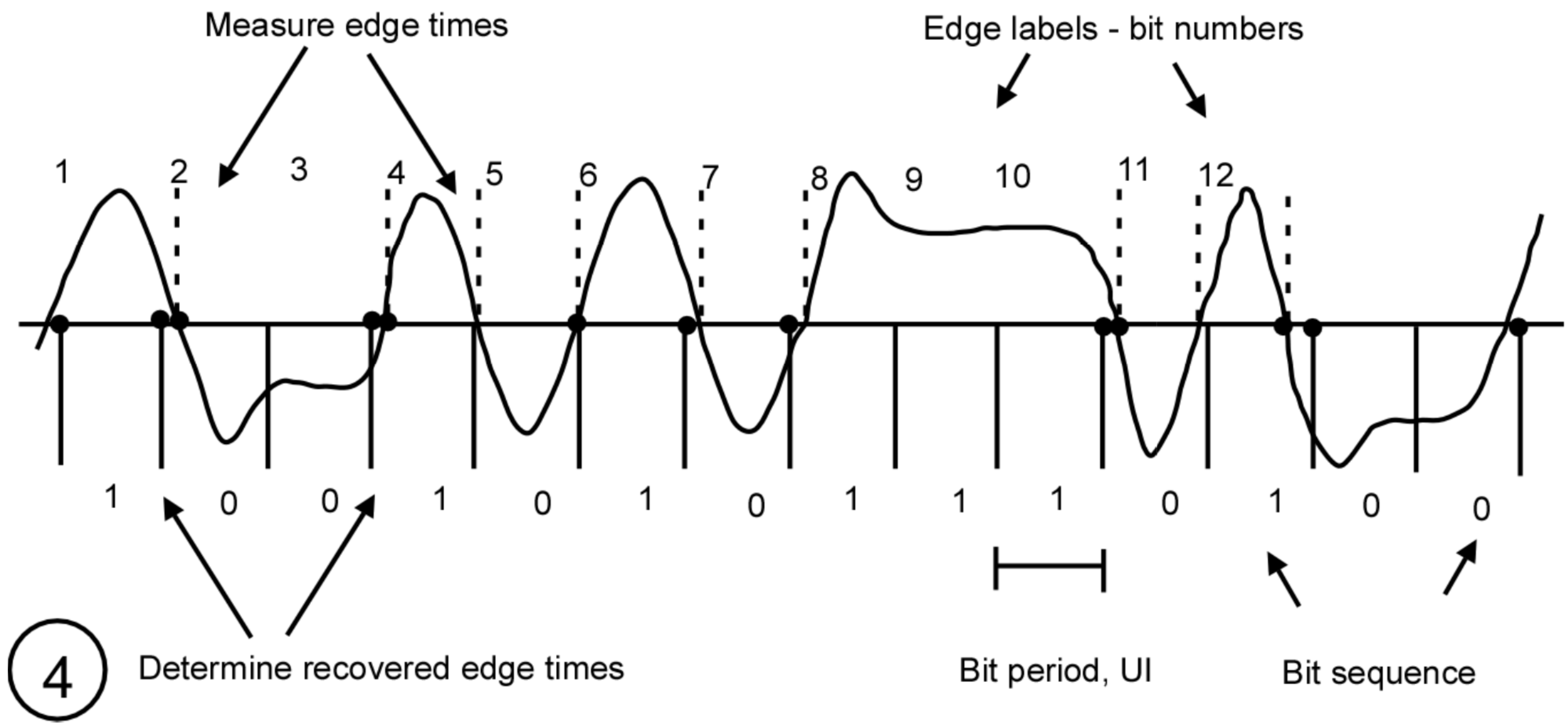
2. Determine the Edge Times

Eye Diagram Construction



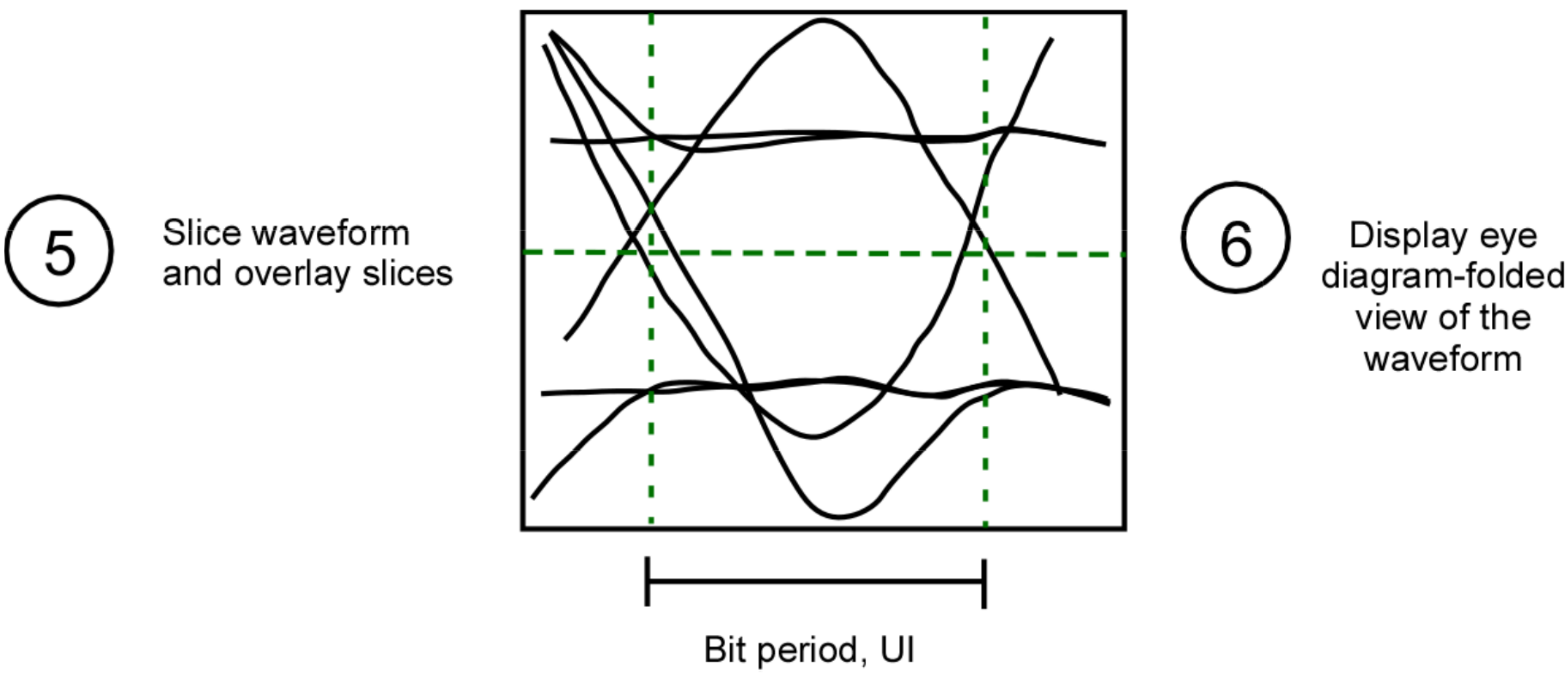
3. Determine the Bit Labels

Eye Diagram Construction



4. Clock Recovery

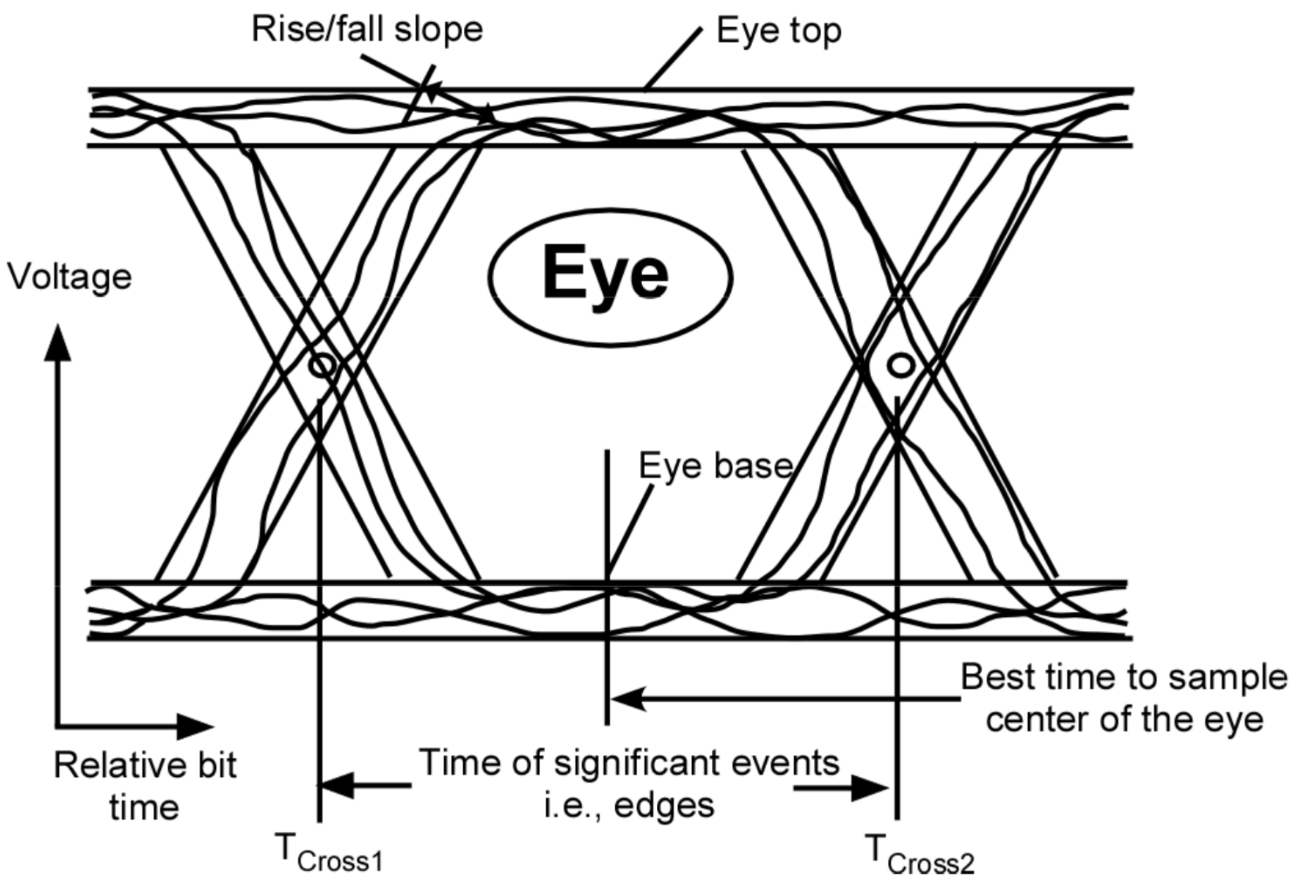
Eye Diagram Construction



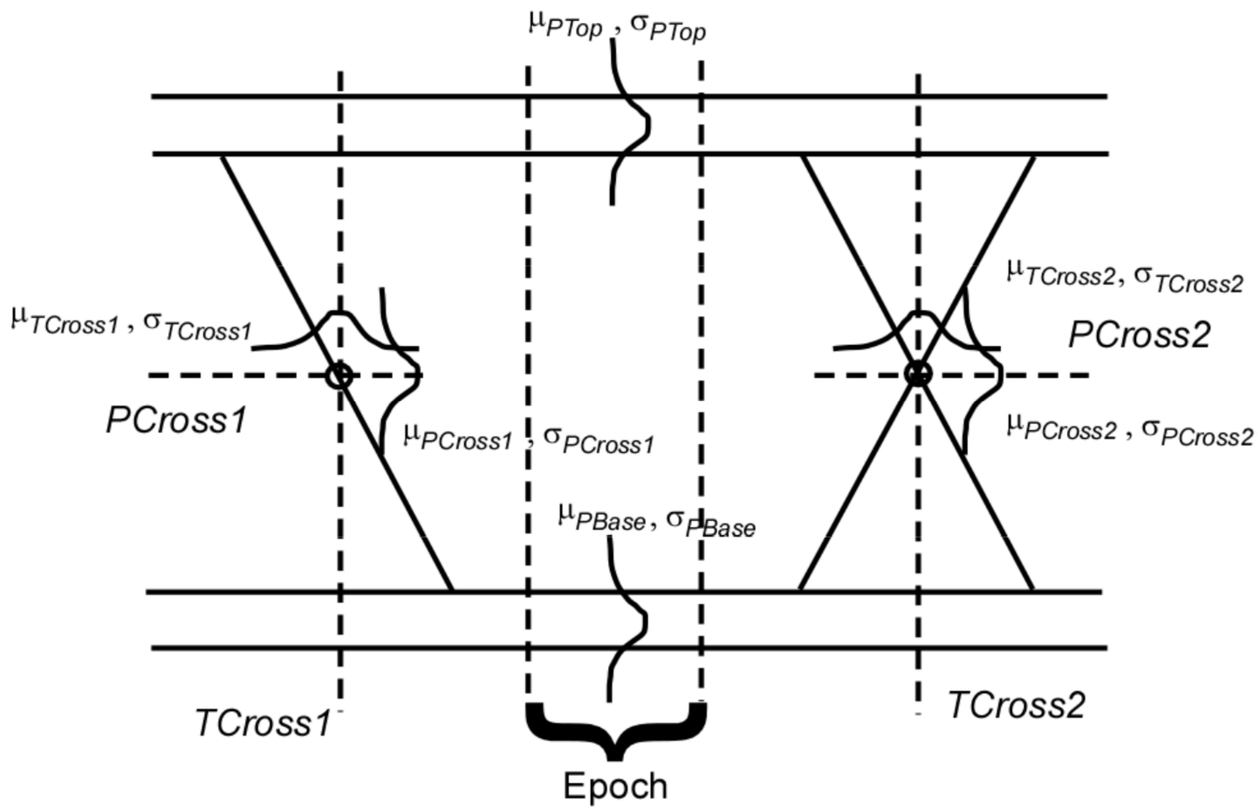
5. Slice Overlay

6. Display

Eye Diagram Measurements



Reference Levels



Eye Height

Eye Height is the measuremnt of the eye height in volts

$$Eye\ Height = \left(\mu_{PTop} - 3\sigma_{PTop}\right) - \left(\mu_{PBase} + 3\sigma_{PBase}\right)$$

μ_{PTop} : mean value of eye top

σ_{PTop} : standard deviation of eye top

μ_{PBase} : mean value of eye base

σ_{PBase} : standard deviation of eye base

Eye Width

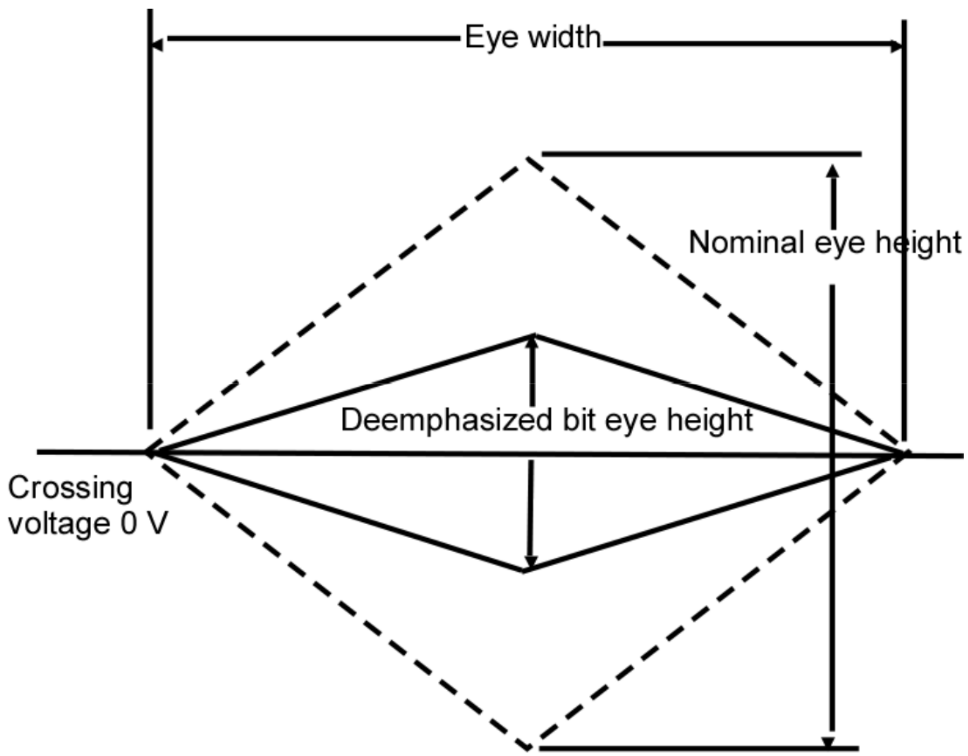
Eye Width **is the measuremnt of the eye width in seconds**

$$Eye\,Width = \left(\mu_{TCross2} - 3\sigma_{TCross2}\right) - \left(\mu_{TCross1} + 3\sigma_{TCross1}\right)$$

Crossing percent **measurement is the eye crossing point expressed as a percentage of the eye height**

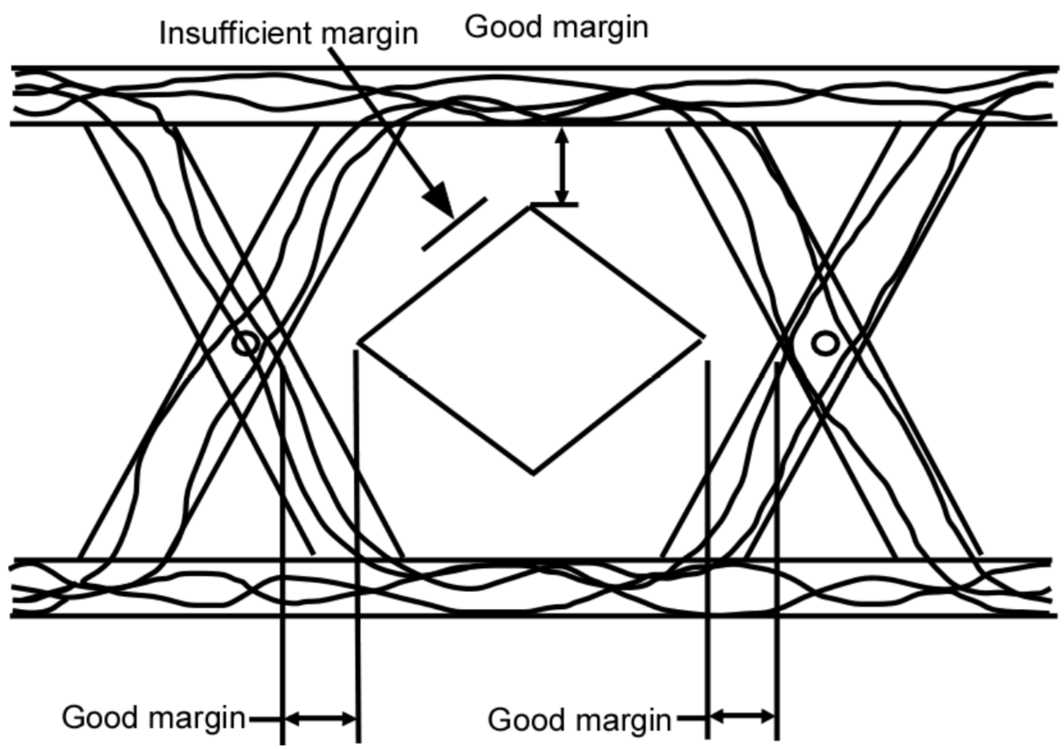
$$\text{Crossing Percent} = \frac{\left(\mu_{PCross1} - \mu_{PBase}\right)}{\left(\mu_{PTop} - \mu_{PBase}\right)} \times 100\%$$

Eye Diagram Specifications



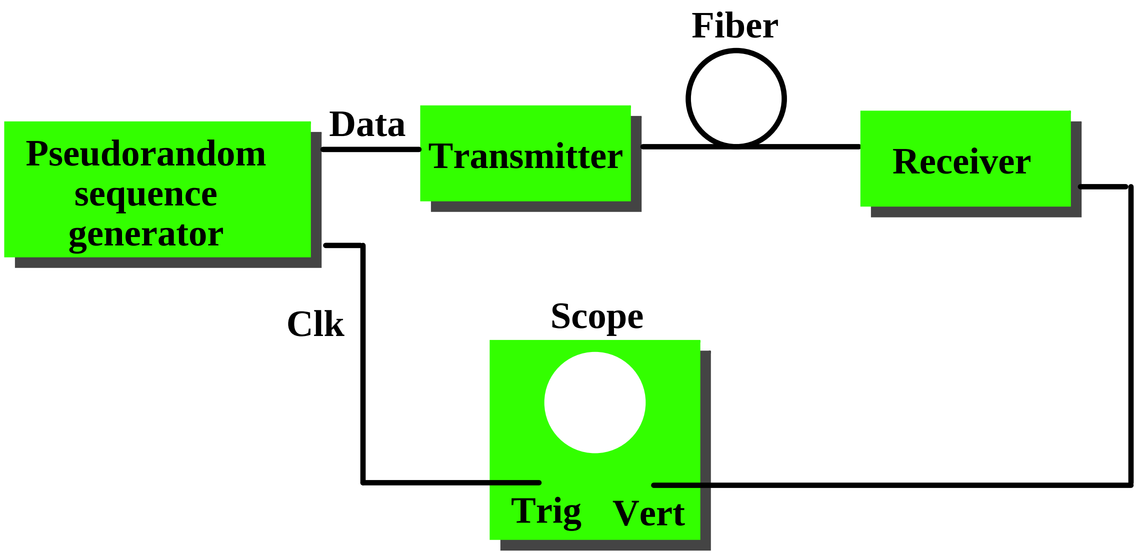
PCI Express 2.0 eye diagram specification for full and deemphasized signals

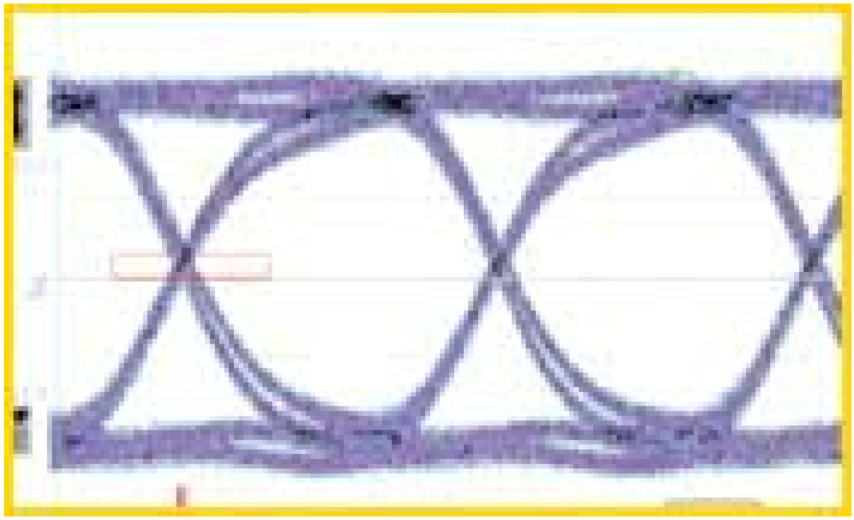
Margin Testing



Eye diagram with low margin

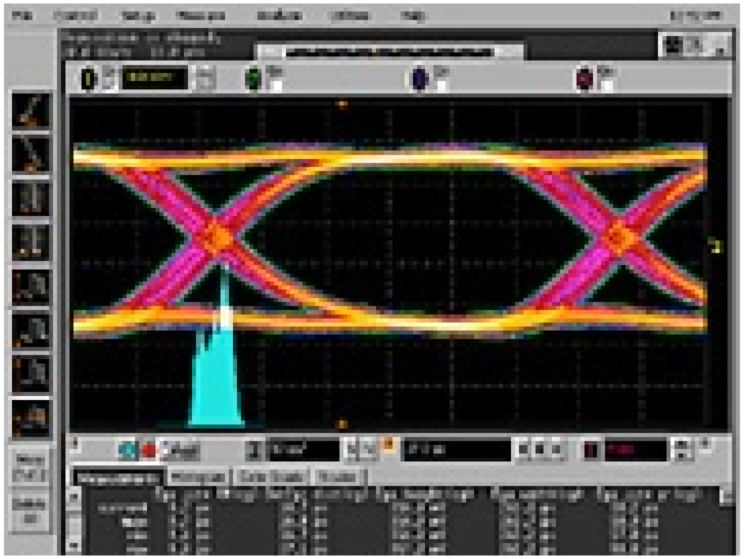
Eye Pattern Analysis

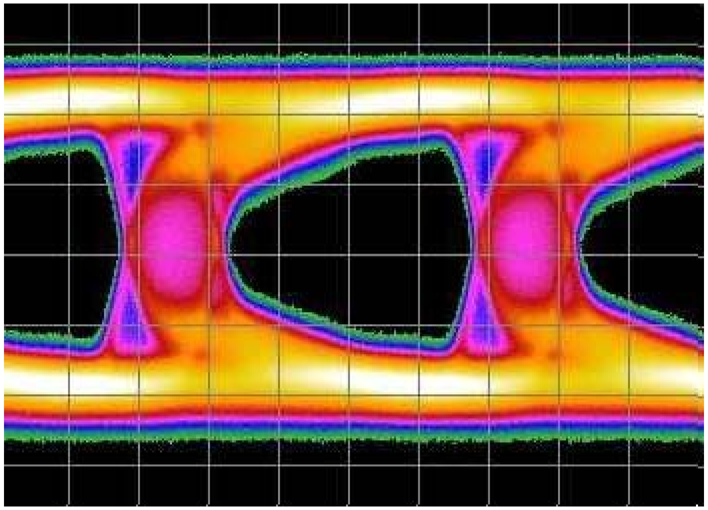




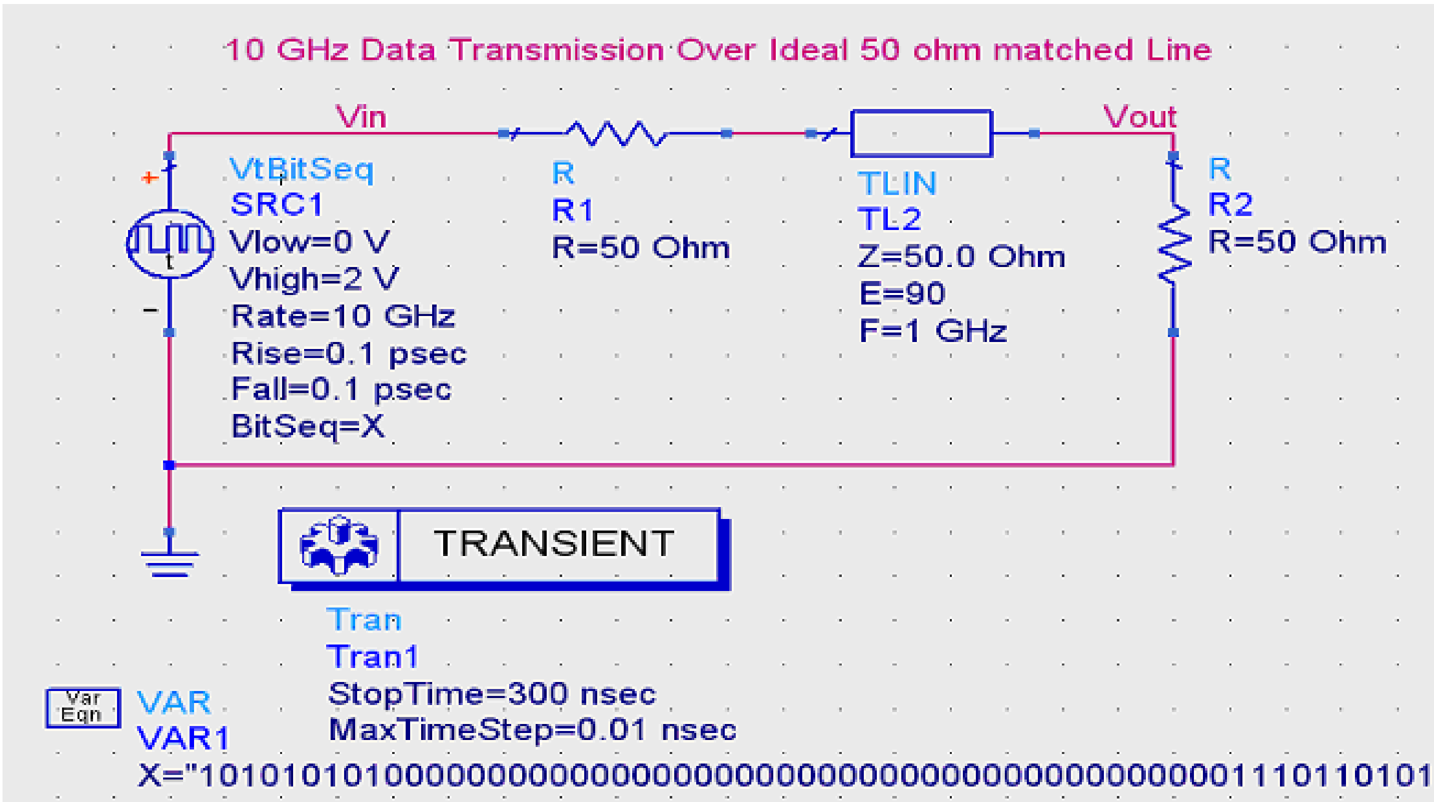
Eye Diagram

Typical Eye Diagrams

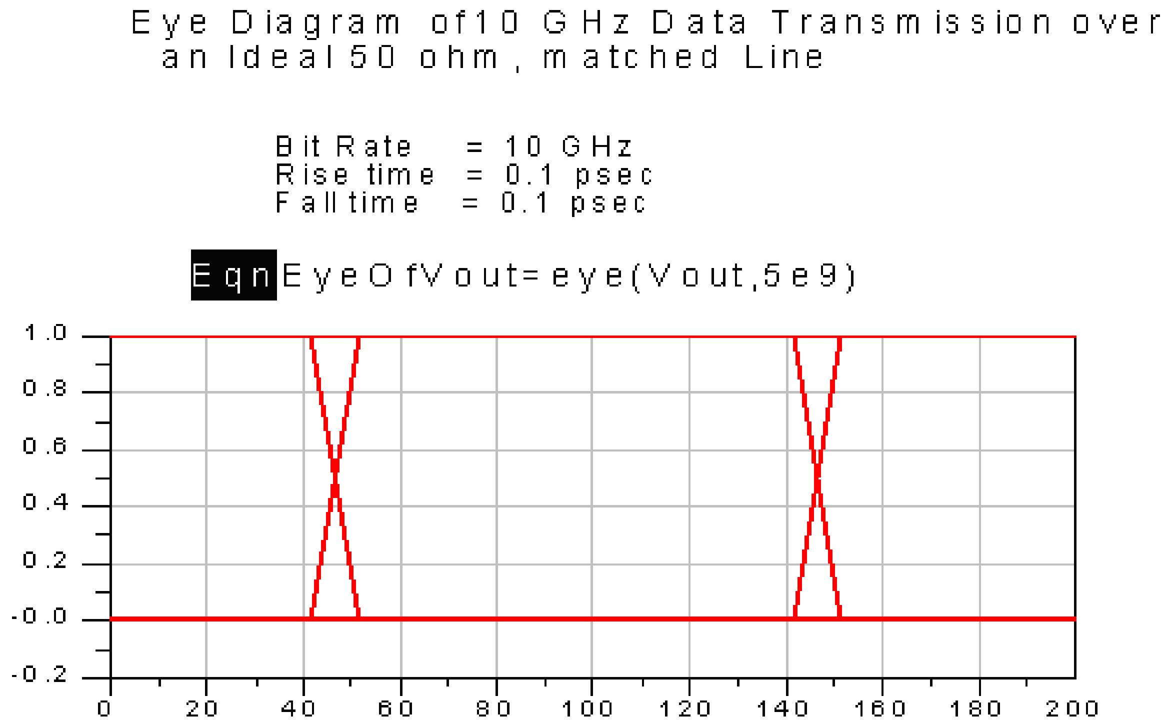




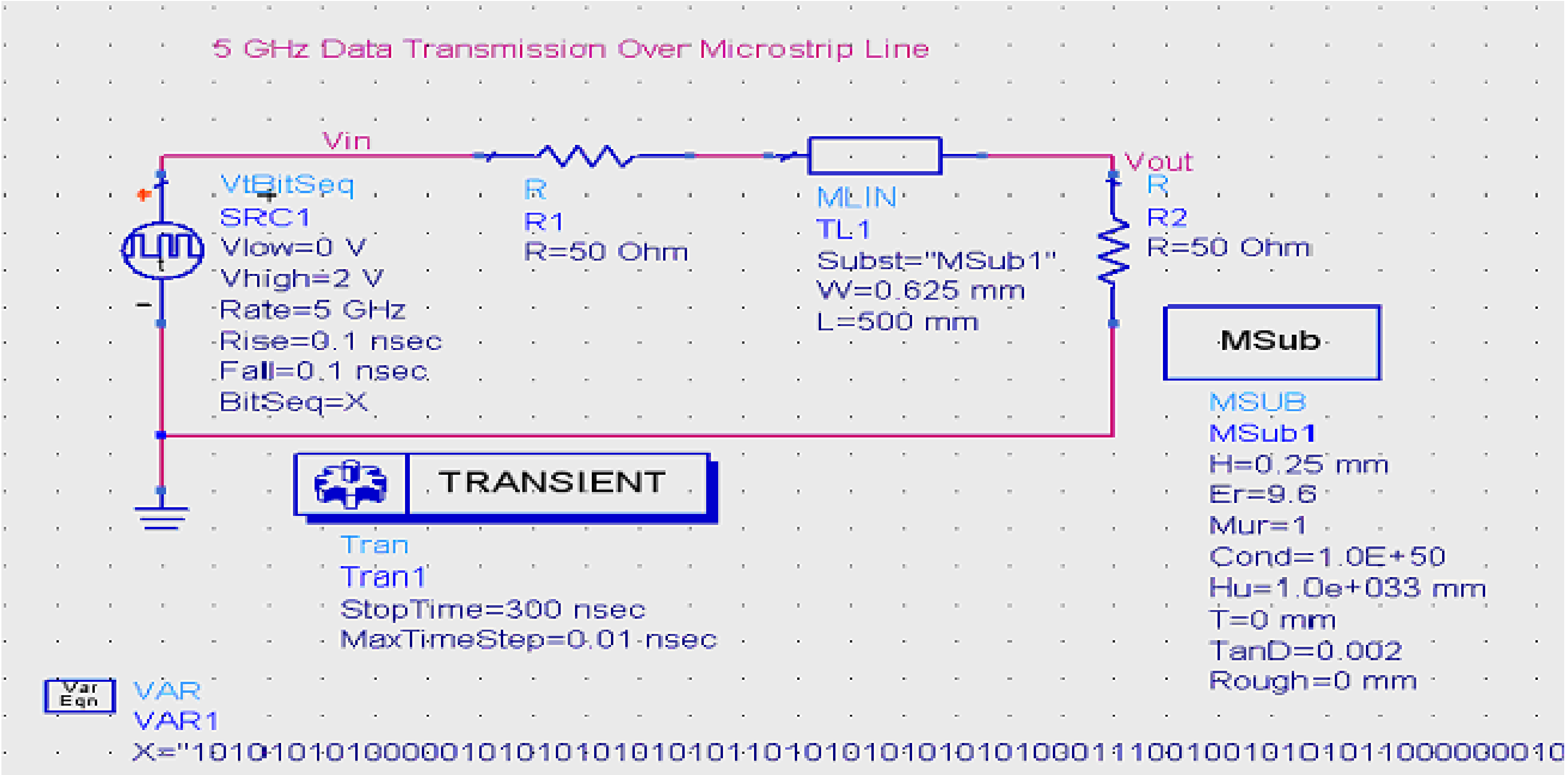
Eye Diagram - ADS Simulation



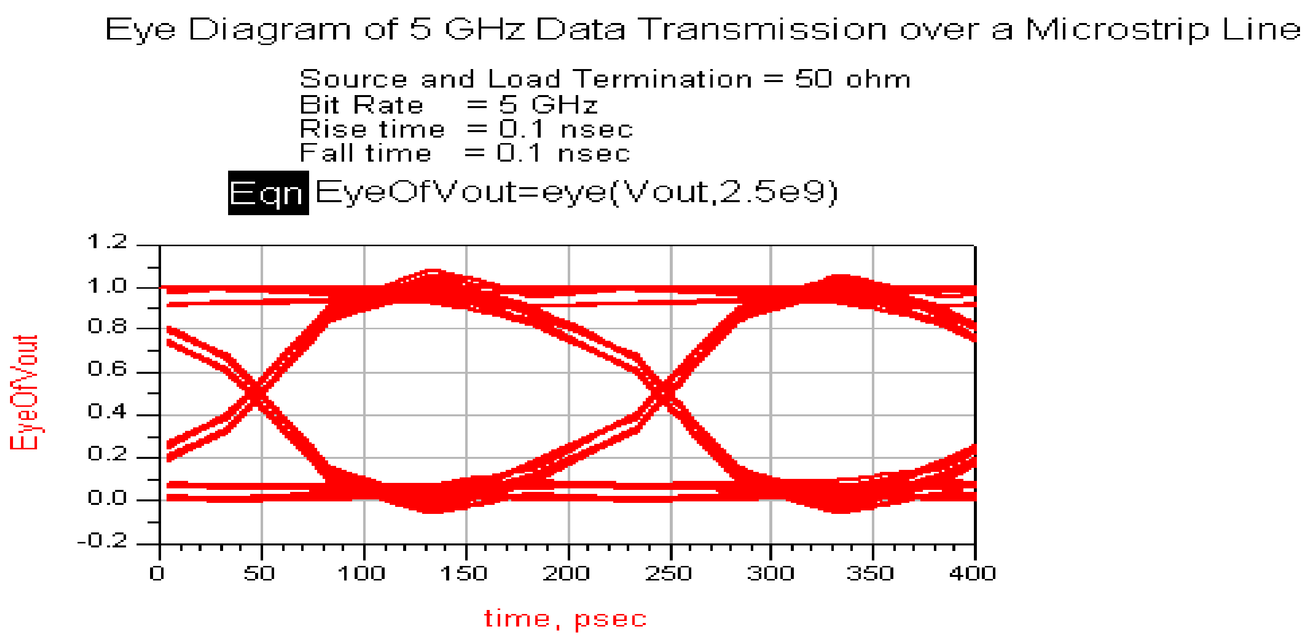
Eye Diagram - ADS Simulation
Ideal Matched Line



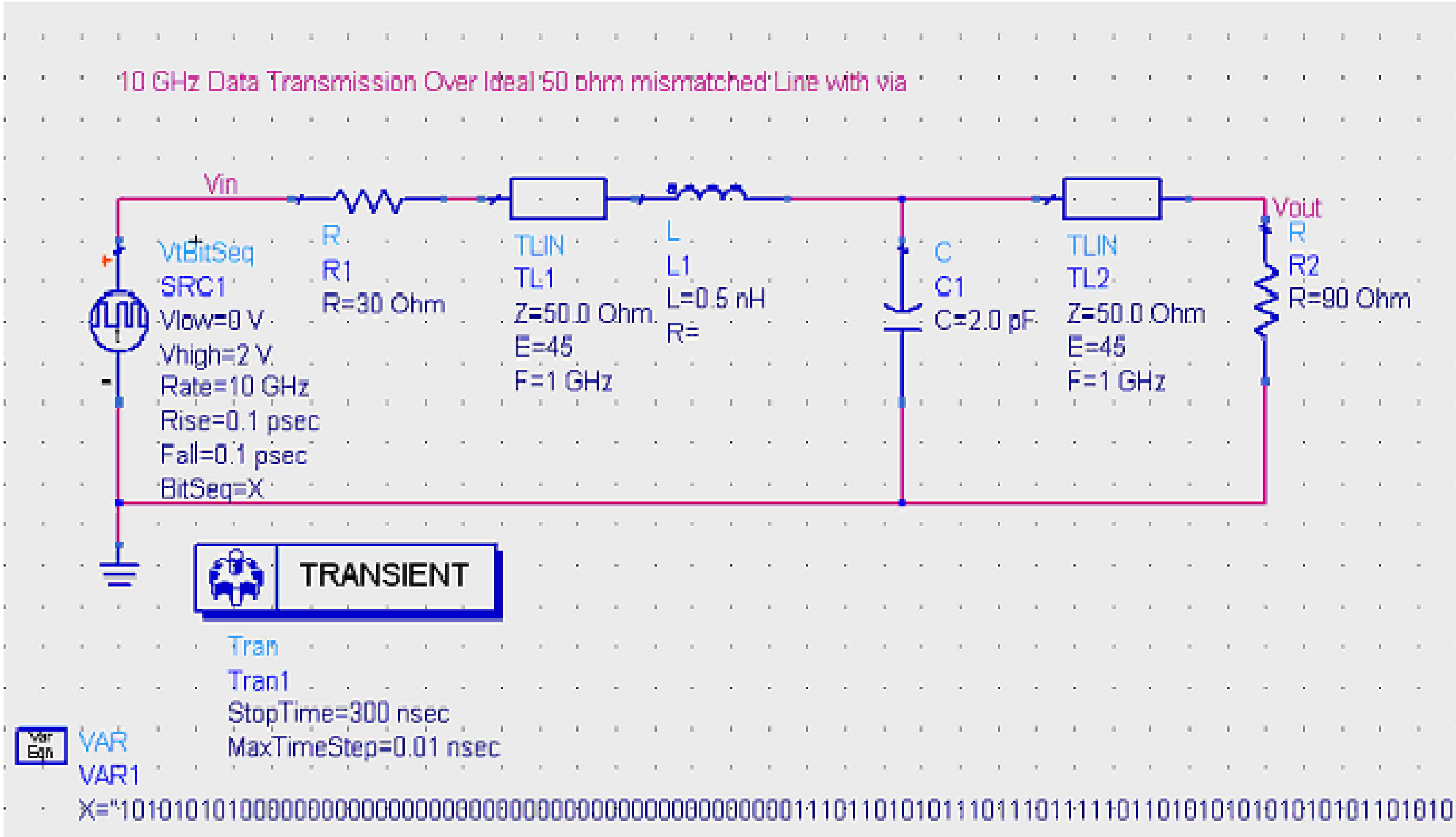
Eye Diagram - ADS Simulation
5 GHz Data Transmission



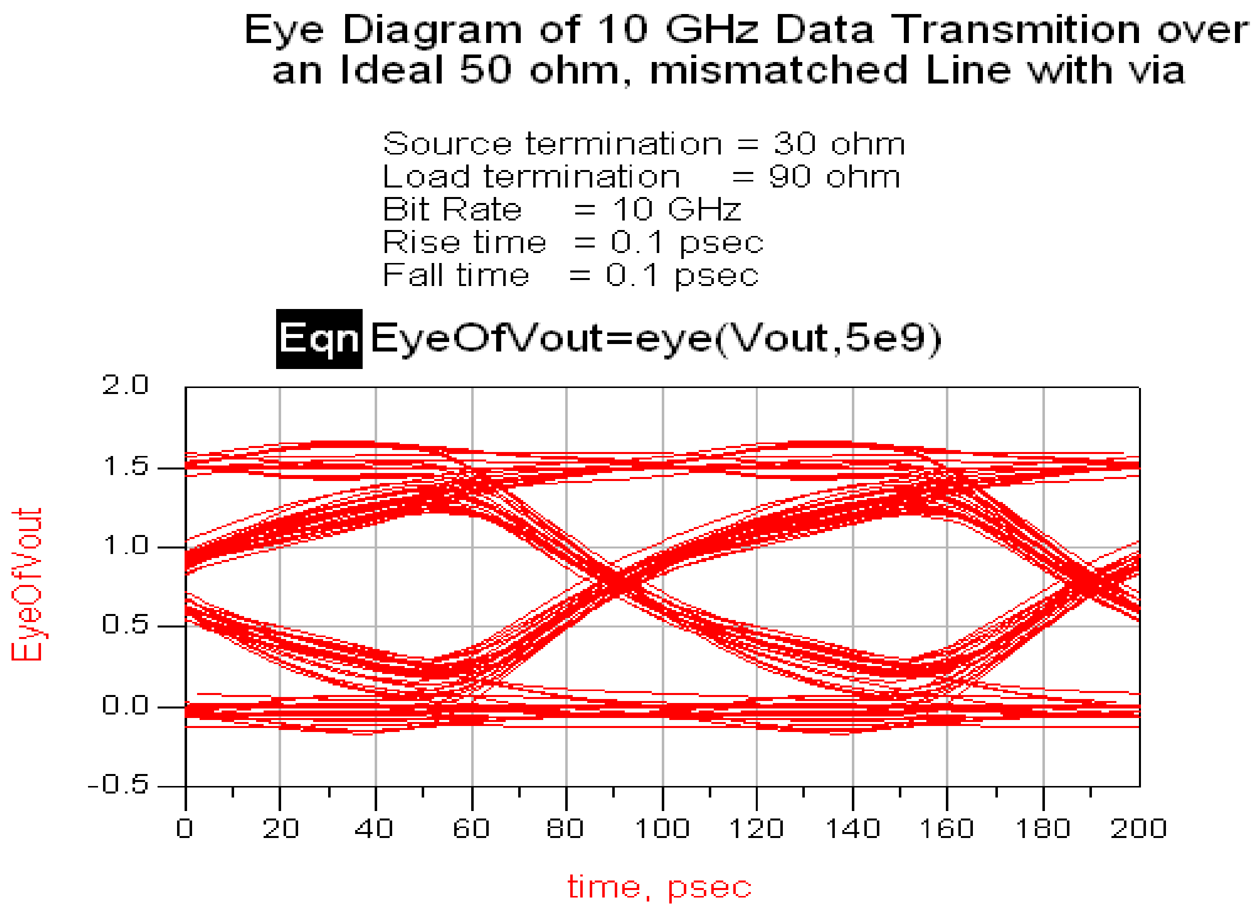
Eye Diagram - ADS Simulation
5 GHz Data Transmission



Eye Diagram - ADS Simulation
10 GHz Data Transmission



Eye Diagram - ADS Simulation



Bit-Error Rate

- **The Bit-error rate (BER) quantifies the likelihood of a bit being interpreted at the receiver incorrectly due to jitter- or amplitude-induced degradation on the received signal**

- **No higher than a 10^{-16} BER is tolerable → no more than 1 error out of 10^{16} bits.**

- **BER can be measured directly or quantified with statistical calculations**

- **Deterministic jitter(DJ) can be easily measured via S-parameters obtained in the frequency domain**