ECE 453
Wireless Communication Systems

Phase Locked Loops

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Phase Locked Loop (PLL)

A PLL is a voltage-controlled oscillator which has its frequency controlled by an external source

- **Loop oscillator frequency can be same or multiple of reference frequency**
- **If reference signal comes from a crystal oscillator, other frequencies can be derived with same stability as crystal frequency**
- **Loop oscillator frequency will track that of input**
- **Principle used in FM and FSCK demodulators tracking filters and instrumentation**

Why need PLLs?

- Reduces jitter.
- Reduces clock-skew in high-speed digital ckts.
- Instrumental in frequency synthesizers.
- Essential building block of CDRs.

Phase Locked Loop (PLL)

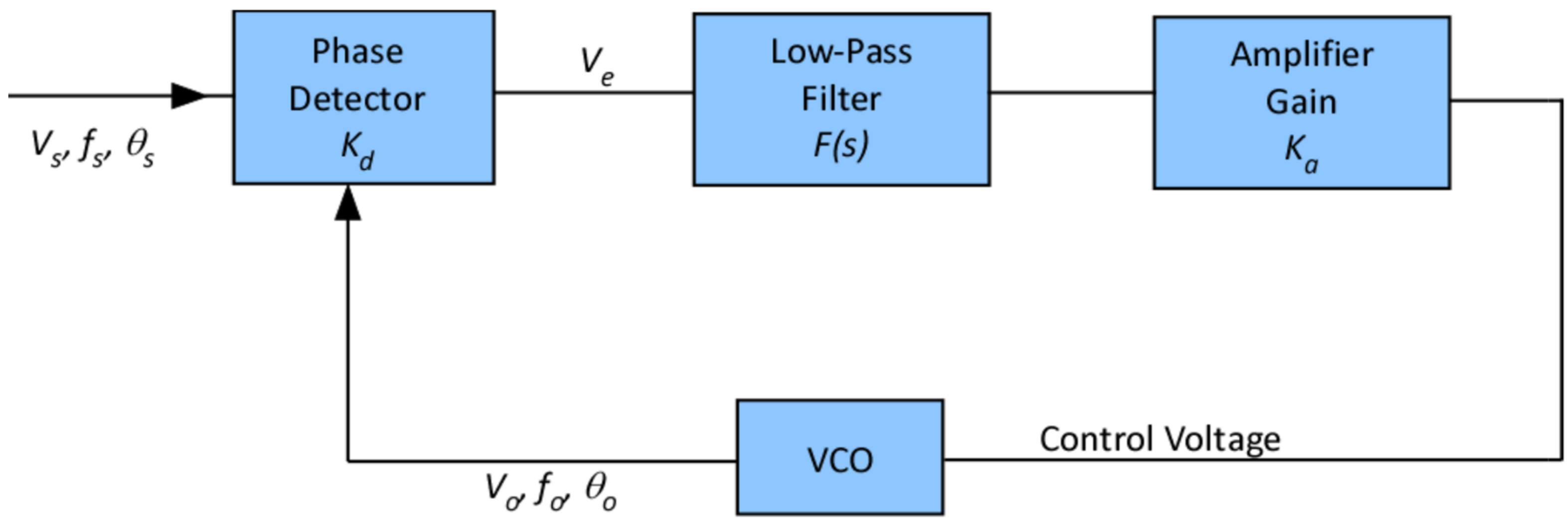
A PLL synchronizes the output phase and frequency of a controlled oscillator with the phase and frequency of a reference oscillator

The task of the PLL is to maintain coherence between the reference signal frequency and the output frequency via phase comparison

Functional Blocks

- Voltage controlled oscillator (VCO)
- Phase detector (PD or PFD)
- Loop filter
- Feedback divider (=1 for the simplest case)

Components of PLL



- **Loop is in lock when frequencies of input and VCO are identical ($f_s = f_o$)**
- **If input frequency changes, phase difference must change enough to produce control voltage V_d that produce equality in frequency**

Phase Definitions

θ_s : Phase of reference (input) signal

θ_o: Phase of VCO (output) signal

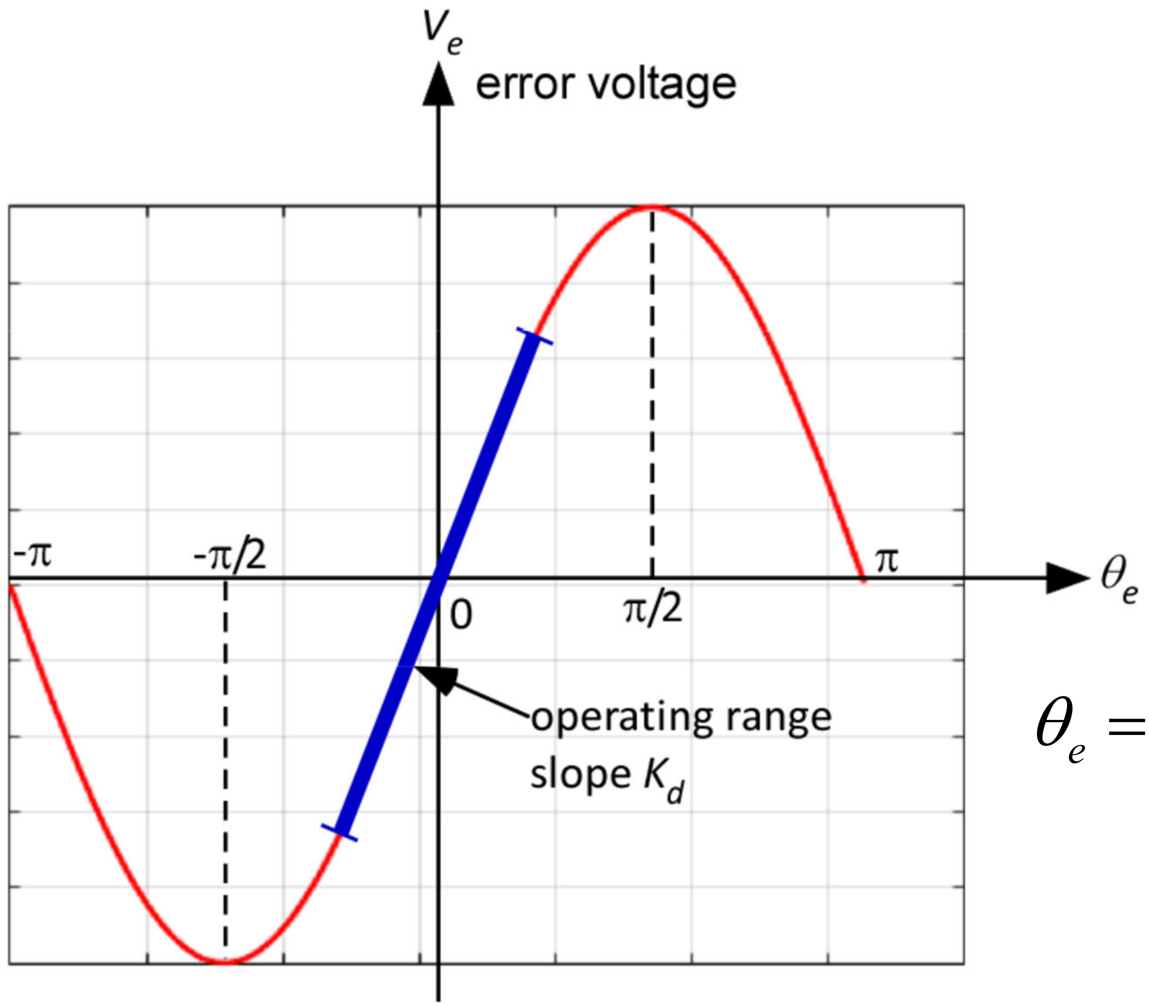
θ_d: Phase difference θ_s - θ_o

θ_e: Shifted angle

$\theta_e = \theta_d - \pi/2$, *for sinusoidal and triangular detectors*

$\theta_e = \theta_d - \pi$, *for sawtooth detectors*

Phase Detector - Sinusoidal



$$\theta_e = \theta_d - 90^\circ$$

Phase Detector - Sinusoidal

K_d = gain factor of the phase detector

$$K_d = \frac{\Delta V_e}{\Delta \theta_e}$$

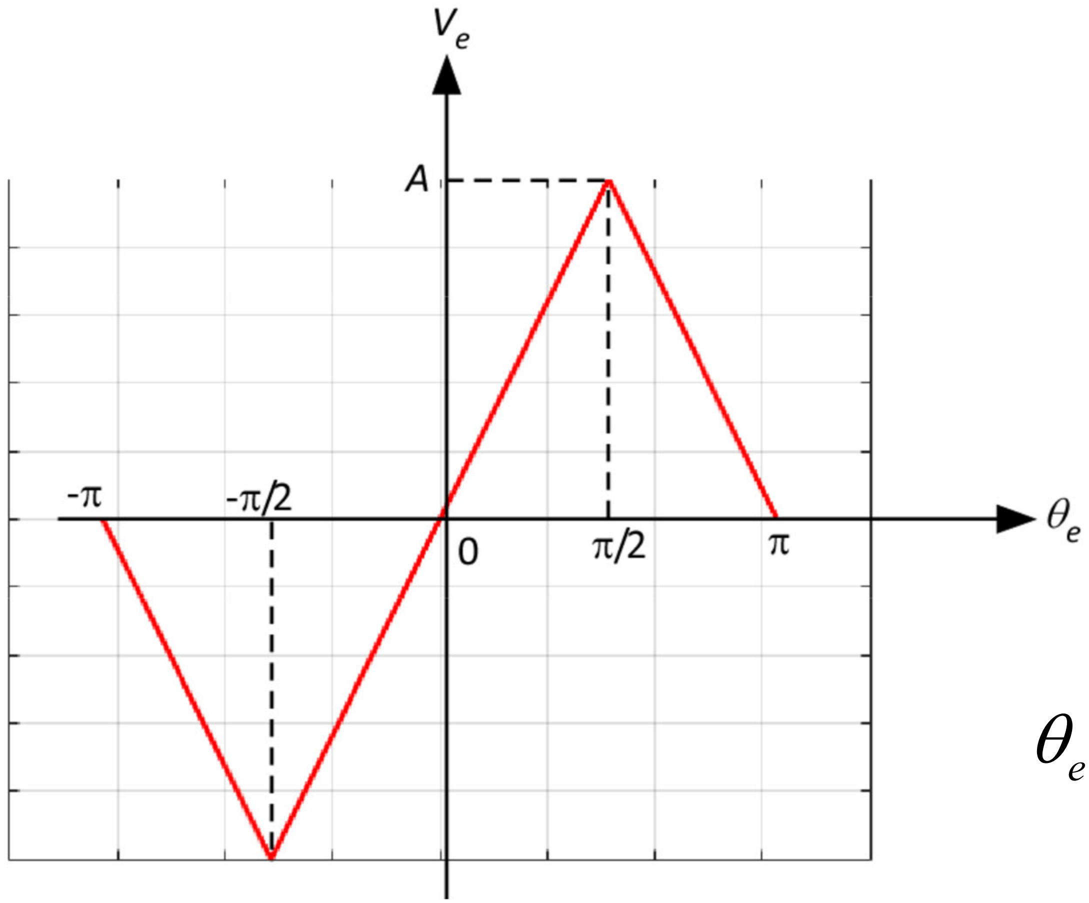
for a sinusoidal detector

$$V_e = A \sin \theta_e$$

for θ_e small,

$$V_e \simeq A\theta_e \quad \rightarrow \quad K_d = \frac{\Delta V_e}{\Delta \theta_e} \cong A = \frac{V_e}{\theta_e}$$

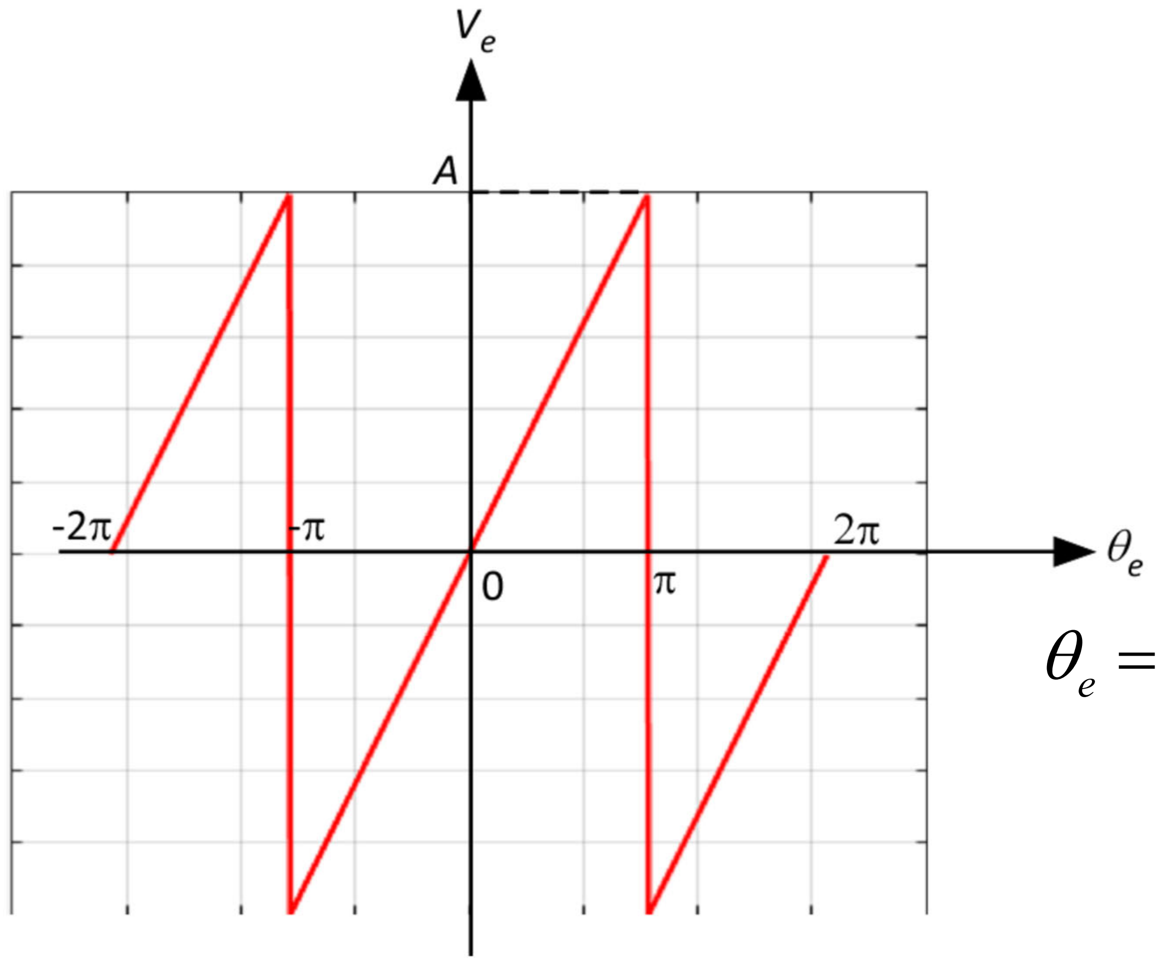
Phase Detector - Triangular



$$\theta_e = \theta_d - 90^\circ$$

$$K_d = \frac{2A}{\pi}$$

Phase Detector - Sawtooth

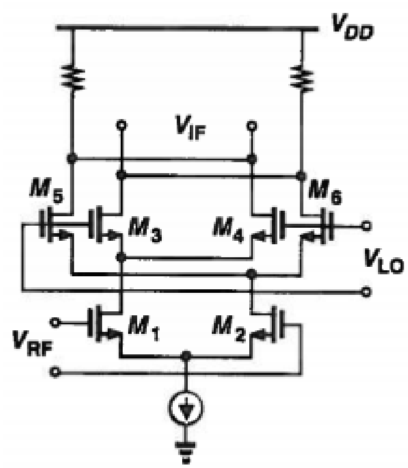


$$\theta_e = \theta_d - 180°$$

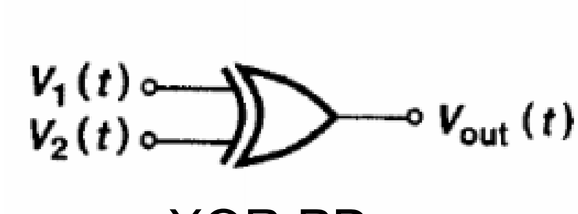
$$K_d = \frac{A}{\pi}$$

PD/PFD Circuits

Common PD Implementations:

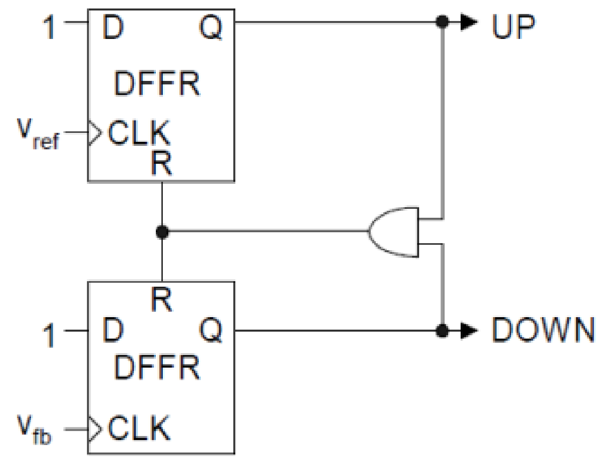


Gilbert-cell Mixer



XOR PD

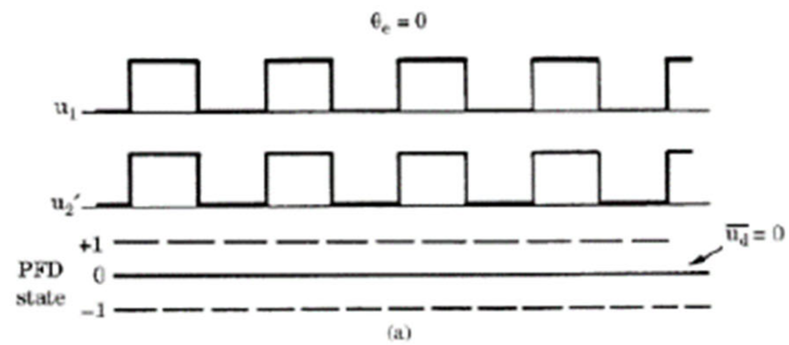
Common PFD Implementations:



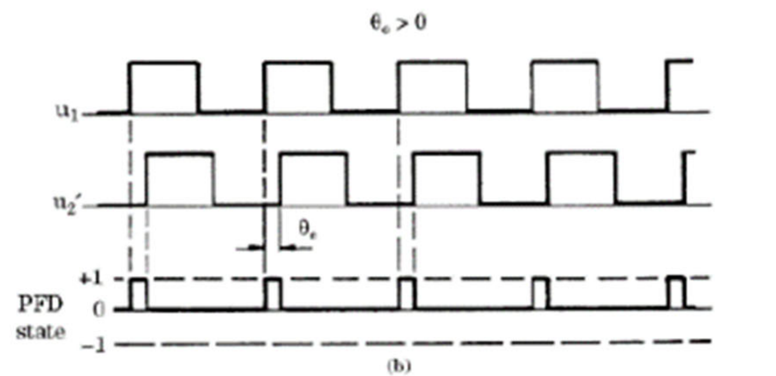
- PD/PFD are strictly digital circuits in high speed SerDes transceivers.
- Ideal PD is a "multiplier" in time-domain, <u>ex:</u> Mixer
- Analog PD → High Jitter, noise.
- XOR PD → sensitive to clock duty cycle
- PFD ~ best to lock phase and frequency!

PFD Analysis

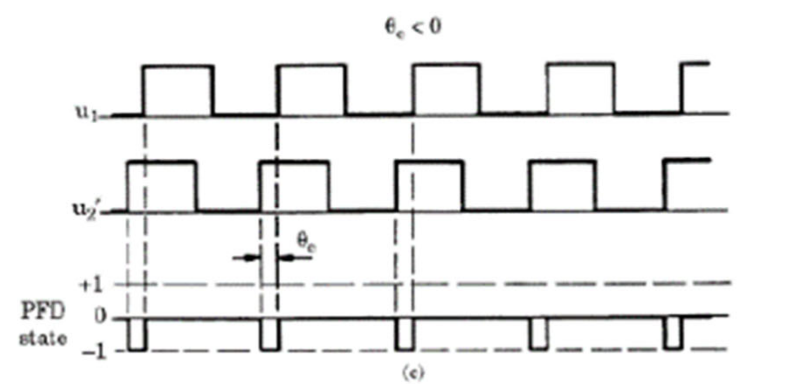
1. PFD is in state 0 with no phase difference.



2. PFD is in state 1 with positive phase difference.



3. PFD is in state -1 with negative phase difference.



Voltage-Controlled Oscillator

Output frequency is expressed by:

$$\omega_o = \omega_f + K_o V_d \; (rad/s)$$

Total angle of VCO can be described by:

$$\theta(t) = \int_0^t \left(\omega_f + \Delta\omega\right) dt = \omega_f t + \theta_o(t)$$

$\Delta\omega$ is deviation from ω_f

$$\theta_o(t) = \int_0^t \Delta\omega dt$$

DC Loop Gain

K_v = change in the oscillator frequency due to change in phase difference θ_e.

$$K_v = \frac{\Delta\omega_o}{\theta_e} = \frac{V_e}{\theta_e} \times \frac{V_d}{V_e} \times \frac{\Delta\omega}{V_d} = K_d \times K_a \times K_o$$

K_d = Phase detector gain factor
K_a = Amplifier gain
K_o = VCO gain factor

Phase Detector Mathematics

The phase detector is a mixer with

$$v_1(t) = V_1 \cos\left(\omega_{RF} t + \theta_1\right)$$

$$v_2(t) = V_2 \cos\left(\omega_{LO} t + \theta_2\right)$$

After mixing

$$v_p(t) = \frac{V_1 V_2}{2}\begin{bmatrix} \cos\left(\omega_{LO} t - \omega_{RF} t + \theta_2 - \theta_1\right) \\ + \cos\left(\omega_{LO} t + \omega_{RF} t + \theta_2 + \theta_1\right) \end{bmatrix}$$

Phase Detector Mathematics

Define

$$\omega_{beat} = \omega_{LO} - \omega_{RF}$$

$$V_{pb} = \frac{V_1 V_2}{2}$$

$$\theta_e = \theta_2 - \theta_1$$

Phase-error difference between signal 1 and signal 2

We get

$$v_p(t) = V_{pb}\cos\left(\omega_{beat} t + \theta_e\right)$$

Phase Detector Mathematics

We have

$$v_p(t) = V_{pb} \cos\left(\omega_{beat} t + \theta_e\right)$$

When the loop is in lock, ω_{beat}= 0 and v_p is a DC voltage. When the loop is not in lock, v_p is a voltage that tries to pull the VCO into synchronism with the input signal.

Actual process of acquiring lock is nonlinear

Order of PLL

Highest power of *s* in denominator of closed-loop transfer function

First Order

$$H(s) = \frac{K}{s+a}$$

Second Order

$$H(s) = \frac{K}{s^2 + as + b}$$

Type of PLL

Number of poles at the origin for the open-loop transfer function

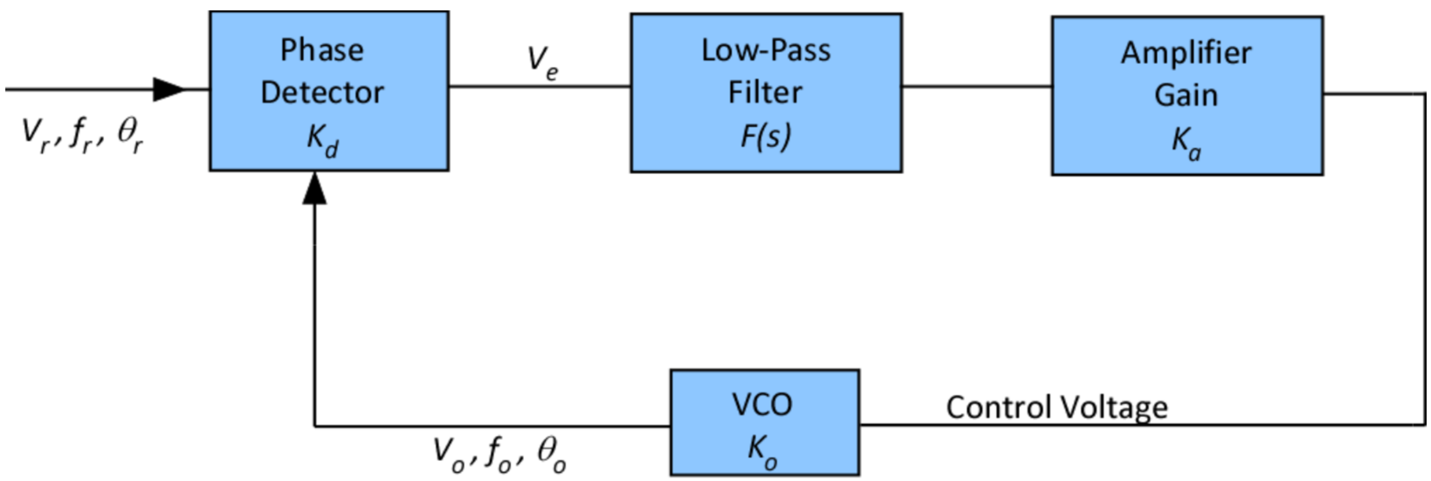
Type 1

$$A(s) = \frac{K}{s}$$

Type 2

$$A(s) = \frac{K}{s^2}$$

PLL Transfer Functions



$$H(s) = \frac{\theta_o(s)}{\theta_r(s)} = \frac{K_o K_d K_a F(s)}{s + K_o K_d K_a F(s)}$$

$$H_e(s) = \frac{\theta_e(s)}{\theta_r(s)} = \frac{s}{s + K_o K_d K_a F(s)}$$

Loop Transfer Function - No Filter

When there is no filter in the loop, *F(s) =1,* and

$$H(s) = \frac{K_o K_d}{s + K_o K_d} = \frac{K_o K_d / s}{1 + K_o K_d / s}$$

⟵ **First-order PLL**

which can be rewritten as

$$H(s) = \frac{\omega_L / s}{1 + \omega_L / s}$$

where

$$\omega_L = K_o K_d$$

⟵ **loop bandwidth**

First-Order PLL

When there is no filter in the loop, *F(s) =1,* and

$$H_e(s)=\frac{\theta_e(s)}{\theta_r(s)}=\frac{s}{s+K_oK_dK_a}$$

For a step change in the input <u>phase</u> ($\Delta\theta_r/s$) the corresponding phase error is:

$$\theta_e(s)=\frac{s(\Delta\theta_r/s)}{s+K_oK_dK_a}$$

To find steady-state response, use final-value theorem for Laplace transforms

$$\lim_{t\to\infty}\theta_e(t)=\lim_{s\to 0}s\theta_e(s)=\lim_{s\to 0}\frac{s^2(\Delta\theta_r/s)}{s+K_oK_dK_a}=0$$

First-order loop will eventually track phase change at input

First-Order PLL

For a step change in frequency, the resulting phase change will be a ramp ($\Delta\omega_r/s^2$) and the corresponding phase error is:

$$\theta_e(s) = \frac{s\left(\Delta\omega_r / s^2\right)}{s + K_o K_d K_a}$$

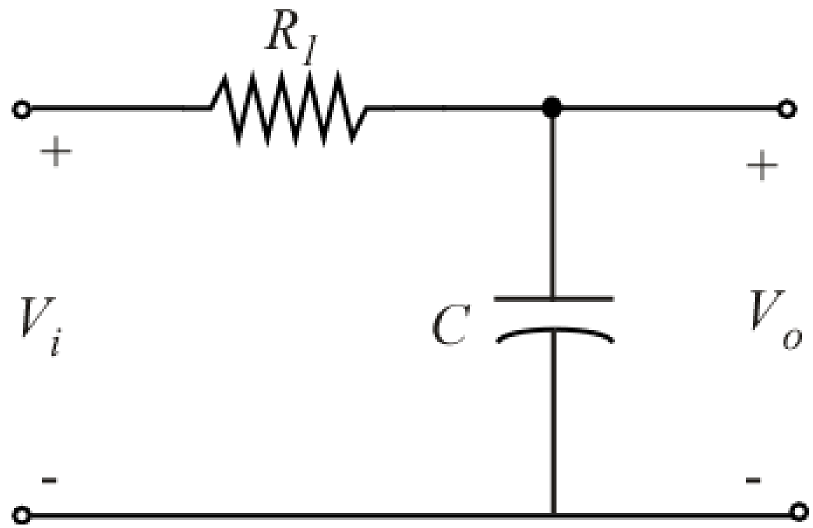
Use final-value theorem for Laplace transforms

$$\lim_{t\to\infty}\theta_e(t) = \lim_{s\to 0} s\theta_e(s) = \lim_{s\to 0}\frac{s^2\left(\Delta\omega_r / s^2\right)}{s + K_o K_d K_a} = \frac{\Delta\omega_r}{K_o K_d K_a}$$

Phase error is proportional to frequency change

➔ ***PLL can be used as FM demodulator!***

Loop Transfer Function - RC Filter



$$F(s) = \frac{V_o}{V_i} = \frac{1}{1 + s\tau}$$

$$\tau \equiv RC$$

$$H(s) = \frac{1}{\frac{s^2\tau}{K_o K_d} + \frac{s}{K_o K_d} + 1}$$

Loop Transfer Function - RC Filter

$$H(s) = \frac{1}{\dfrac{s^2\tau}{K_oK_d} + \dfrac{s}{K_oK_d} + 1}$$

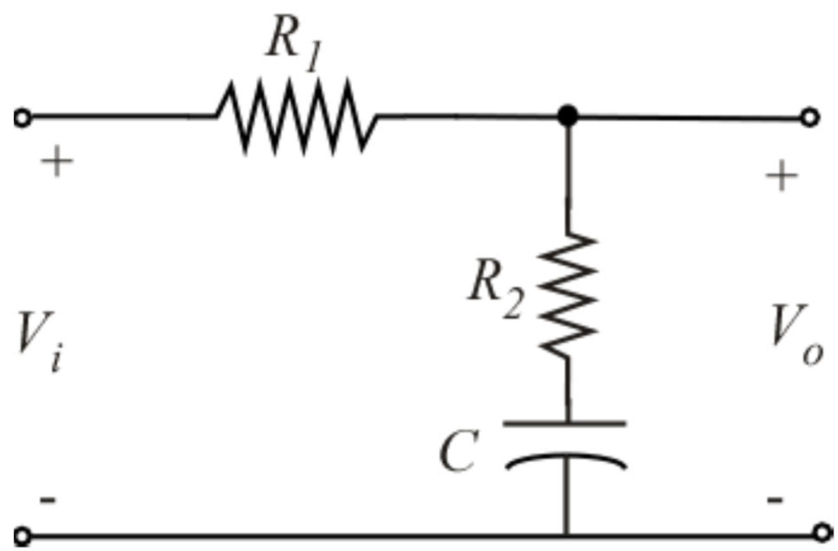
$$H(s) = \frac{1}{\dfrac{1}{\omega_n^2}s^2 + \dfrac{2\varsigma}{\omega_n}s + 1}$$

ζ: damping factor

ω_n: "natural frequency"

$$\omega_n = \sqrt{\frac{K_oK_d}{\tau}} \qquad \varsigma = \frac{\omega_n}{2K_oK_d} = \frac{1}{2\sqrt{\tau K_oK_d}}$$

Loop Transfer Function - Lag-Lead Filter



$$F(s)=\frac{V_o}{V_i}=\frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}$$

$$\tau_1 \equiv R_1 C$$

$$\tau_2 \equiv R_2 C$$

$$H(s)=\frac{s\left(2\varsigma\omega_n-\omega_n^2/K_oK_d\right)+\omega_n^2}{s^2+2\varsigma\omega_n s+\omega_n^2}$$

Loop Transfer Function - Lag-Lead Filter

$$H(s)=\frac{s\left(2\varsigma\omega_n-\omega_n^2/K_oK_d\right)+\omega_n^2}{s^2+2\varsigma\omega_n s+\omega_n^2}$$

$$\tau_1 \equiv R_1C$$

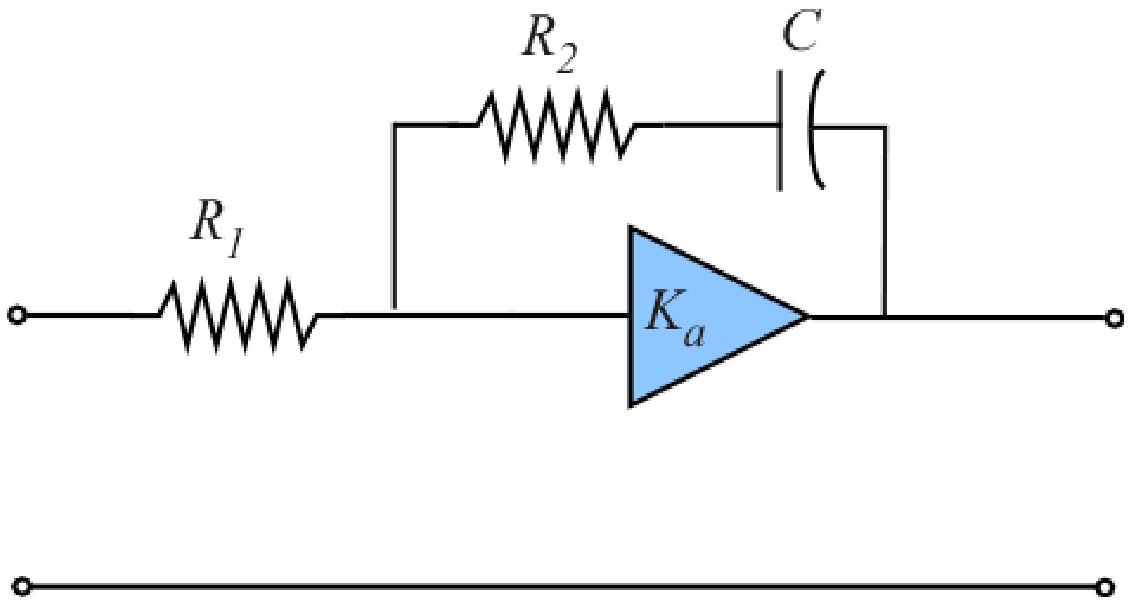
$$\tau_2 \equiv R_2C$$

$$\omega_n=\sqrt{\frac{K_oK_d}{\tau_1+\tau_2}} \qquad \varsigma=\frac{1}{2}\left(\frac{K_oK_d}{\tau_1+\tau_2}\right)^{1/2}\left(\tau_2+\frac{1}{K_oK_d}\right)=\frac{\tau_2\omega_n}{2}+\frac{\omega_n}{2K_oK_d}$$

ζ: damping factor

ω_n: "natural frequency"

PLL Transfer Function - Active Filter



$$\tau_1 \equiv R_1 C$$

$$\tau_2 \equiv R_2 C$$

$$F(s) = \frac{V_o}{V_i} = \frac{1 + s\tau_2}{s\tau_1}$$

PLL Transfer Function - Active Filter

$$H(s) = \frac{2\varsigma\omega_n s + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1}}$$

$$\varsigma = \frac{\tau_2 \omega_n}{2}$$

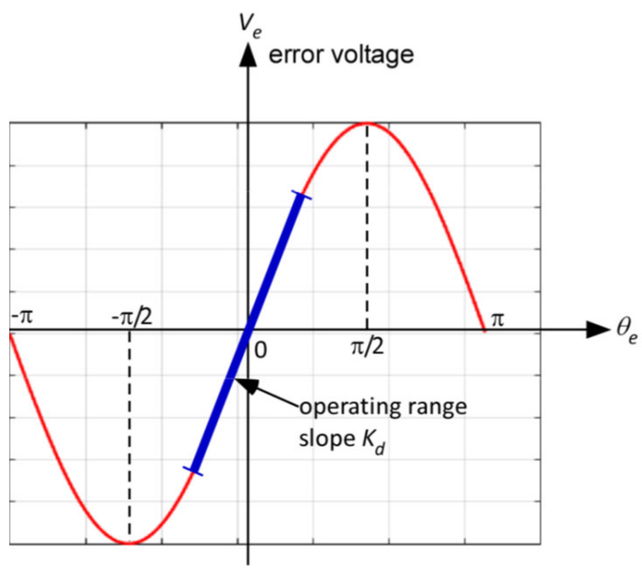
ζ: damping factor

ω_n: "natural frequency"

Hold in Range

Range over which we can change f_s and still have the loop remain in lock.

For sinusoidal phase detector



$$V_e = K_d \sin\theta_e$$

$$\sin\theta_e = \frac{V_e}{K_d} = \frac{V_e K_a K_o}{K_v} = \frac{\Delta\omega}{K_v}$$

Since sin θ_e cannot exceed ± 1 as θ_e approaches $\pm\pi/2$ The hold-in range is equal to the DC loop gain

Sinusoidal detector:

Max V_e* is *A* and *$A=V_d$

$$\pm\Delta\omega_H = \pm K_v$$

Lock in Range

Range of frequencies over which the loop will come into lock without slipping cycles.

- **If the frequency difference $|\omega_s - \omega_f|$ is less than the 3-dB bandwidth of the closed-loop transfer function *H(s)*, the loop will lock up without slipping cycles.**

$$\Delta\omega_L \approx \pm 2\varsigma\omega_n$$ ⟵ **Maximum lock-in range**

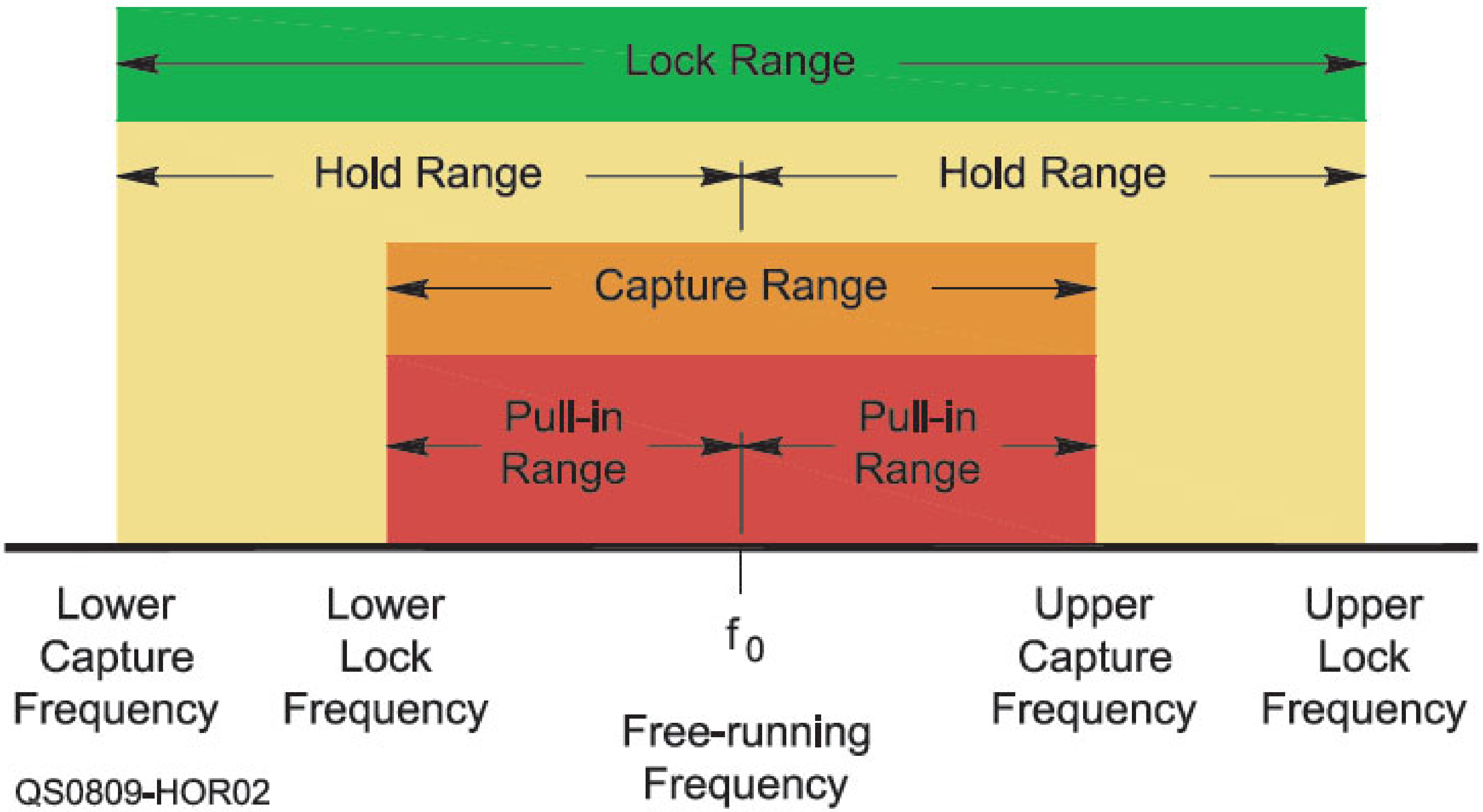
Pull in Range

Range of frequencies over which the loop will eventually lock

- **Once loop is in lock, small loop bandwidth is desirable to minimize noise transmission**
- **If initial frequency difference is outside lock-in range but inside pull-in range, difference-frequency waveshape is nonlinear and contains DC component that gradually shifts VCO frequency until lock up occurs**

$$\Delta\omega_p \approx \pm\sqrt{2}\left(2\varsigma\omega_n K_v - \omega_n^2\right)^{1/2}$$

Frequency Ranges of PLL



Source: N0ax Hands-On Radio

Transfer Function Representation

In general, the transfer function of an amplifier can be expressed as

$$H(s) = a_m \frac{(s - Z_1)(s - Z_2)\ldots(s - Z_m)}{(s - P_1)(s - P_2)\ldots(s - P_m)}$$

$Z_1, Z_2, \ldots Z_m$ are the **zeros** of the transfer function

$P_1, P_2, \ldots P_m$ are the **poles** of the transfer function

s is a complex number $s = \sigma + j\omega$

Transfer Function and Stability

H(s) can also be written in the form

$$H(s)=\frac{1+a_1s+a_2s^2+\ldots+a_ns^n}{1+b_1s+b_2s^2+\ldots b_ns^n}$$

The coefficients *a* and *b* are related to the frequencies of the zeros and poles respectively.

For a system to be stable all the poles and the zeros must reside on the left half of the s plane.

PLL Stability

The closed-loop transfer function *H(s)* can be expressed in terms of the open-loop gain *A(s)*

$$H(s) = \frac{A(s)}{1 + A(s)}$$

- **The loop is stable if the magnitude of the open-loop gain falls below 1 dB before its phase reaches 180º**
- **The greater the phase margin, the more stable the system and the higher the signal integrity**

PLL Stability

Let A(s) be the open-loop gain

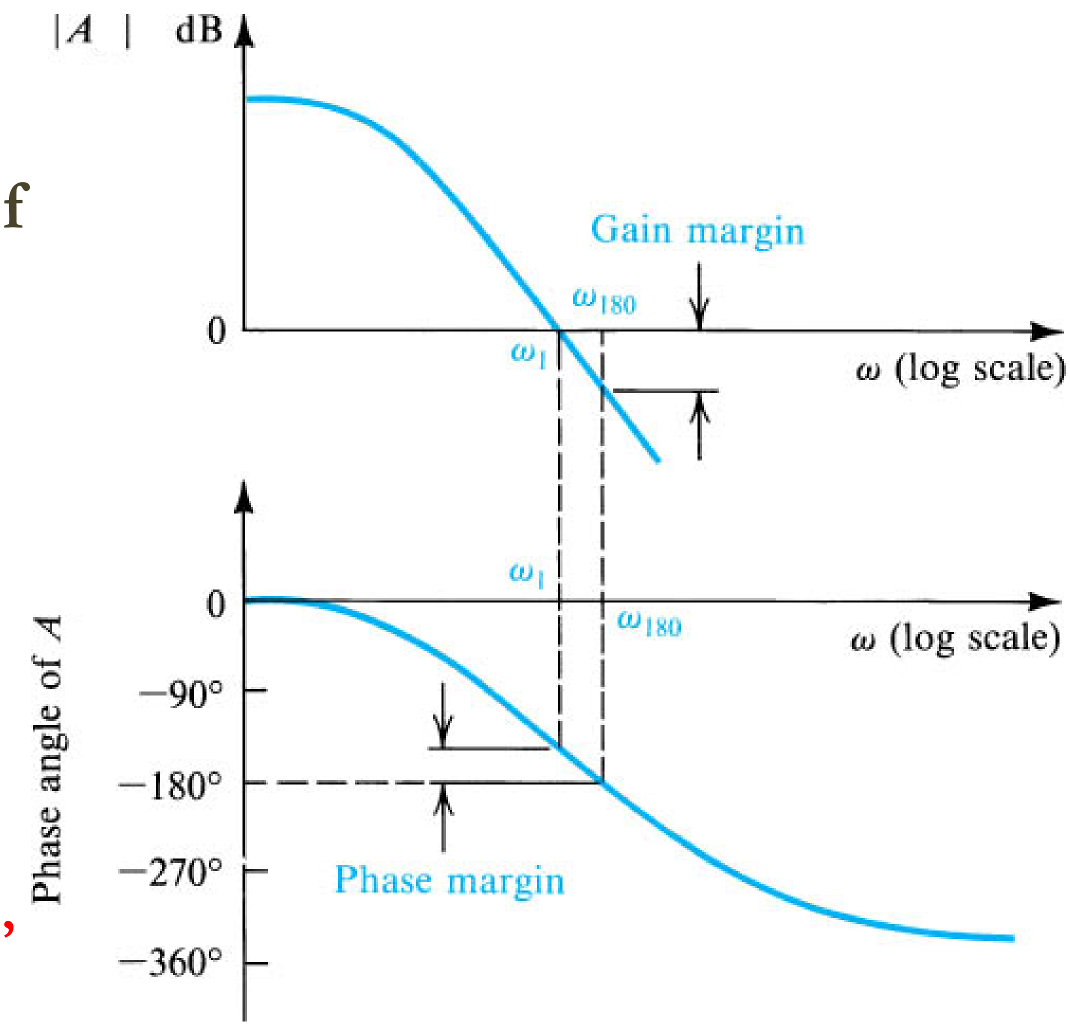
Gain Margin:

Difference between value of $|A(s)|$ at ω_{180} and unity

Phase Margin:

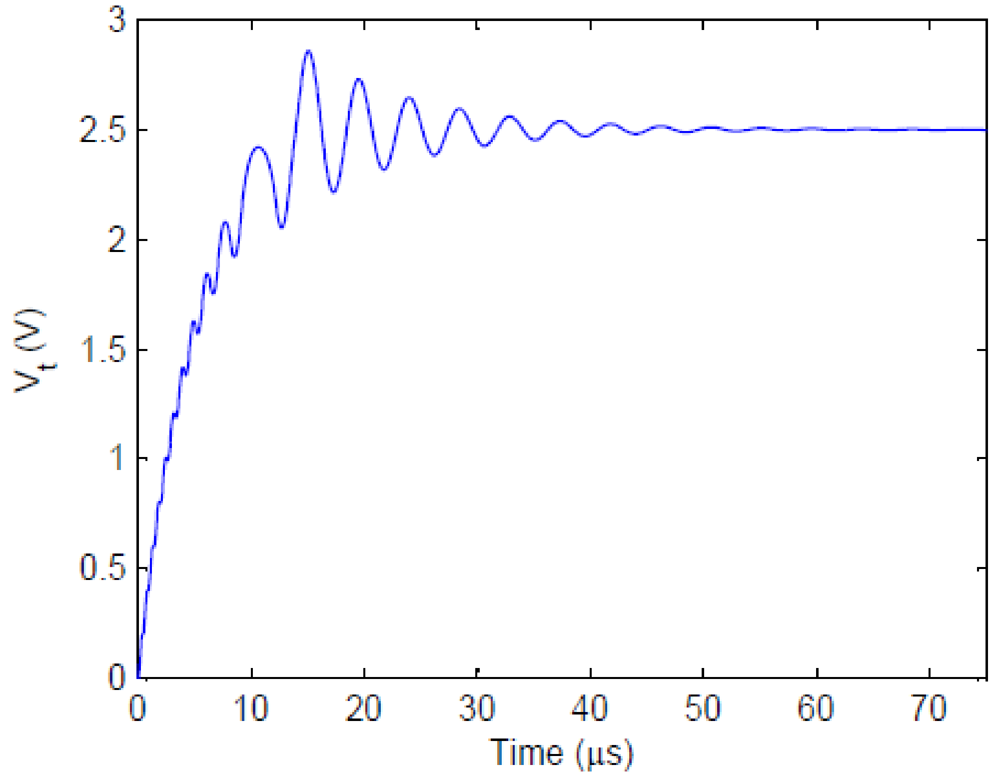
Difference between value of phase when $|A(s)|=1$ and 180^o

If phase angle at frequency when $|A(s)|=1$ is less than 180^o, loop is stable, otherwise, loop is unstable



PLL Operation – Acquisition

Tuning Voltage
During acquisition

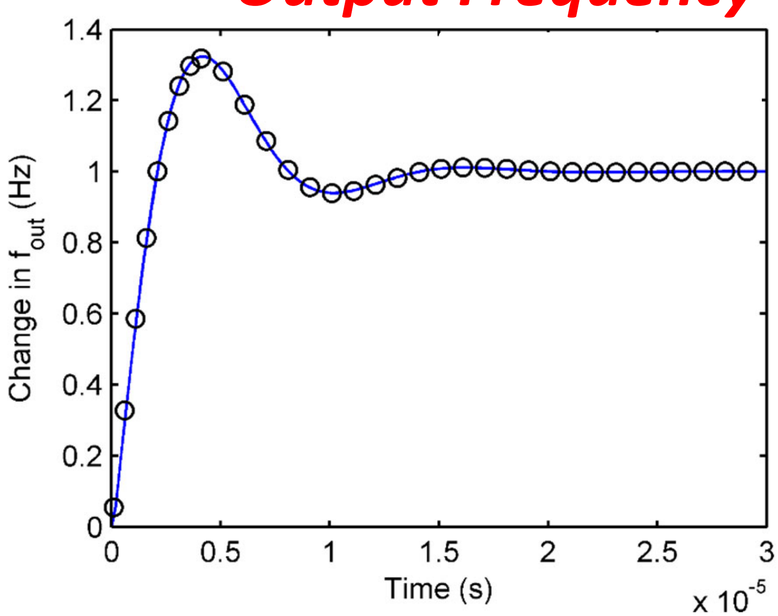


PLL Operation – Lock-In

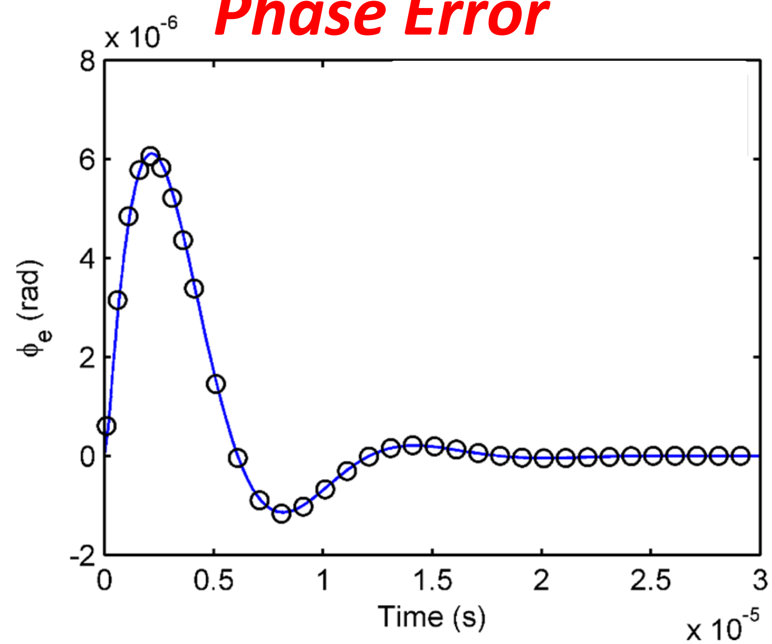
- PLL characteristics
  - $K_D = 5/(2\pi)$ V/rad, $K_V = 2\pi\,(3\times10^5)$ rad/V, $\tau_1 = 4.385\times10^{-6}$ s, $\tau_2 = 1.592\times10^{-6}$ s
- Small unit step change in $f_{in.}$
- PLL operates in the linear region:

$$\sin\phi_e(t) \approx \phi_e(t)$$

Output Frequency

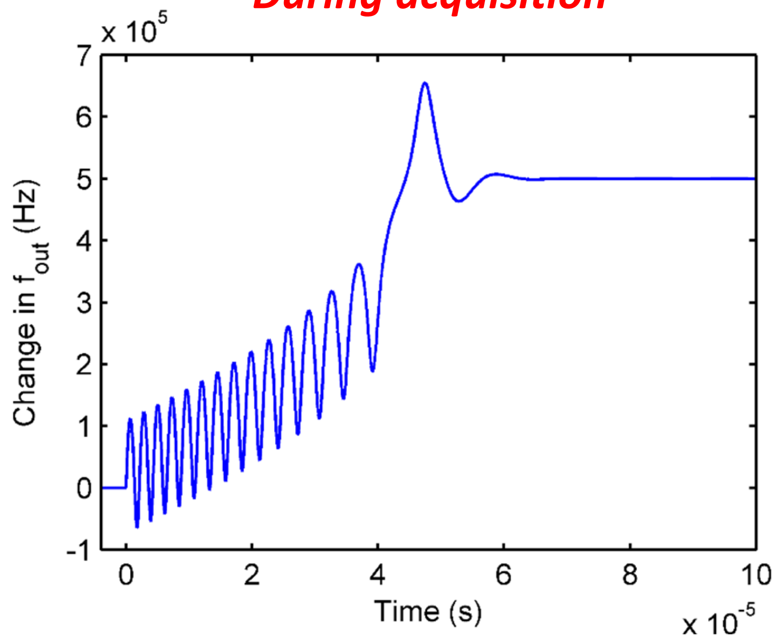


Phase Error

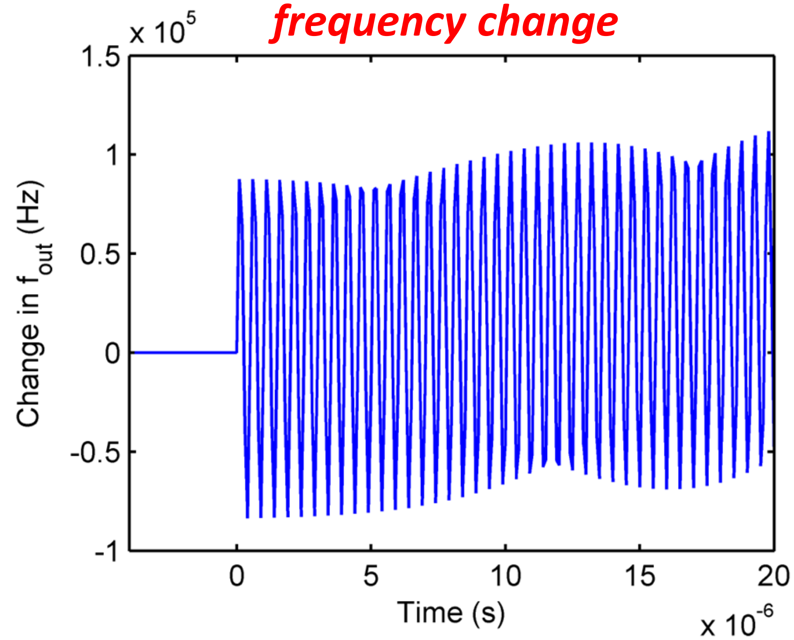


PLL Operation – Acquisition

- Large change in $f_{in.}$
- PLL exhibits non-linear behavior:



5 kHz change in f_{in}. Pull-in/acquisition process.



2 MHz change in f_{in}. Pull-out process. PLL no longer locks.

PLL Operation – Long Simulation

- Another example:
  - Long simulation (200 μs)
- Input:
  - 0 – 75 μs : 38.5 MHz
  - 75 μs – 130 μs : 38.3 MHz
  - 130 μs – 180 μs : 38.6 MHz
  - 180 μs – 200 μs : 38 MHz