ECE 453
Wireless Communication Systems

Phase Locked Loops

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Phase Locked Loop (PLL)

A PLL is a voltage-controlled oscillator which has its frequency controlled by an external source

- Loop oscillator frequency can be same or multiple of reference frequency
- If reference signal comes from a crystal oscillator, other frequencies can be derived with same stability as crystal frequency
- Loop oscillator frequency will track that of input
- Principle used in FM and FSCK demodulators tracking filters and instrumentation

Phase Locked Loop (PLL)

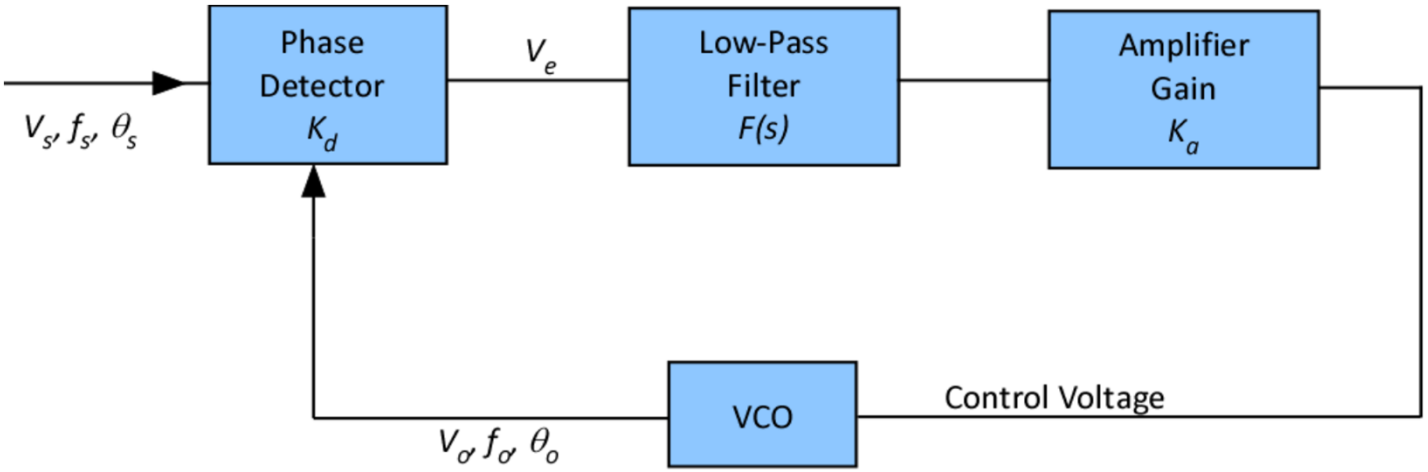
A PLL synchronizes the output phase and frequency of a controlled oscillator with the phase and frequency of a reference oscillator

The task of the PLL is to maintain coherence between the reference signal frequency and the output frequency via phase comparison

Functional Blocks

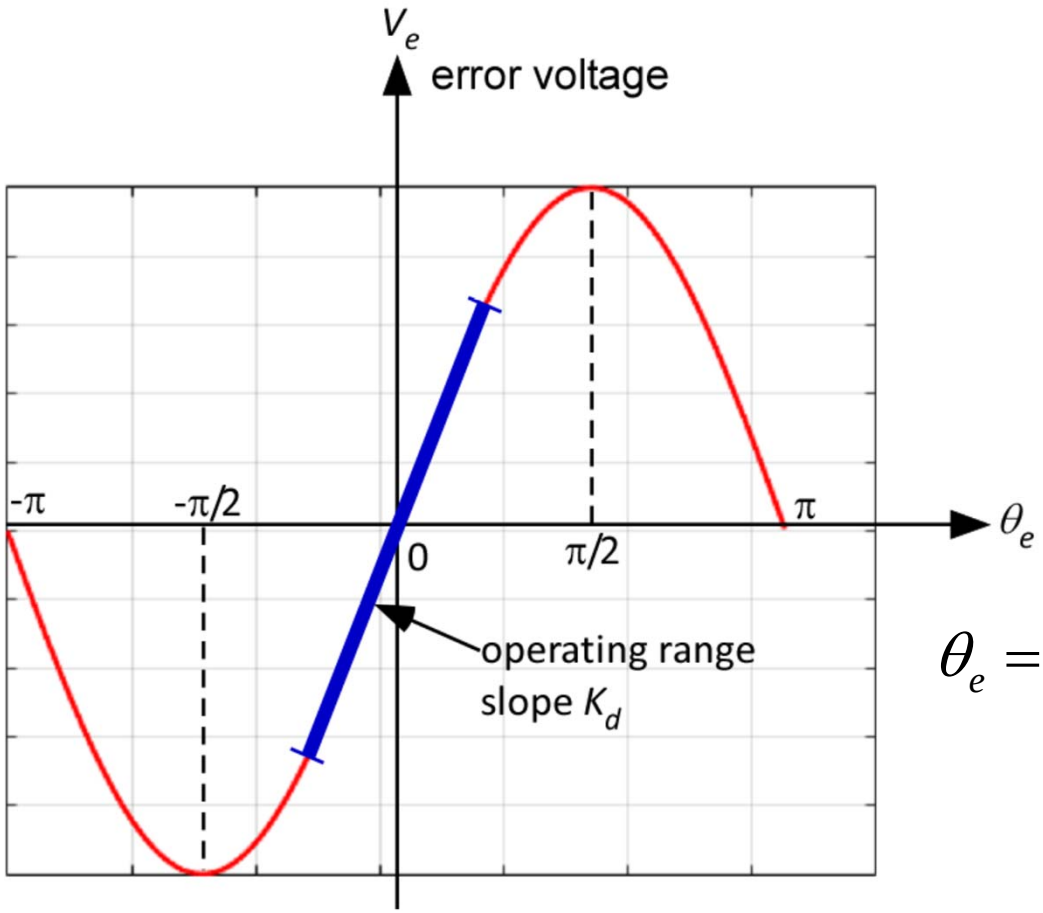
- Voltage controlled oscillator (VCO)
- Phase detector (PD or PFD)
- Loop filter
- Feedback divider (=1 for the simplest case)

Components of PLL



- Loop is in lock when frequencies of input and VCO are identical ($f_s = f_o$)
- If input frequency changes, phase difference θ_e must change enough to produce control voltage V_d that produce equality in frequency

Phase Detector - Sinusoidal



$$\theta_e = \theta_d - 90°$$

Phase Detector - Sinusoidal

K_d = gain factor of the phase detector

$$K_d = \frac{\Delta V_e}{\Delta \theta_e}$$

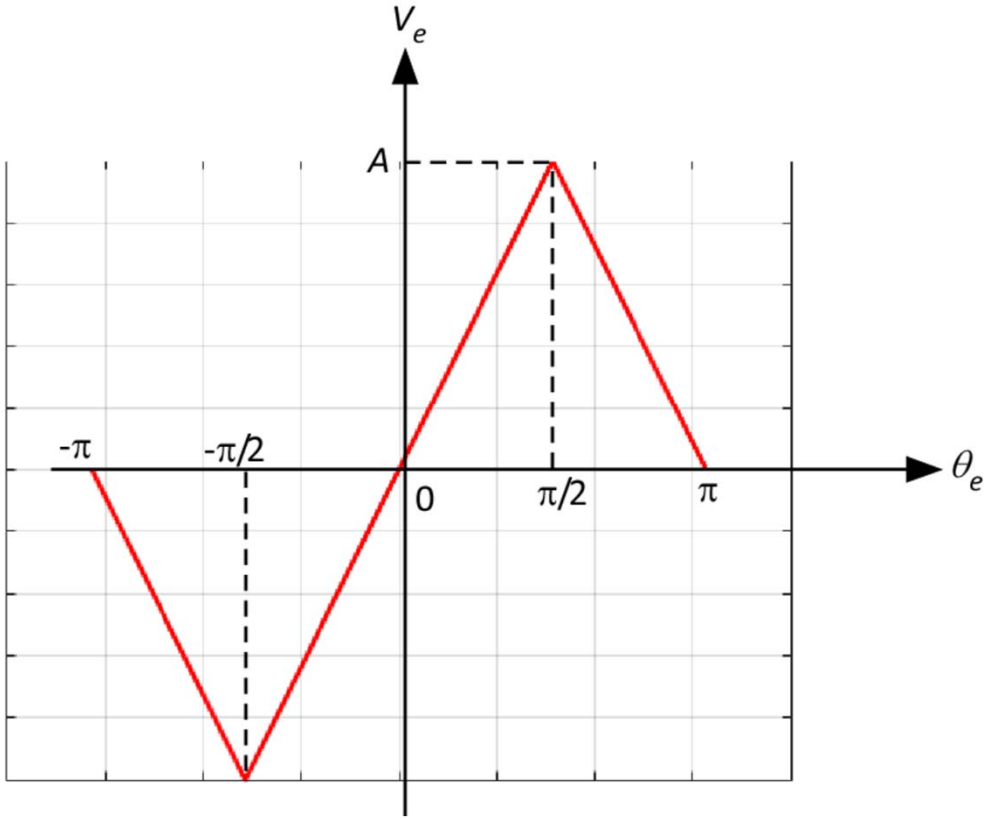
for a sinusoidal detector

$$V_e = A \sin \theta_e$$

for θ_e small,

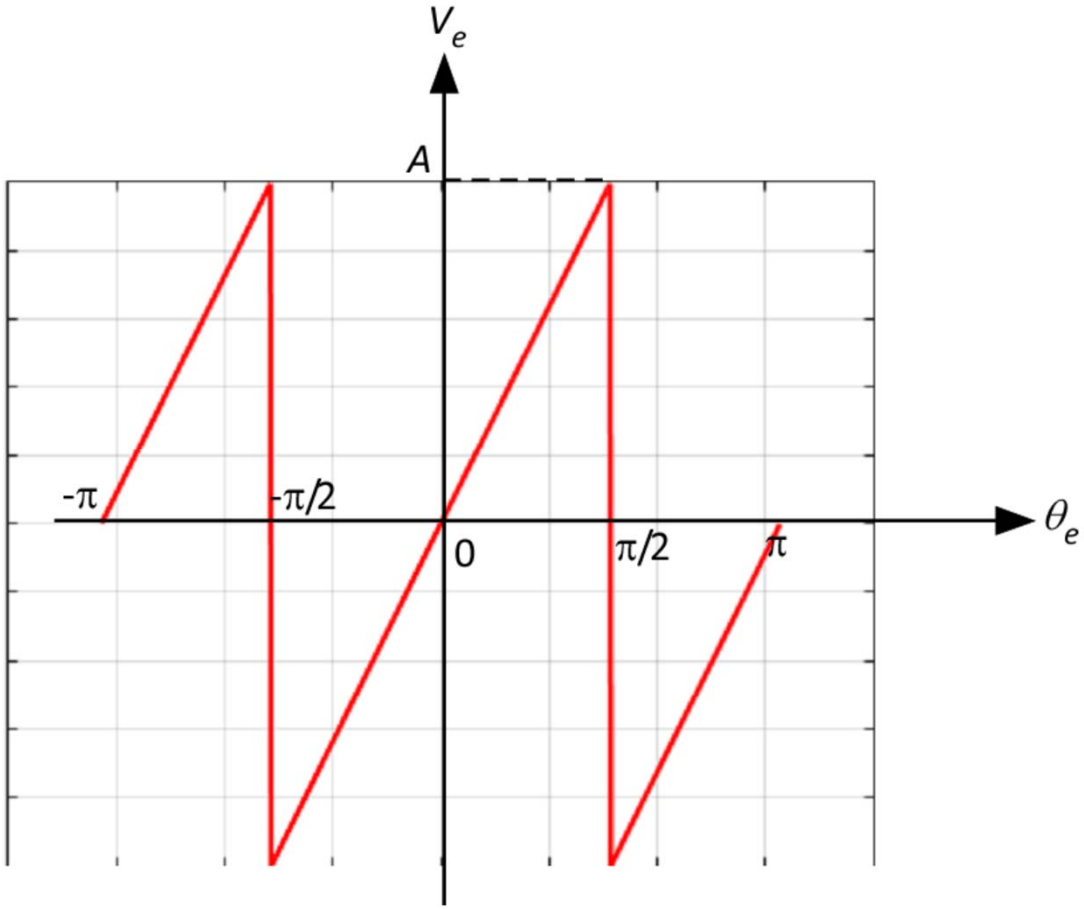
$$V_e \simeq A\theta_e \quad \Rightarrow \quad K_d = \frac{\Delta V_e}{\Delta \theta_e} \cong A = \frac{V_e}{\theta_e}$$

Phase Detector - Triangular



$$K_d = \frac{2A}{\pi}$$

Phase Detector - Sawtooth



$$K_d = \frac{A}{\pi}$$

Voltage-Controlled Oscillator

Output frequency is expressed by:

$$\omega_o = \omega_f + K_o V_d \ (rad/s)$$

Total angle of VCO can be described by:

$$\theta(t) = \int_0^t \left(\omega_f + \Delta\omega\right) dt = \omega_f t + \theta_o(t)$$

$\Delta\omega$ is deviation from ω_f

$$\theta_o(t) = \int_0^t \Delta\omega dt$$

DC Loop Gain

K_v = change in the oscillator frequency due to change in phase difference θ_e.

$$K_v = \frac{\Delta\omega_o}{\theta_e} = \frac{V_e}{\theta_e} \times \frac{V_d}{V_e} \times \frac{\Delta\omega}{V_d} = K_d \times K_a \times K_o$$

K_d = Phase detector gain factor
K_a = Amplifier gain
K_o = VCO gain factor

Phase Detector Mathematics

The phase detector is a mixer with

$$v_1(t) = V_1 \cos(\omega_{RF} t + \theta_1)$$

$$v_2(t) = V_2 \cos(\omega_{LO} t + \theta_2)$$

After mixing

$$v_p(t) = \frac{V_1 V_2}{2}\left[\begin{array}{l}\cos(\omega_{LO} t - \omega_{RF} t + \theta_2 - \theta_1) \\ +\cos(\omega_{LO} t + \omega_{RF} t + \theta_2 + \theta_1)\end{array}\right]$$

Phase Detector Mathematics

Define

$$\omega_{beat} = \omega_{LO} - \omega_{RF}$$

$$V_{pb} = \frac{V_1 V_2}{2}$$

$$\theta_e = \theta_2 - \theta_1$$ **Phase-error difference between signal 1 and signal 2**

We get

$$v_p(t) = V_{pb} \cos\left(\omega_{beat} t + \theta_e\right)$$

Phase Detector Mathematics

We have

$$v_p(t) = V_{pb}\cos(\omega_{beat}t + \theta_e)$$

When the loop is in lock, ω_{beat}= 0 and v_p is a DC voltage. When the loop is not in lock, v_p is a voltage that tries to pull the VCO into synchronism with the input signal.

Actual process of acquiring lock is nonlinear

Order of PLL

Highest power of *s* in denominator of closed-loop transfer function

First Order

$$H(s) = \frac{K}{s + a}$$

Second Order

$$H(s) = \frac{K}{s^2 + as + b}$$

Type of PLL

Number of poles at the origin for the open-loop transfer function

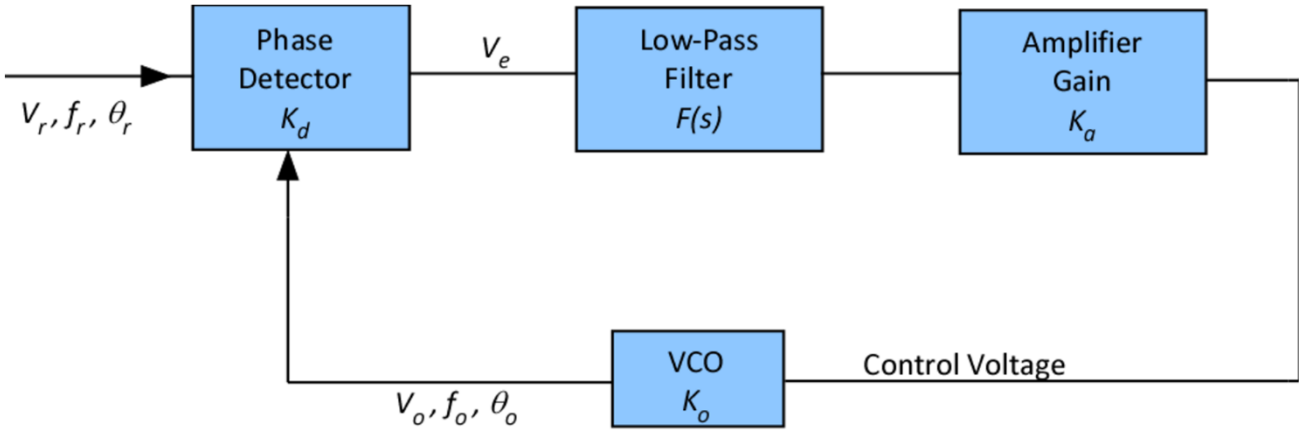
Type 1

$$A(s) = \frac{K}{s}$$

Type 2

$$A(s) = \frac{K}{s^2}$$

PLL Transfer Functions



$$H(s) = \frac{\theta_o(s)}{\theta_r(s)} = \frac{K_o K_d K_a F(s)}{s + K_o K_d K_a F(s)}$$

$$H_e(s) = \frac{\theta_e(s)}{\theta_r(s)} = \frac{s}{s + K_o K_d K_a F(s)}$$

Loop Transfer Function - No Filter

When there is no filter in the loop, *F(s) =1*, and

$$H(s) = \frac{K_o K_d K_a}{s + K_o K_d K_a} = \frac{K_o K_d K_a / s}{1 + K_o K_d K_a / s}$$ ← **First-order PLL**

which can be rewritten as

$$H(s) = \frac{\omega_L / s}{1 + \omega_L / s}$$

where

$$\omega_L = K_o K_d K_a$$ ← **loop bandwidth**

First-Order PLL

When there is no filter in the loop, *F(s) =1,* and

$$H_e(s) = \frac{\theta_e(s)}{\theta_r(s)} = \frac{s}{s + K_o K_d K_a}$$

For a step change in the input phase ($\Delta\theta_r/s$) the corresponding phase error is:

$$\theta_e(s) = \frac{s(\Delta\theta_r / s)}{s + K_o K_d K_a}$$

To find steady-state response, use final-value theorem for Laplace transforms

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\theta_e(s) = \lim_{s\to 0} \frac{s^2(\Delta\theta_r / s)}{s + K_o K_d K_a} = 0$$

First-order loop will eventually track phase change at input

First-Order PLL

For a step change in frequency, the resulting phase change will be a ramp ($\Delta\omega_r/s^2$) and the corresponding phase error is:

$$\theta_e(s) = \frac{s\left(\Delta\omega_r / s^2\right)}{s + K_o K_d K_a}$$

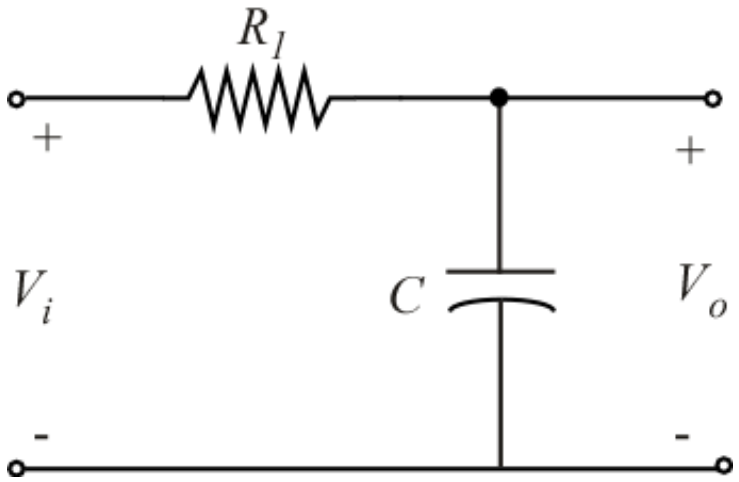
Use final-value theorem for Laplace transforms

$$\lim_{t\to\infty}\theta_e(t) = \lim_{s\to 0} s\theta_e(s) = \lim_{s\to 0}\frac{s^2\left(\Delta\omega_r / s^2\right)}{s + K_o K_d K_a} = \frac{\Delta\omega_r}{K_o K_d K_a}$$

Phase error is proportional to frequency change

➔ ***PLL can be used as FM demodulator!***

Loop Transfer Function - RC Filter



$$F(s) = \frac{V_o}{V_i} = \frac{1}{1 + s\tau}$$

$$\tau \equiv RC$$

$$H(s) = \frac{1}{\frac{s^2\tau}{K_o K_d K_a} + \frac{s}{K_o K_d K_a} + 1}$$

Loop Transfer Function - RC Filter

$$H(s) = \frac{1}{\frac{s^2\tau}{K_o K_d K_a} + \frac{s}{K_o K_d K_a} + 1}$$

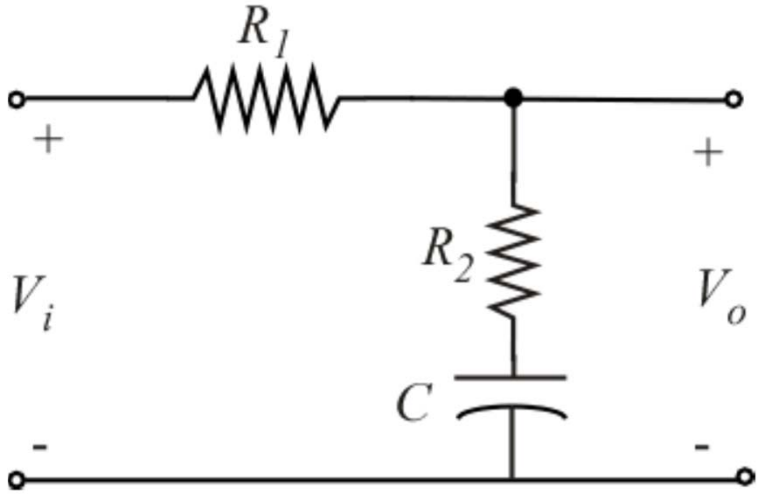
$$H(s) = \frac{1}{\frac{1}{\omega_n^2}s^2 + \frac{2\varsigma}{\omega_n}s + 1}$$

ζ: **damping factor**

ω_n: "natural frequency"

$$\omega_n = \sqrt{\frac{K_o K_d K_a}{\tau}} \qquad \varsigma = \frac{\omega_n}{2K_o K_d K_a} = \frac{1}{2\sqrt{\tau K_o K_d K_a}}$$

Loop Transfer Function - Lag-Lead Filter



$$F(s) = \frac{V_o}{V_i} = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}$$

$$\tau_1 \equiv R_1 C$$

$$\tau_2 \equiv R_2 C$$

$$H(s) = \frac{s\left(2\varsigma\omega_n - \omega_n^2 / K_o K_d K_a\right) + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$$

Loop Transfer Function - Lag-Lead Filter

$$H(s) = \frac{s\left(2\varsigma\omega_n - \omega_n^2 / K_o K_d K_a\right) + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$$

$$\tau_1 \equiv R_1 C$$

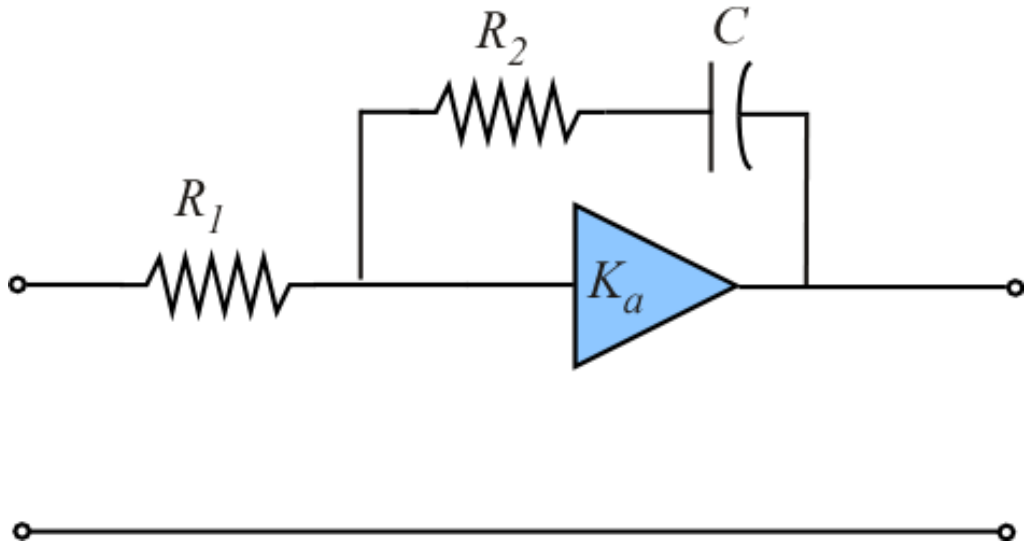
$$\tau_2 \equiv R_2 C$$

$$\omega_n = \sqrt{\frac{K_o K_d K_a}{\tau_1}} \qquad \varsigma = \frac{1}{2}\left(\frac{K_o K_d K_a}{\tau_1}\right)^{1/2}\left(\tau_2 + \frac{1}{K_o K_d K_a}\right) = \frac{\tau_2 \omega_n}{2} + \frac{\omega_n}{2 K_o K_d K_a}$$

ζ: damping factor

ω_n: "natural frequency"

PLL Transfer Function - Active Filter



$$\tau_1 \equiv R_1 C$$

$$\tau_2 \equiv R_2 C$$

$$F(s) = \frac{V_o}{V_i} = \frac{1 + s\tau_2}{s\tau_1}$$

PLL Transfer Function - Active Filter

$$H(s) = \frac{2\varsigma\omega_n s + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\frac{K_o K_d K_a}{\tau_1}}$$

$$\varsigma = \frac{\tau_2 \omega_n}{2}$$

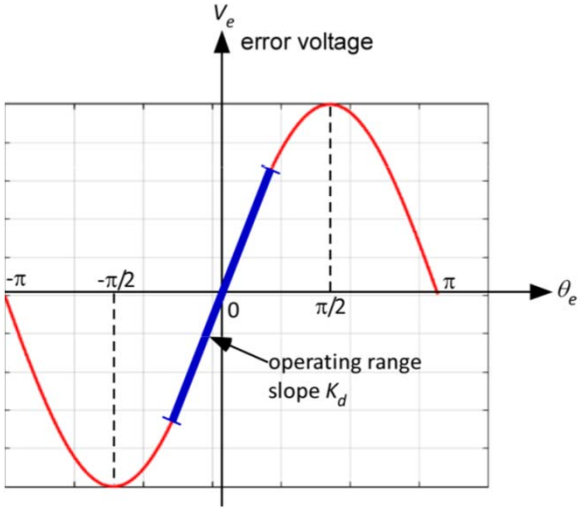
ζ: **damping factor**

ω_n: "natural frequency"

Hold in Range

Range over which we can change f_s and still have the loop remain in lock.

For sinusoidal phase detector



$$V_e = K_d \sin\theta_e$$

$$\sin\theta_e = \frac{V_e}{K_d} = \frac{V_e K_a K_o}{K_v} = \frac{\Delta\omega}{K_v}$$

Since sin θ_e cannot exceed ± 1 as θ_e approaches $\pm\pi/2$

The hold-in range is equal to the DC loop gain

$$\pm\Delta\omega_H = \pm K_v$$

Sinusoidal detector:

Max V_e is A and $A=V_d$

Lock in Range

Range of frequencies over which the loop will come into lock without slipping cycles.

- **If the frequency difference $|\omega_s - \omega_f|$ is less than the 3-dB bandwidth of the closed-loop transfer function *H(s)*, the loop will lock up without slipping cycles.**

$$\Delta\omega_L \approx \pm 2\zeta\omega_n$$ ⟵ **Maximum lock-in range**

Pull in Range

Range of frequencies over which the loop will eventually lock

- Once loop is in lock, small loop bandwidth is desirable to minimize noise transmission
- If initial frequency difference is outside lock-in range but inside pull-in range, difference-frequency waveshape is nonlinear and contains DC component that gradually shifts VCO frequency until lock up occurs

$$\Delta\omega_p \approx \pm\sqrt{2}\left(2\varsigma\omega_n K_v - \omega_n^2\right)^{1/2}$$

Transfer Function Representation

In general, the transfer function of an amplifier can be expressed as

$$H(s) = a_m \frac{(s - Z_1)(s - Z_2)\ldots(s - Z_m)}{(s - P_1)(s - P_2)\ldots(s - P_m)}$$

$Z_1, Z_2, \ldots Z_m$ are the **zeros** of the transfer function

$P_1, P_2, \ldots P_m$ are the **poles** of the transfer function

s is a complex number $s = \sigma + j\omega$

Transfer Function and Stability

H(s) can also be written in the form

$$H(s) = \frac{1 + a_1 s + a_2 s^2 + \ldots + a_n s^n}{1 + b_1 s + b_2 s^2 + \ldots b_n s^n}$$

The coefficients *a* and *b* are related to the frequencies of the zeros and poles respectively.

For a system to be stable all the poles and the zeros must reside on the left half of the s plane.

PLL Stability

The closed-loop transfer function *H(s)* can be expressed in terms of the open-loop gain *A(s)*

$$H(s) = \frac{A(s)}{1 + A(s)}$$

- **The loop is stable if the magnitude of the open-loop gain falls below 1 dB before its phase reaches 180°**
- **The greater the phase margin, the more stable the system and the higher the signal integrity**

PLL Stability

Let A(s) be the open-loop gain

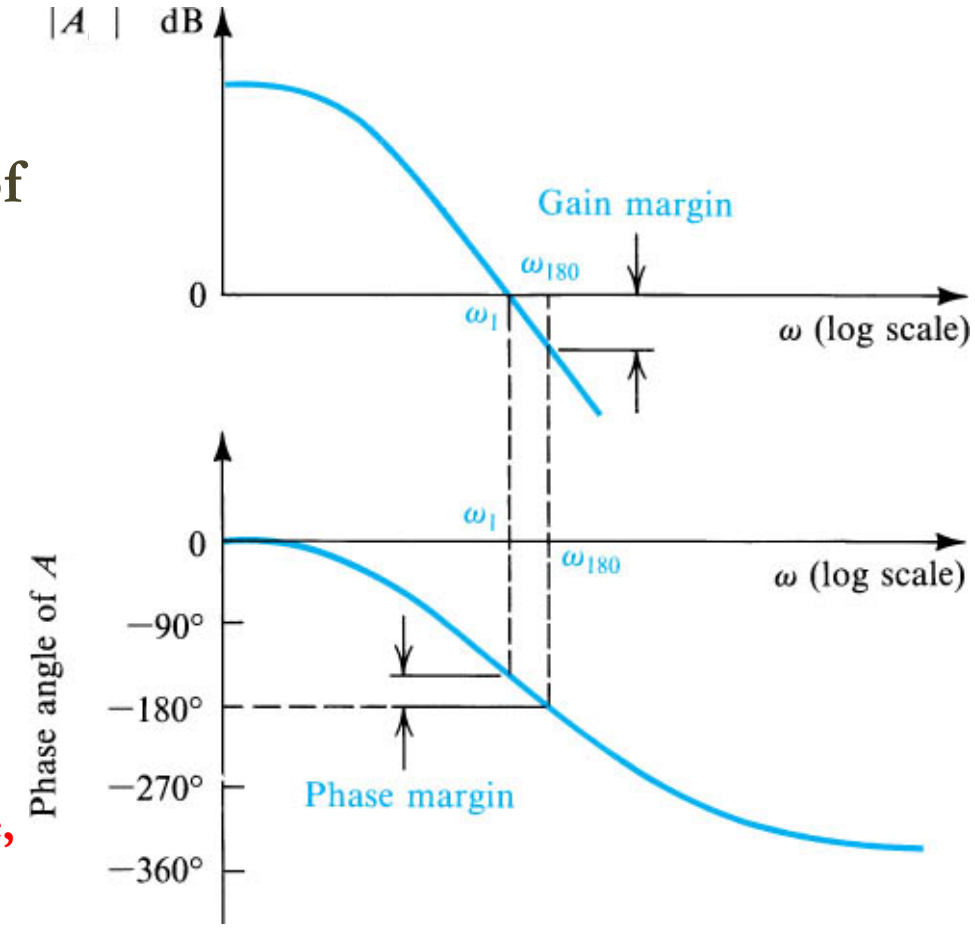
Gain Margin:

Difference between value of $|A(s)|$ at ω_{180} and unity

Phase Margin:

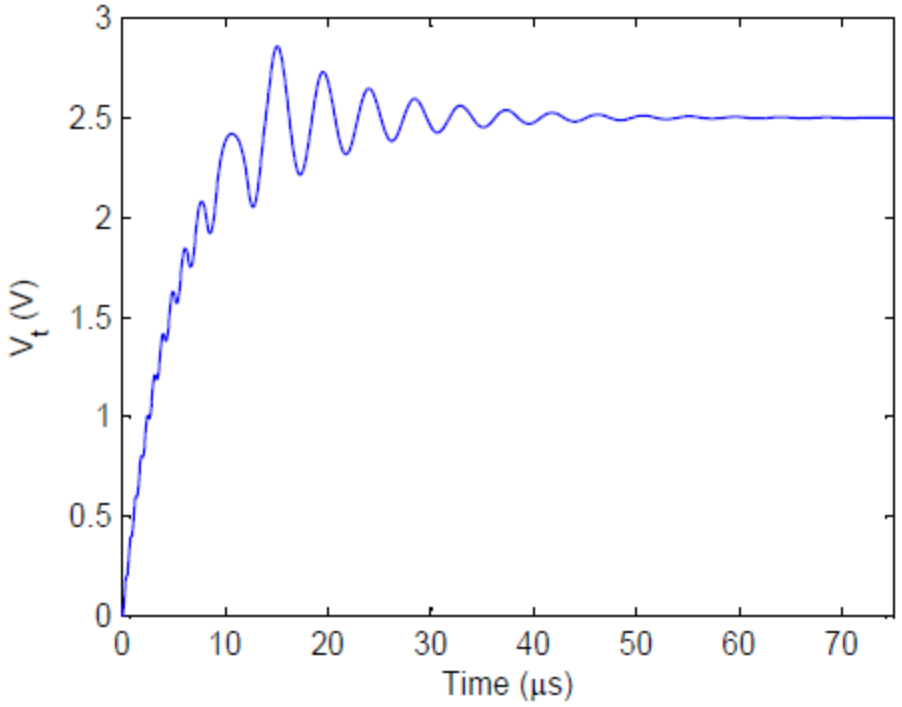
Difference between value of phase when $|A(s)|=1$ and 180^o

If phase angle at frequency when $|A(s)|=1$ is less than 180^o, loop is stable, otherwise, loop is unstable



PLL Operation – Acquisition

Tuning Voltage
During acquisition

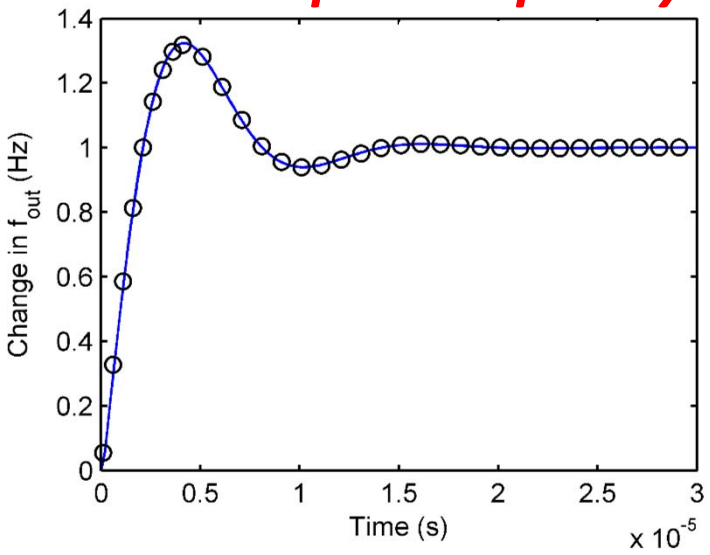


PLL Operation – Lock-In

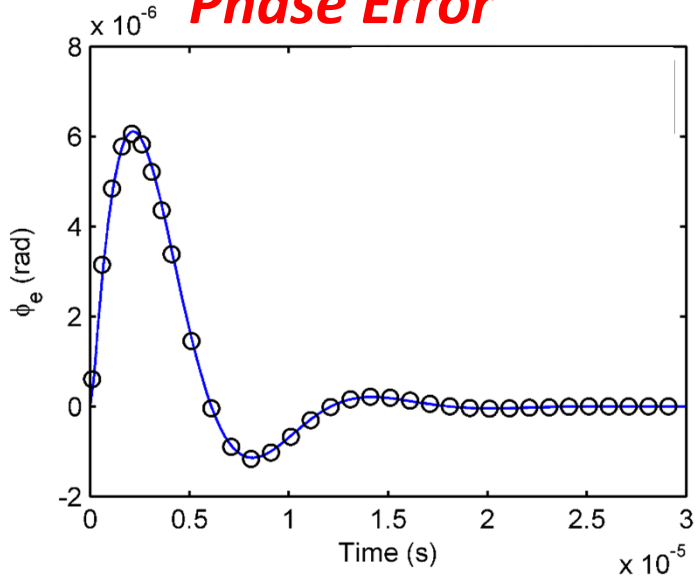
- PLL characteristics
  - $K_D = 5/(2\pi)$ V/rad, $K_V = 2\pi\,(3\times10^5)$ rad/V, $\tau_1 = 4.385\times10^{-6}$ s, $\tau_2 = 1.592\times10^{-6}$ s
- Small unit step change in $f_{in.}$
- PLL operates in the linear region:

$$\sin\phi_e(t) \approx \phi_e(t)$$

Output Frequency



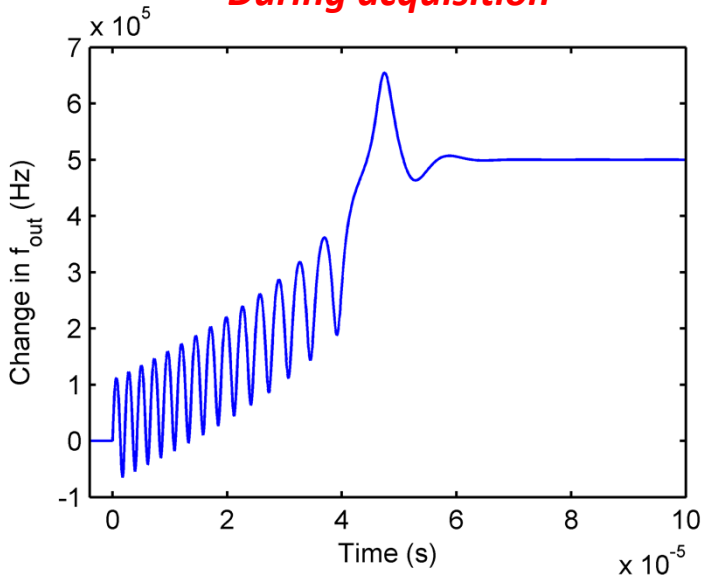
Phase Error



PLL Operation – Acquisition

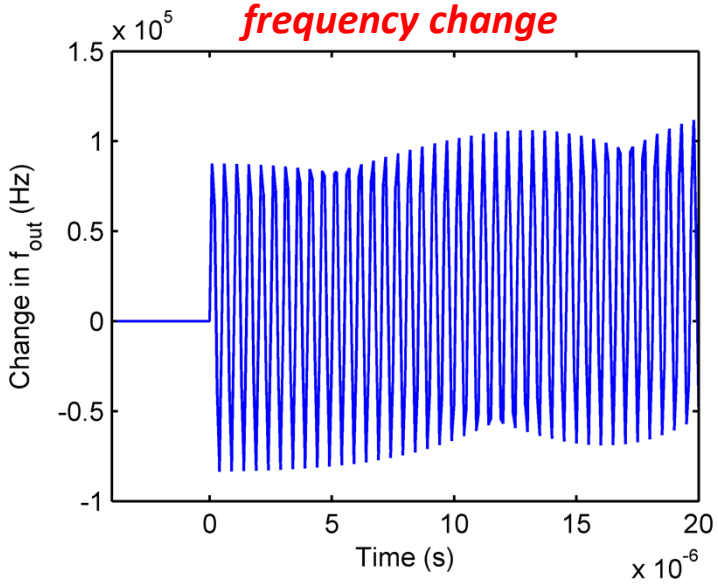
- Large change in $f_{in.}$
- PLL exhibits non-linear behavior:

Output Frequency During acquisition



5 kHz change in f_{in}. Pull-in/acquisition process.

Output Frequency For large step in frequency change

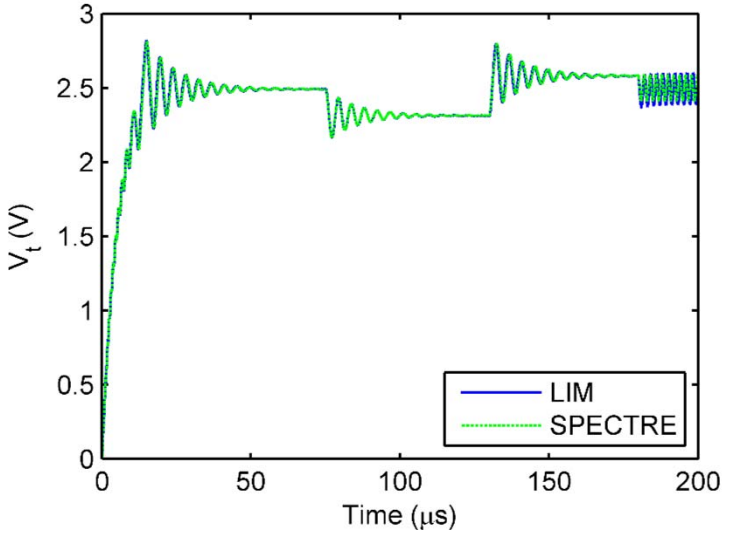


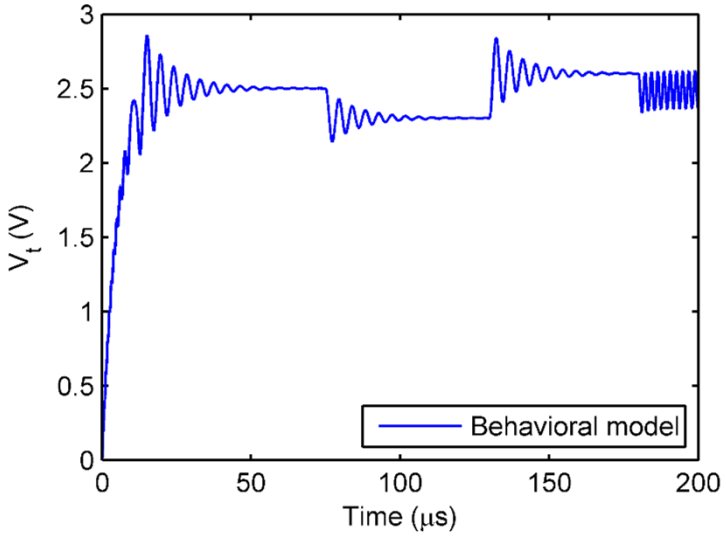
2 MHz change in f_{in}. Pull-out process. PLL no longer locks.

PLL Operation – Long Simulation

- Another example:
  - Long simulation (200 µs)

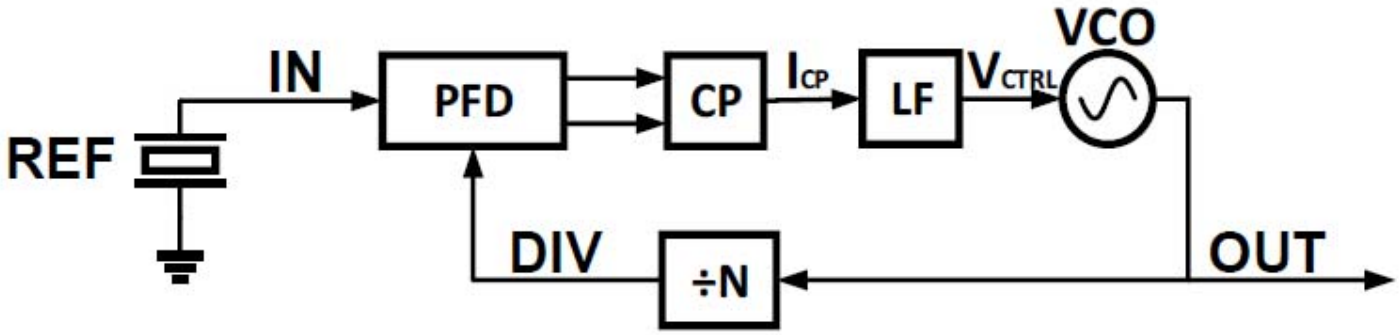
- Input:
  - 0 – 75 µs : 38.5 MHz
  - 75 µs – 130 µs : 38.3 MHz
  - 130 µs – 180 µs : 38.6 MHz
  - 180 µs – 200 µs : 38 MHz





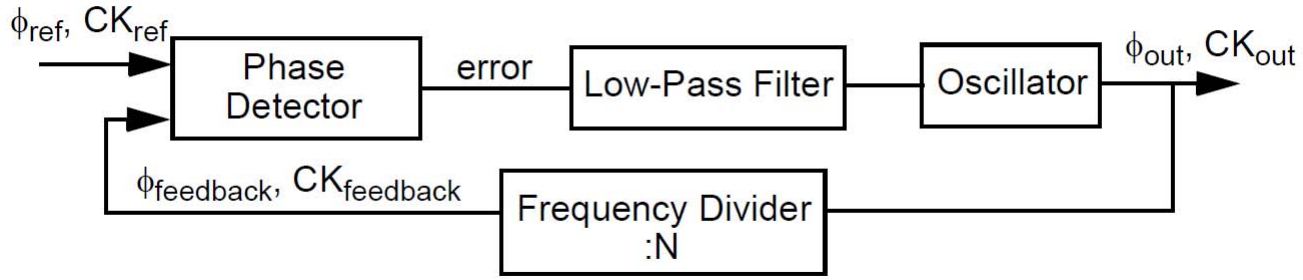
Clock Synthesizer

- PLL based clock-generating circuit needed to have a high-speed system master clock at the TX side.
- Reference clock generated by piezoelectric crystal but can only produce a stable, low-jitter clock in the MHz range.
- Basic Idea: take the reference signal and generate a scaled up clock at a higher frequency by eliminating static phase errors using a negative feedback control system in form of PLL.



PLL Overview

Basic PLL Block Diagram:



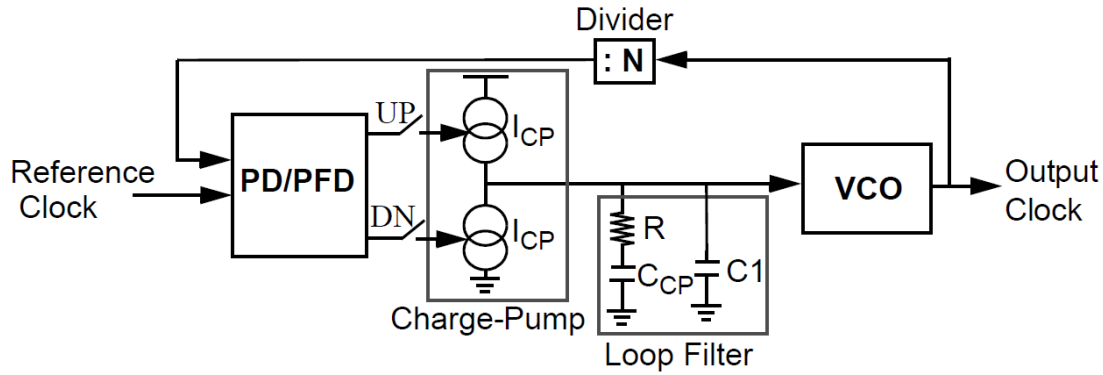
- Closed-loop feedback system that synchronizes the output CLK phase with that of the reference CLK.
- Tracks phase changes w/i the specified BW.
- Idea is that the PD (Phase Detector) will compare the reference CLK phase with that generated by the VCO.
  - Goal: Stabilize $\Delta\phi_e^{SS} \rightarrow 0$ such that VCO output CLK and reference CLK are locked at same frequency and phase.
  - Tracks low-frequencies but rejects high-frequencies.

Why need PLLs?

- Reduces jitter.
- Reduces clock-skew in high-speed digital ckts.
- Instrumental in frequency synthesizers.
- Essential building block of CDRs.

PLL Building Blocks

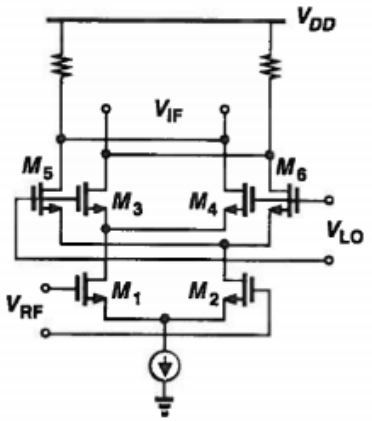
Basic PLL Components:



- PD/PFD ~ Phase/Phase+Frequency Detector
- CP ~ Charge pump circuit
- LF ~ Loop-Filter
- VCO ~ Voltage controlled oscillator
- Frequency Divider

PD/PFD Circuits

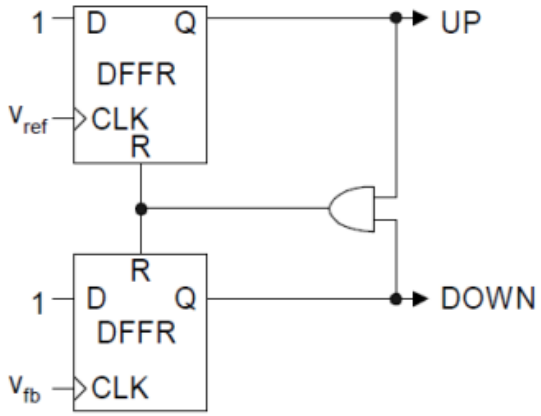
Common PD Implementations:



Gilbert-cell Mixer

XOR PD

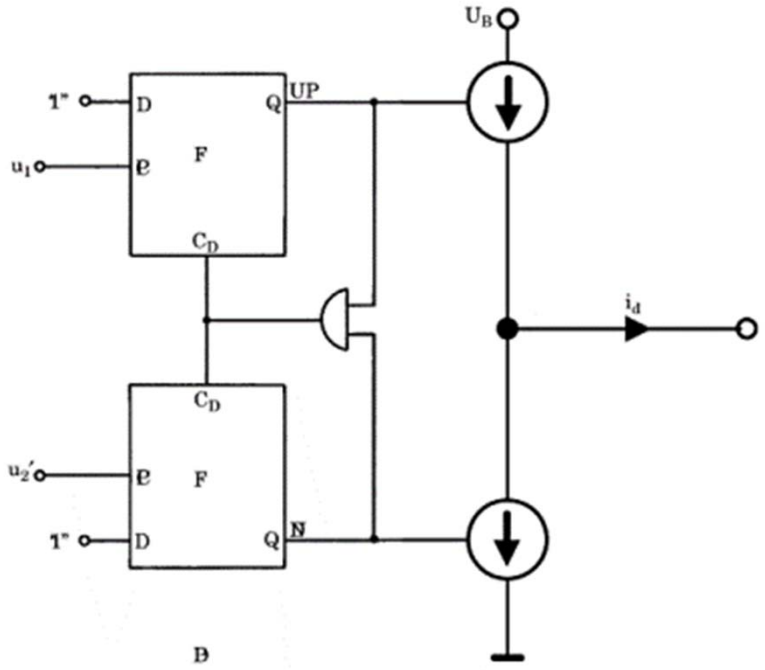
Common PFD Implementations:

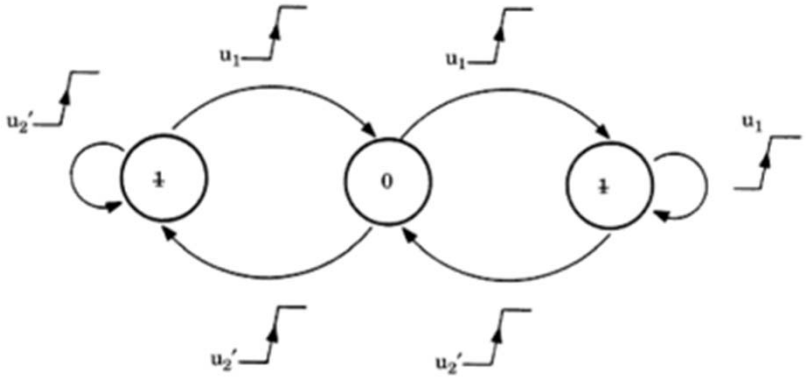


- PD/PFD are strictly digital circuits in high speed SerDes transceivers.
- Ideal PD is a "multiplier" in time-domain, ex: Mixer
- Analog PD → High Jitter, noise.
- XOR PD → sensitive to clock duty cycle
- PFD ~ best to lock phase and frequency!

PFD Theory

1. PFD is needed to adjust the control voltage for VCO according to the phase difference between the VCO output and reference frequency

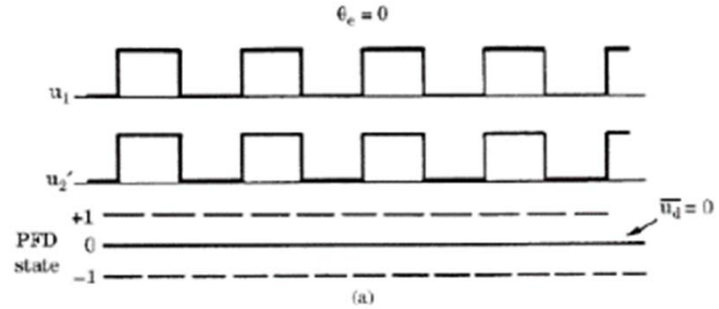




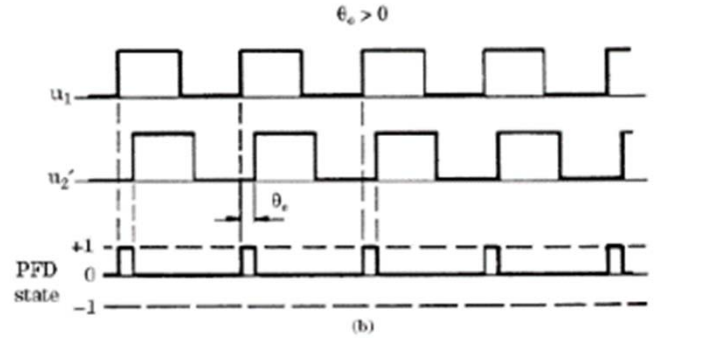
2. PFD can be seen as a state machine with three states. It will change the control voltage of VCO according to its current state and phase/frequency difference will cause state transition.

PFD Analysis

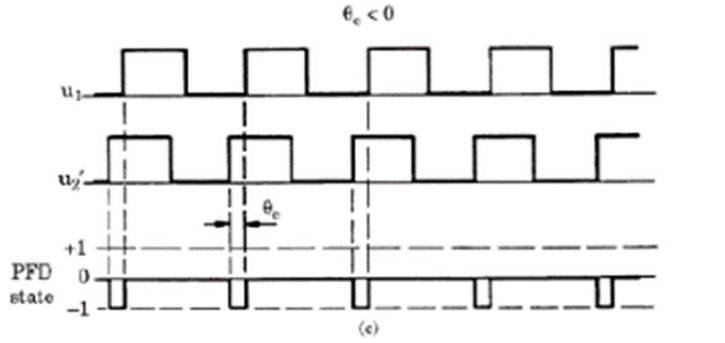
1. PFD is in state 0 with no phase difference.



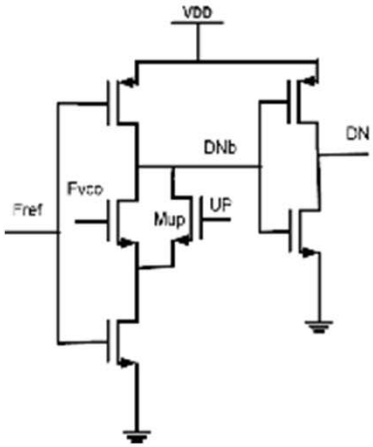
2. PFD is in state 1 with positive phase difference.



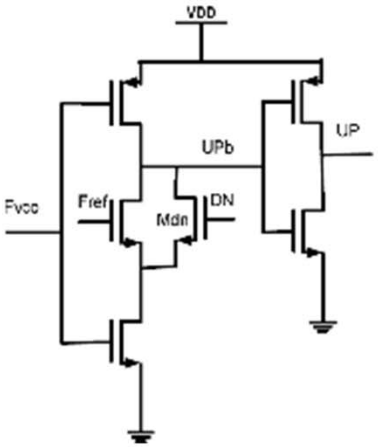
3. PFD is in state -1 with negative phase difference.



PFD Design Overview

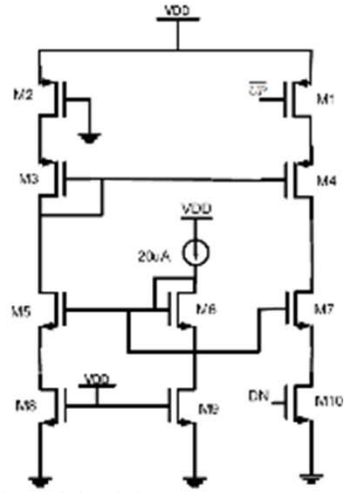


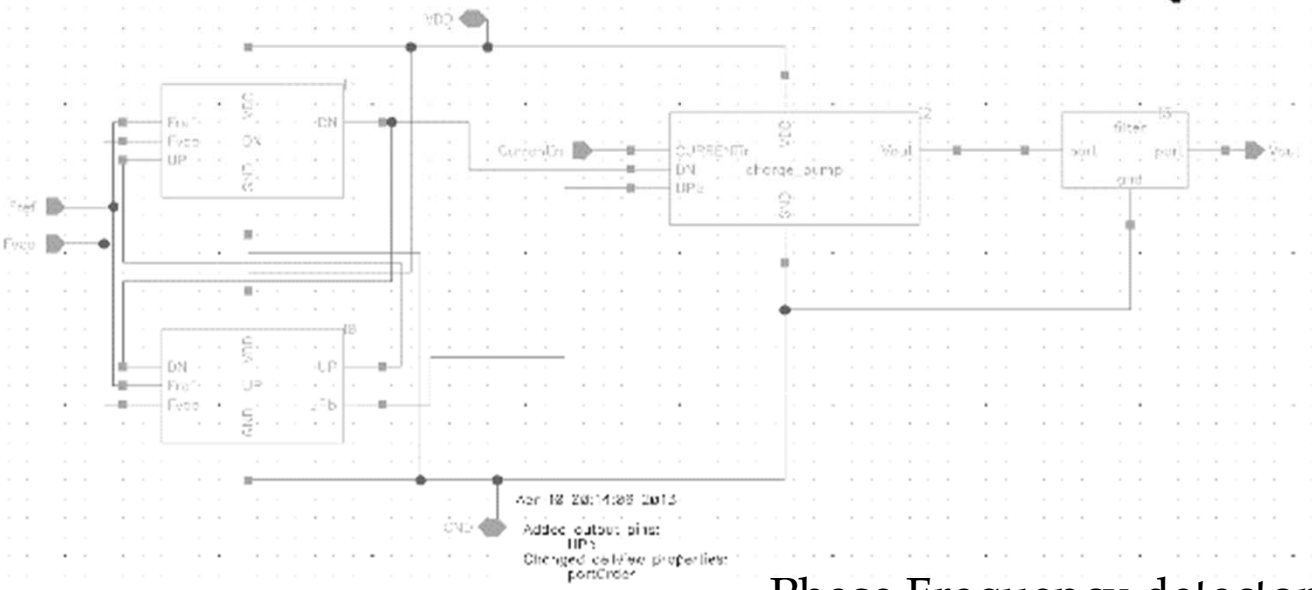
Down circuit



UP circuit

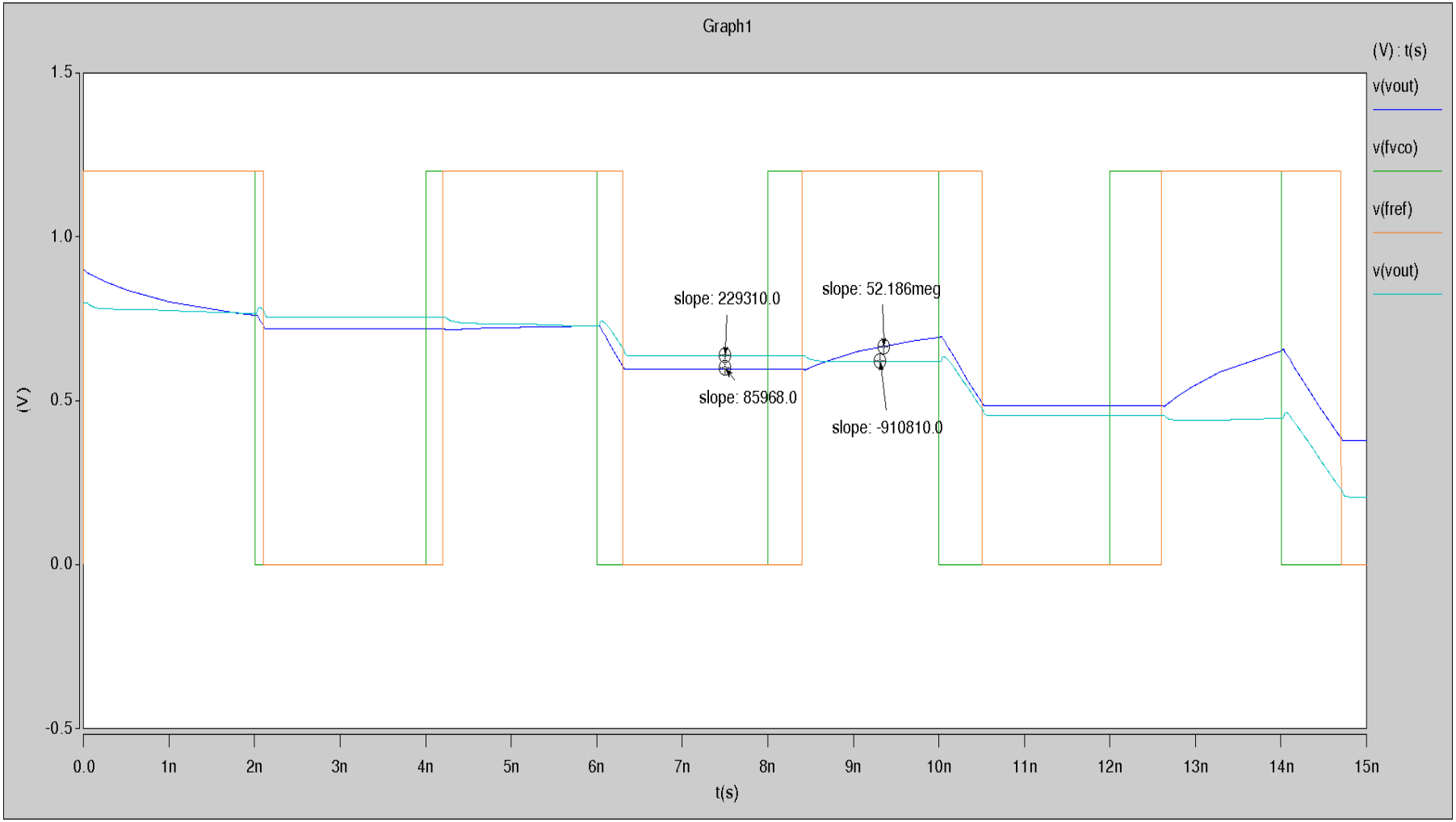
Charge pump





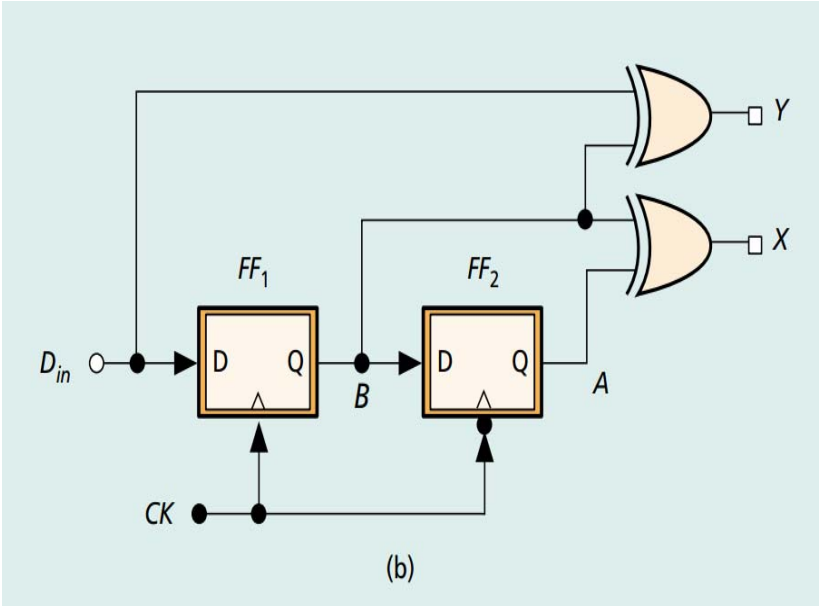
Phase Frequency detector

PFD Simulation



The Hogge Phase Detector

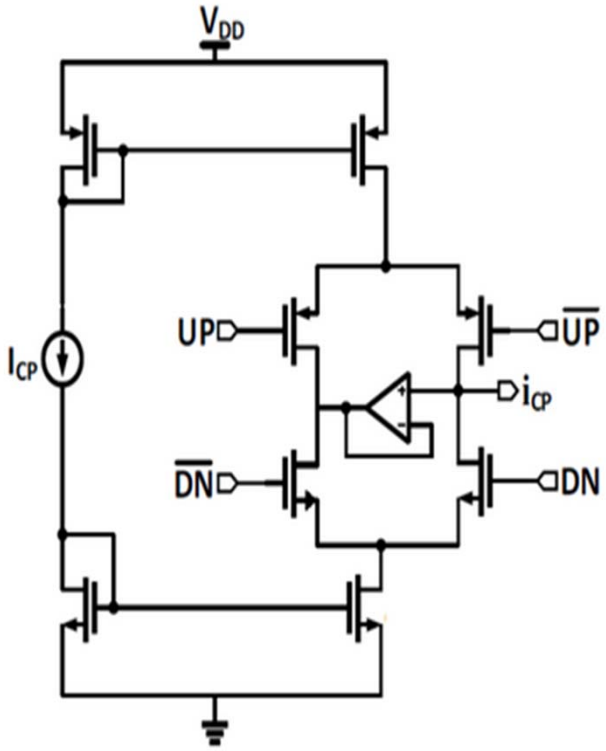
- Two Functions
  - Transition detection
  - Phase Detection



The Charge Pump

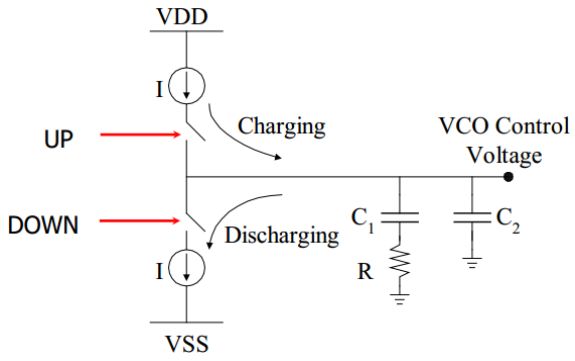
- Combination of current source and sink
- Converts PD output

UP	DN	Io
0	0	0
1	0	Icp
0	1	-Icp

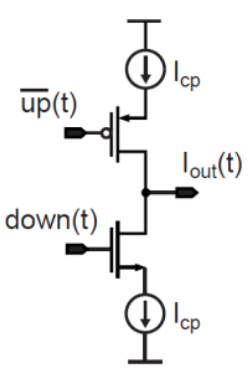


Charge-Pump Circuit

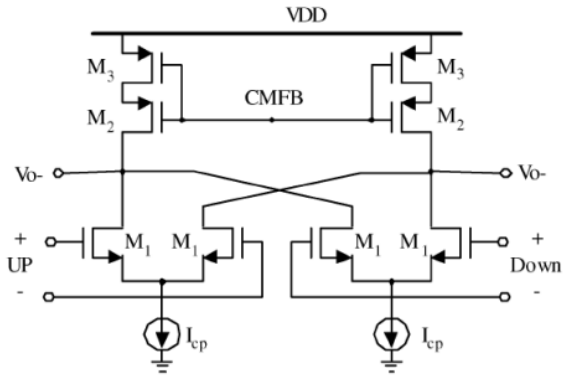
Common CP Implementations:



Single-Ended



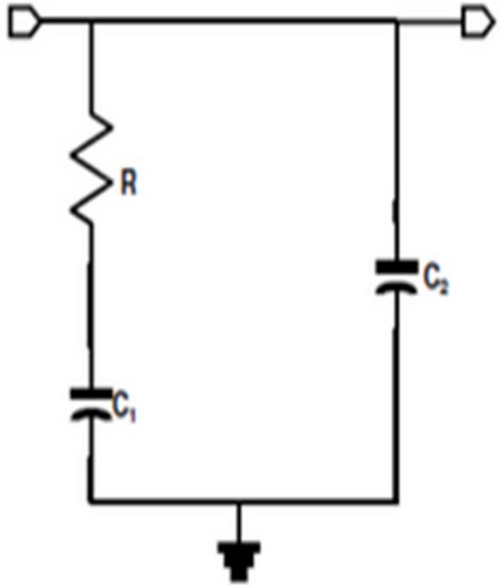
Fully Differential



- Used in conjunction with PFD over PD+LF combo. b/c:
  - Higher capture/lock acquisition range of PLL
  - $\Delta\phi_e^{SS} = 0$ provide no device mismatch exists.
  - Provide infinite gain for a static phase-error

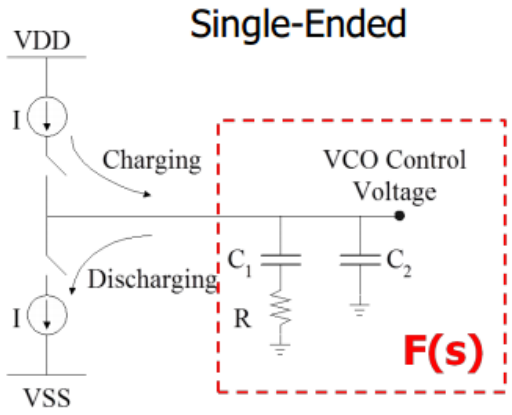
The Loop Filter

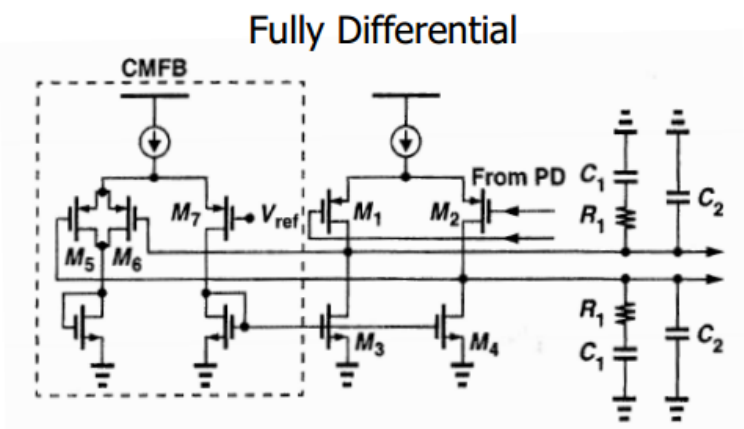
- Low-pass for rejection of high frequency noise
- Forms the control voltage of the VCO



Loop-Filter

Common LF Implementations:



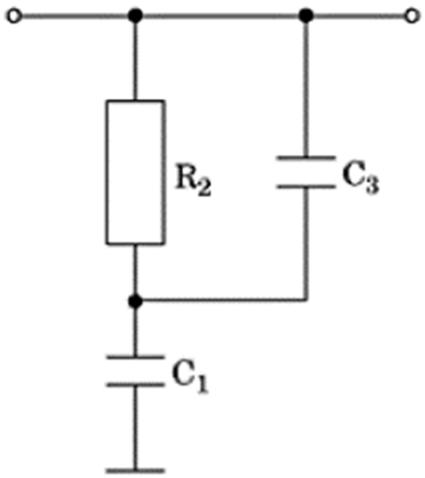


- Extracts average of PD error signals generate VCO control voltage.
- Integrates low-frequency phase-errors on C1 to set avg. freq.
- R adds thermal noise, C_1 determines loop BW, C_2 smoothens control voltage ripple.

Loop-Filter Design

1. Needed to filter out high frequency noise generated by PFD

2. Due to the superior performance of PFD, only a passive second order RC low pass filter is needed.



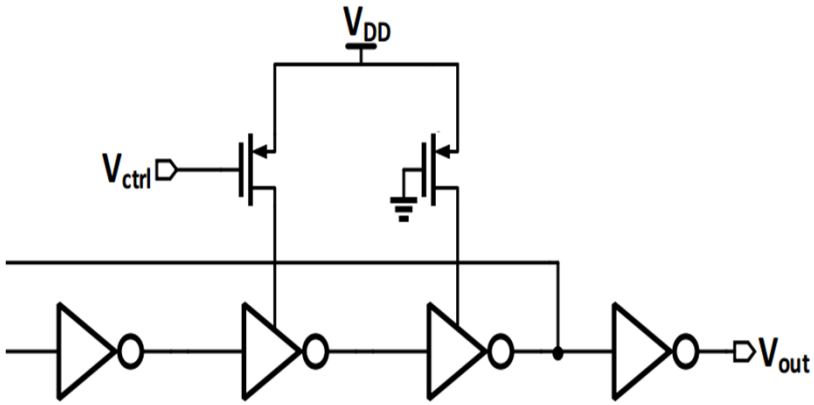
Low pass filter for current input

Where $R_2 = 70.18K\Omega, C_1 = 72.56\text{f}F, C_3 = 18.136\text{f}F;$

Assuming $K_0 = 4.5\,GHz/V\,;\; K_P = 3.183\mu A/rad\,, N = 8, \omega_T = 25\text{MHz}$

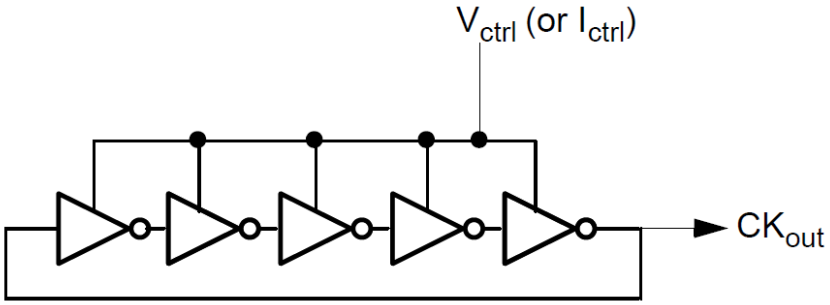
Voltage Controlled Oscillator

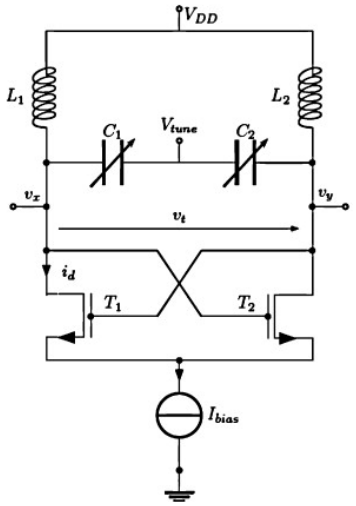
- Generates an output with oscillation frequency proportional to the control voltage
- Helps the CDR accumulate phase and achieve lock



VCO

Common VCO Implementation:

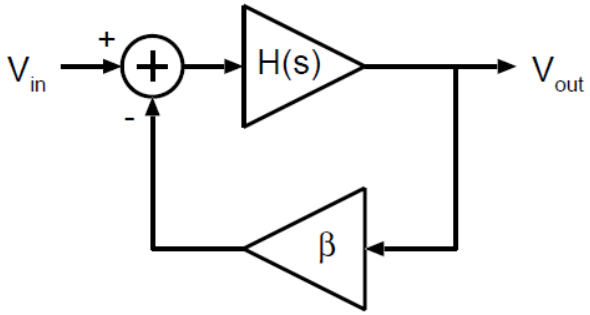




LC-Tank Oscillator

- Extracts average of PD error signals generate VCO control voltage.
- PLL acts like a High-pass filter with respect to VCO jitter.
- VCO always has one pole!

Oscillators Overview



- Closed-Loop Transfer function:

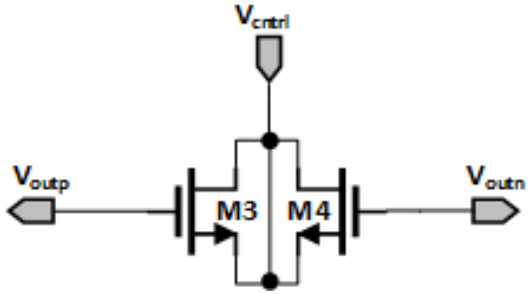
$$-\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+\beta H(s)}, where\ s = j\omega$$

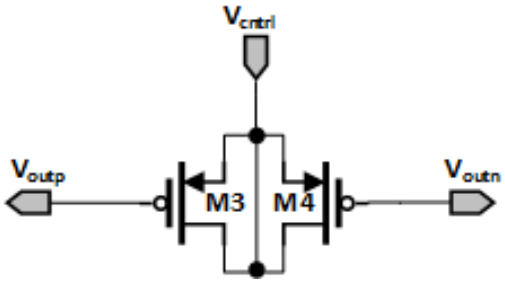
- Barkhausen's criteria for oscillation:
  - $|\beta H(j\omega_0)| = 1$
  - $\arg(\beta H(j\omega_0)) = -180^0$.
- ω_0 = oscillation-frequency.

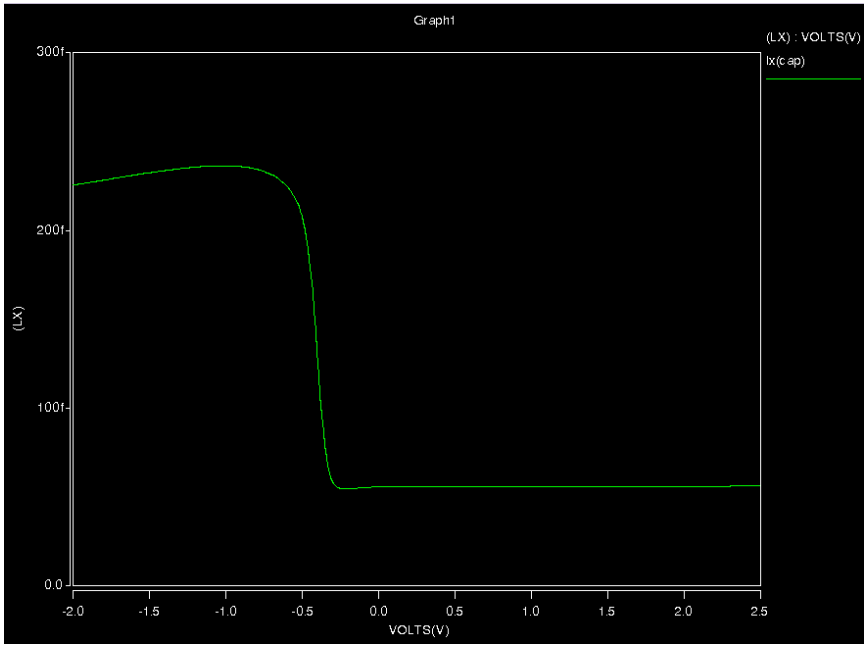
Ring v/s Tank Architecture

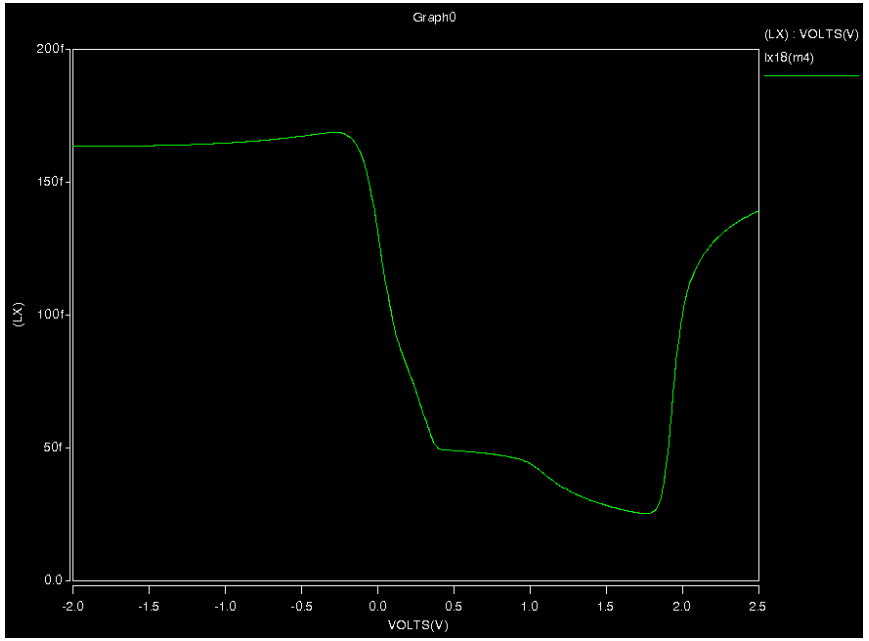
Ring Structure	LC-Tank Structure
1. Low-power, highly integrated.	1. High-power, not integrable.
2. Occupies smaller die-area.	2. Occupies large die-area.
3. Poor-performance at high-frequency due to large phase-noise + jitter.	3. Great phase-noise and jitter performance at high frequency.
4. Can only accept digital signals.	4. Can accept analog and digital signals.

MOS Varactor

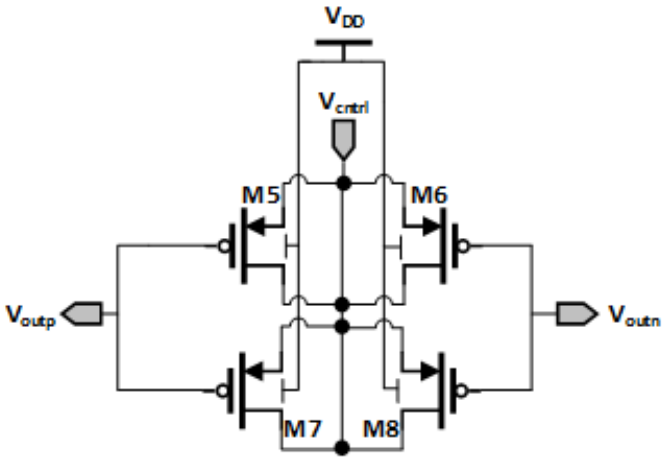


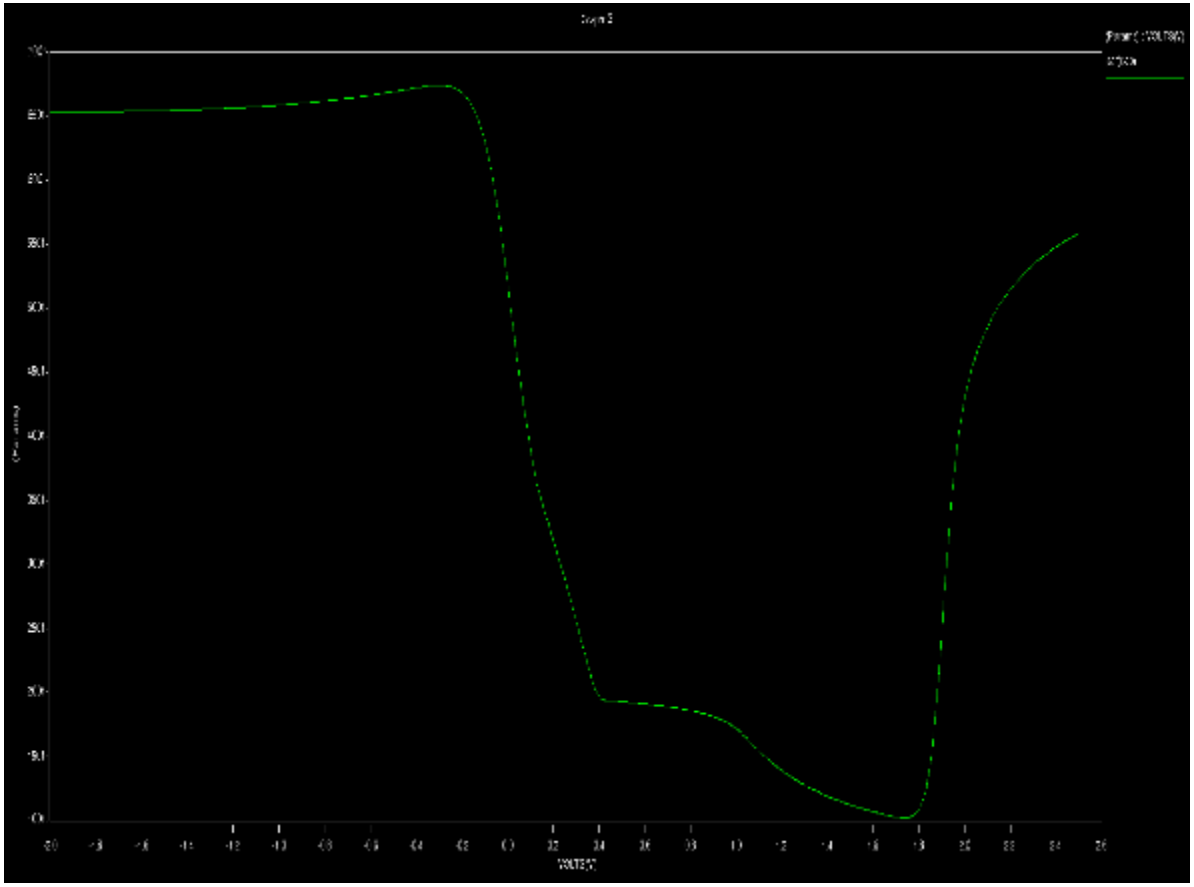




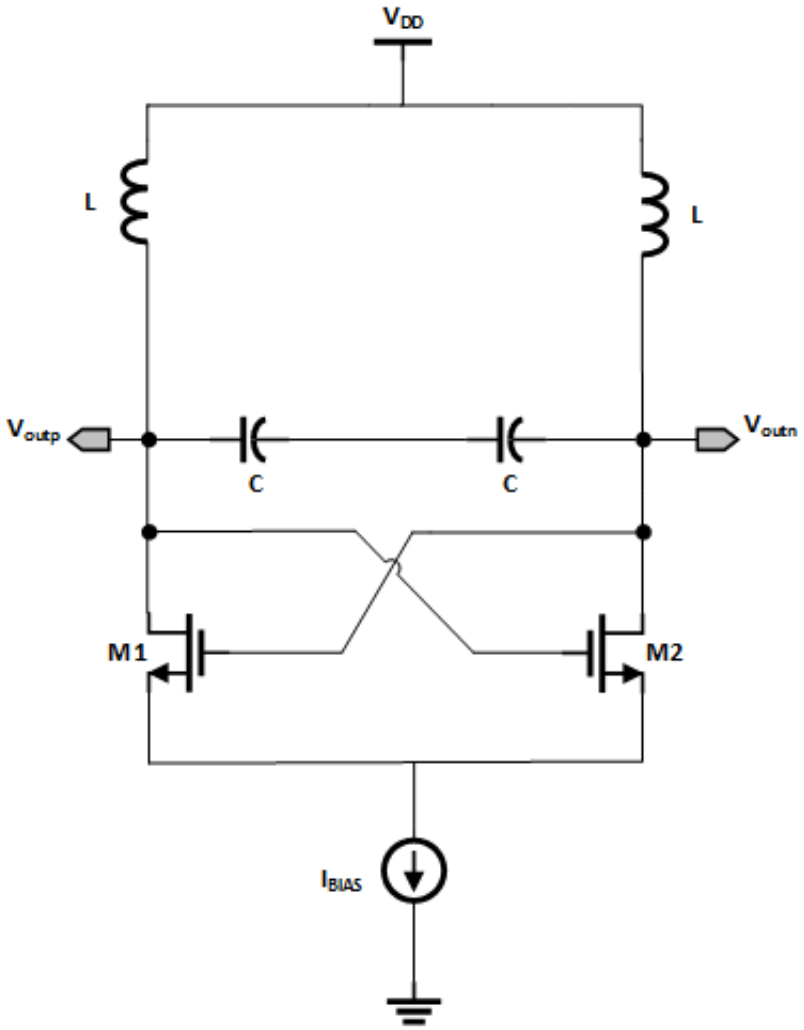


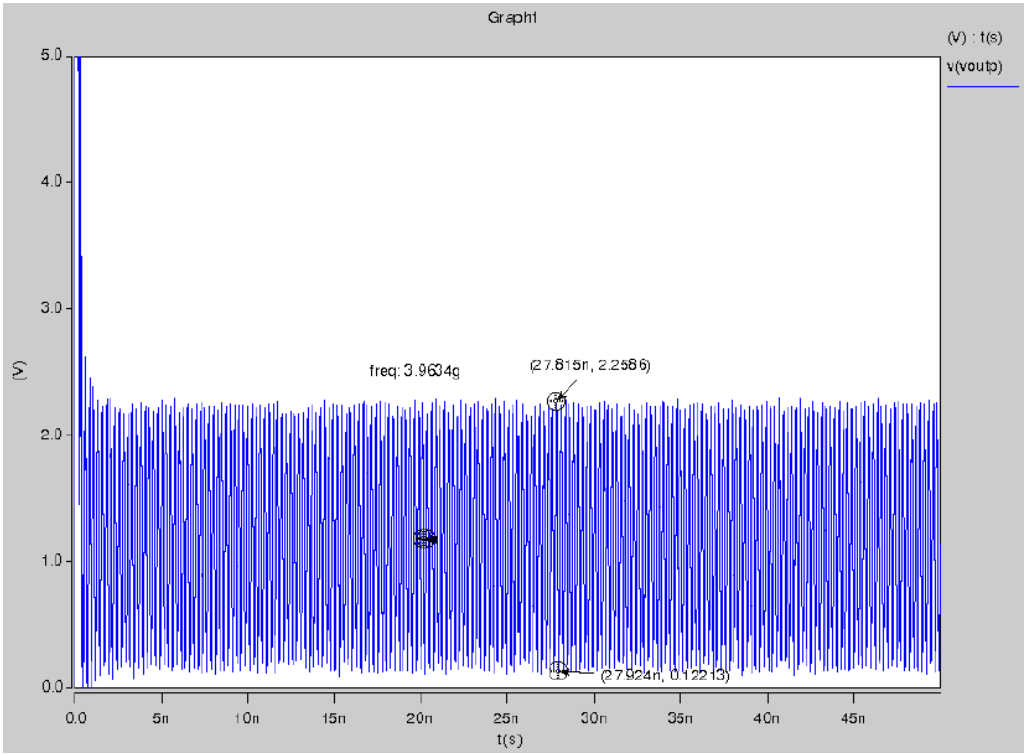
Cascode MOS Varactor



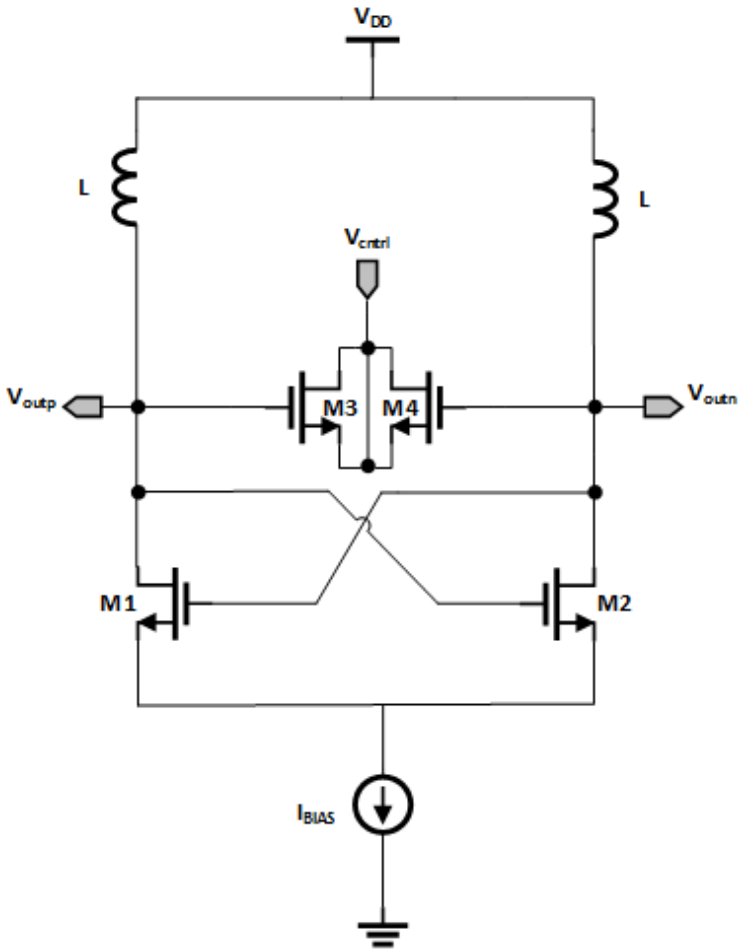


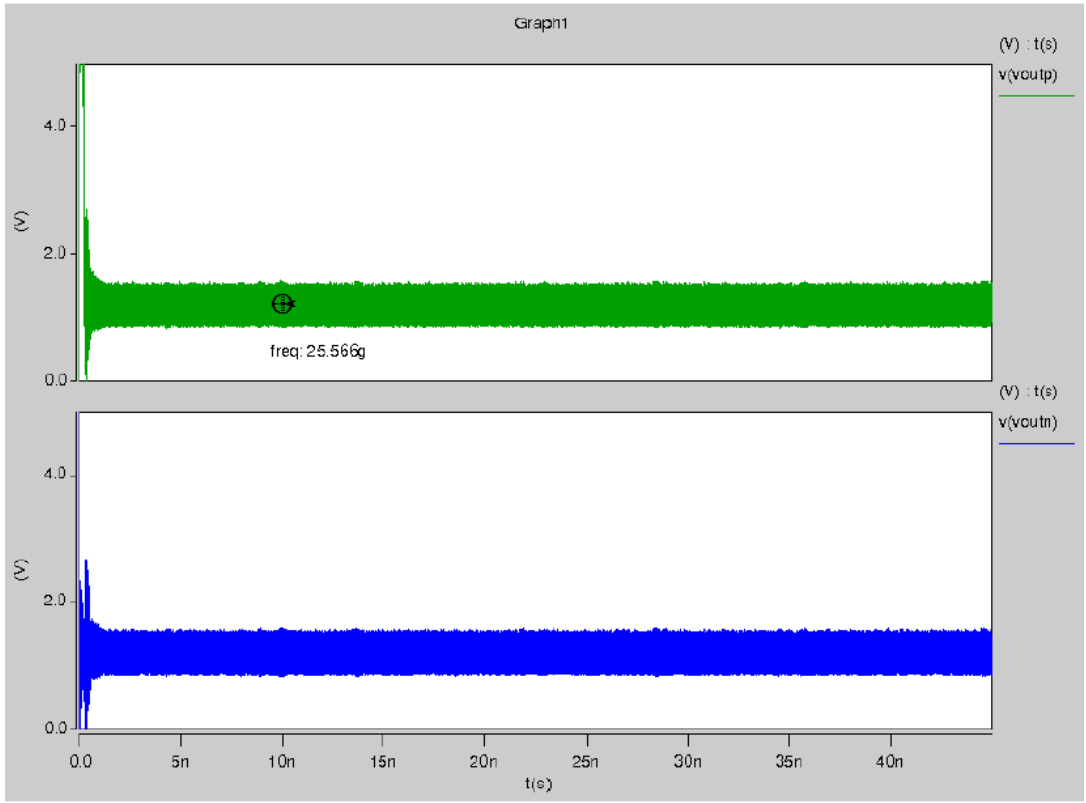
LC-Tank VCO Designs - I



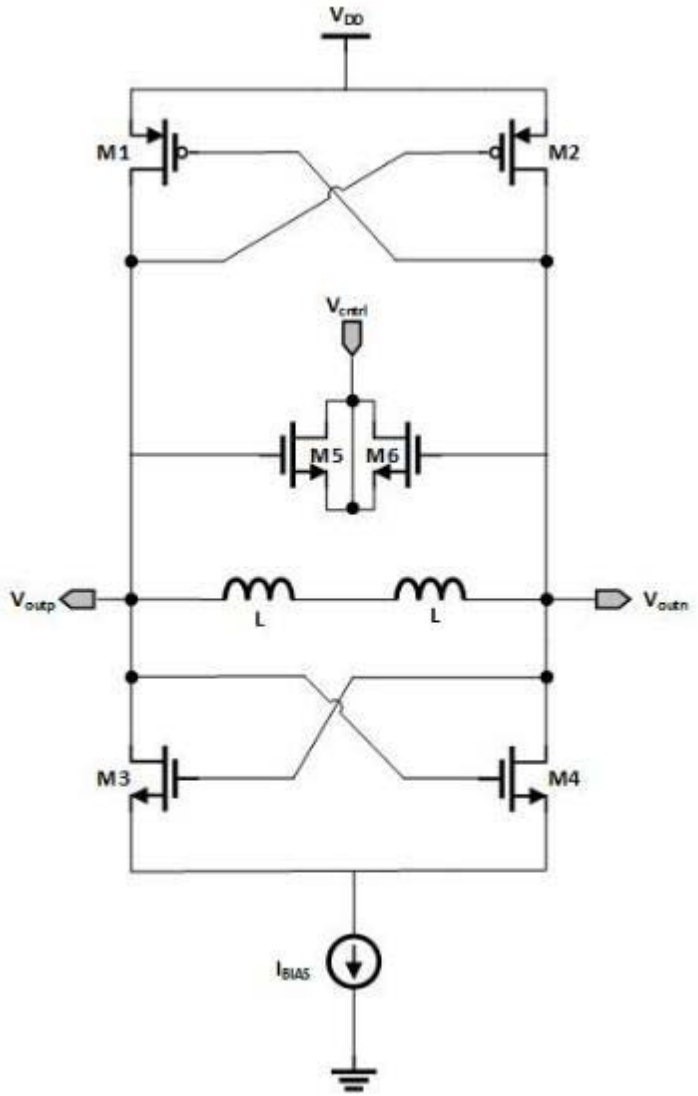


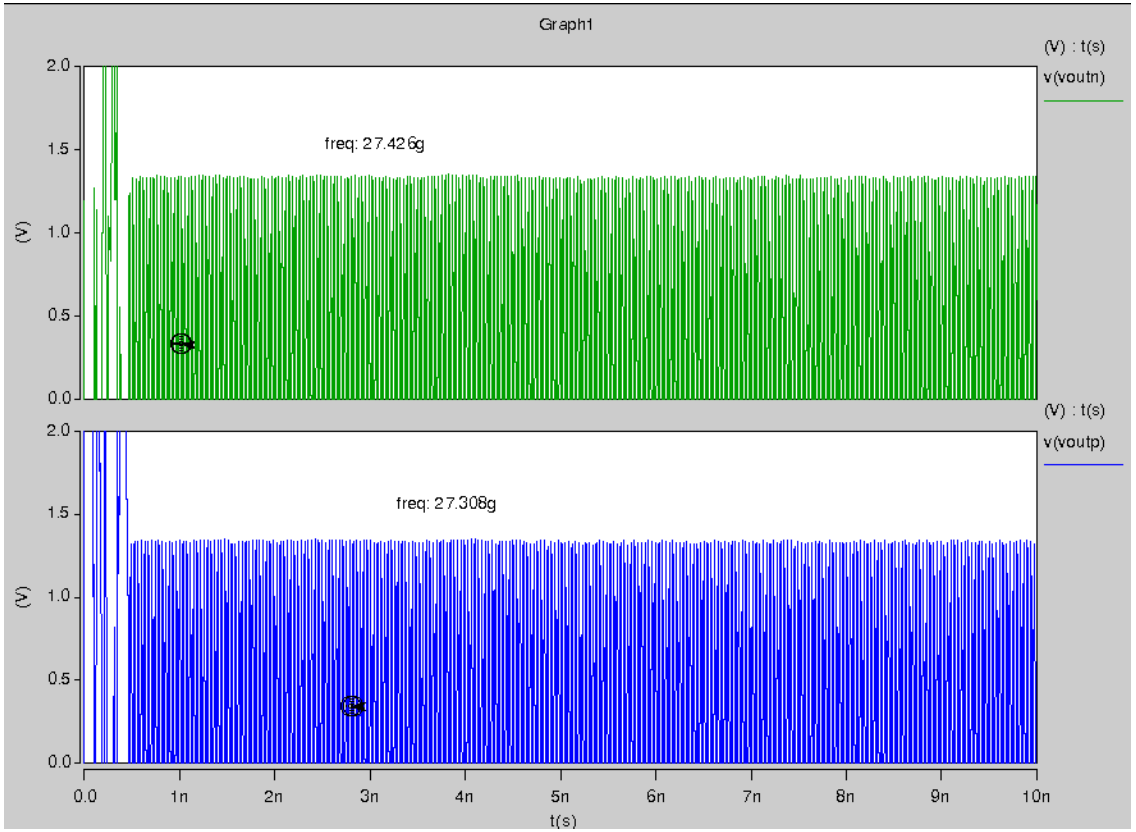
LC-Tank VCO Designs - II



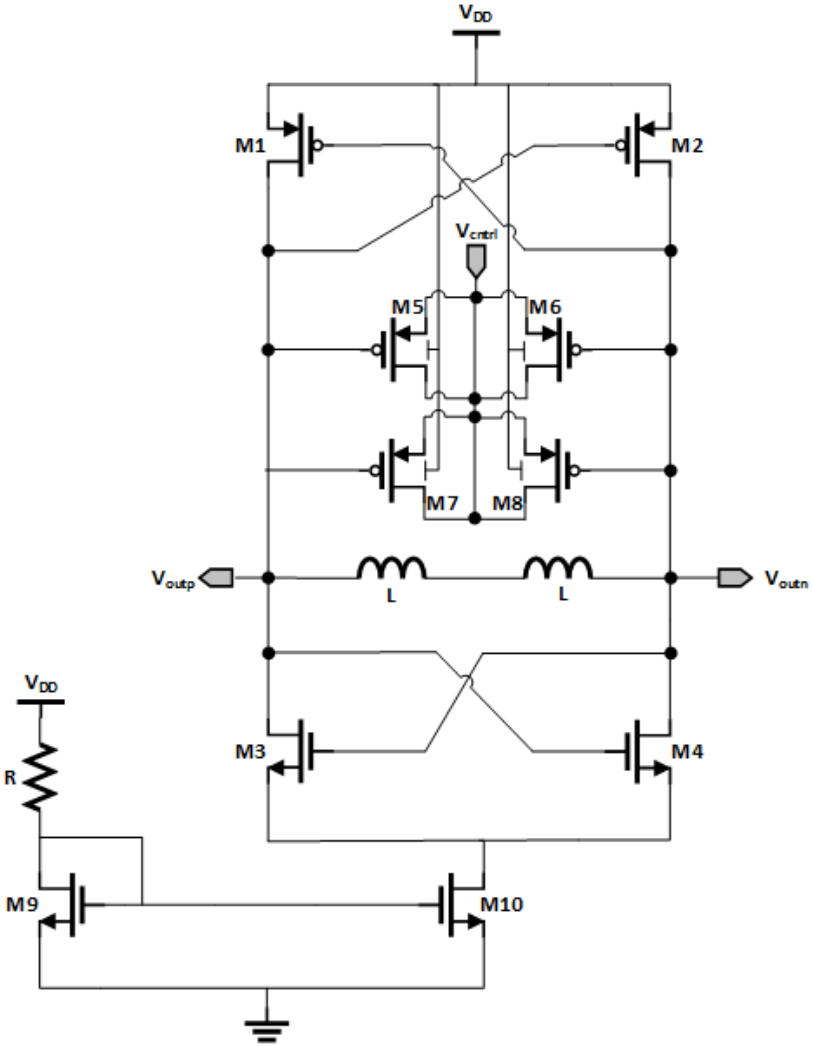


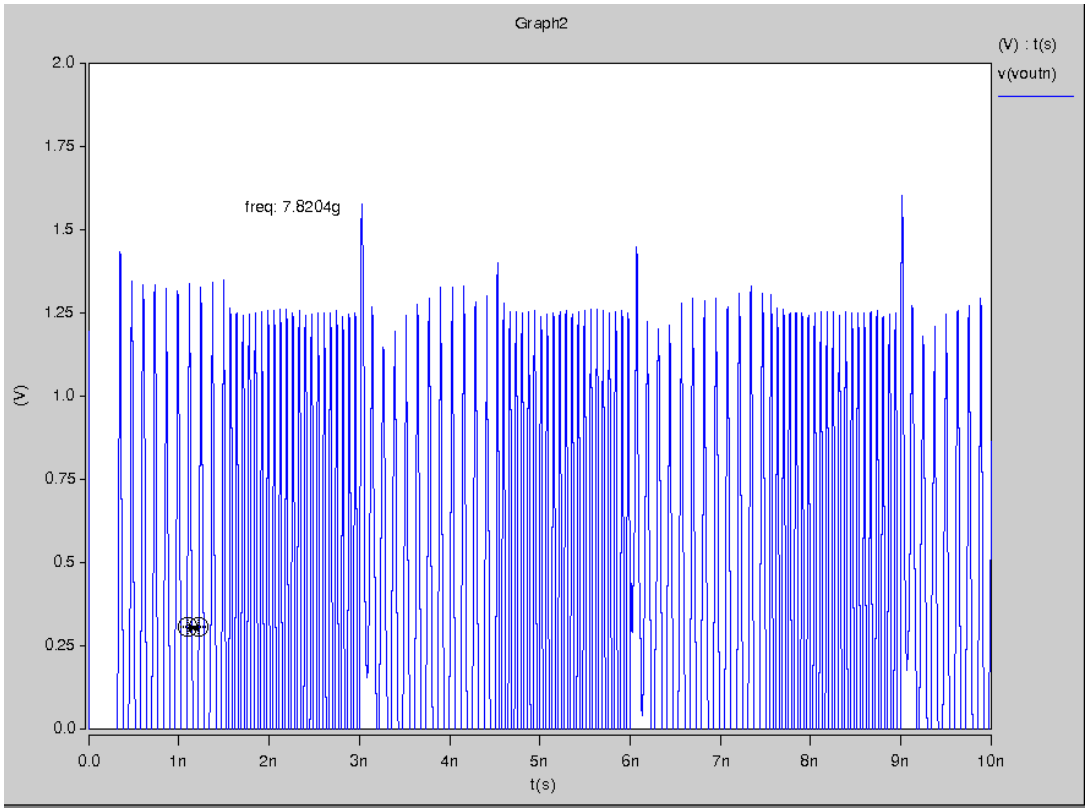
LC-Tank VCO Designs - III





LC-Tank VCO Designs - Final

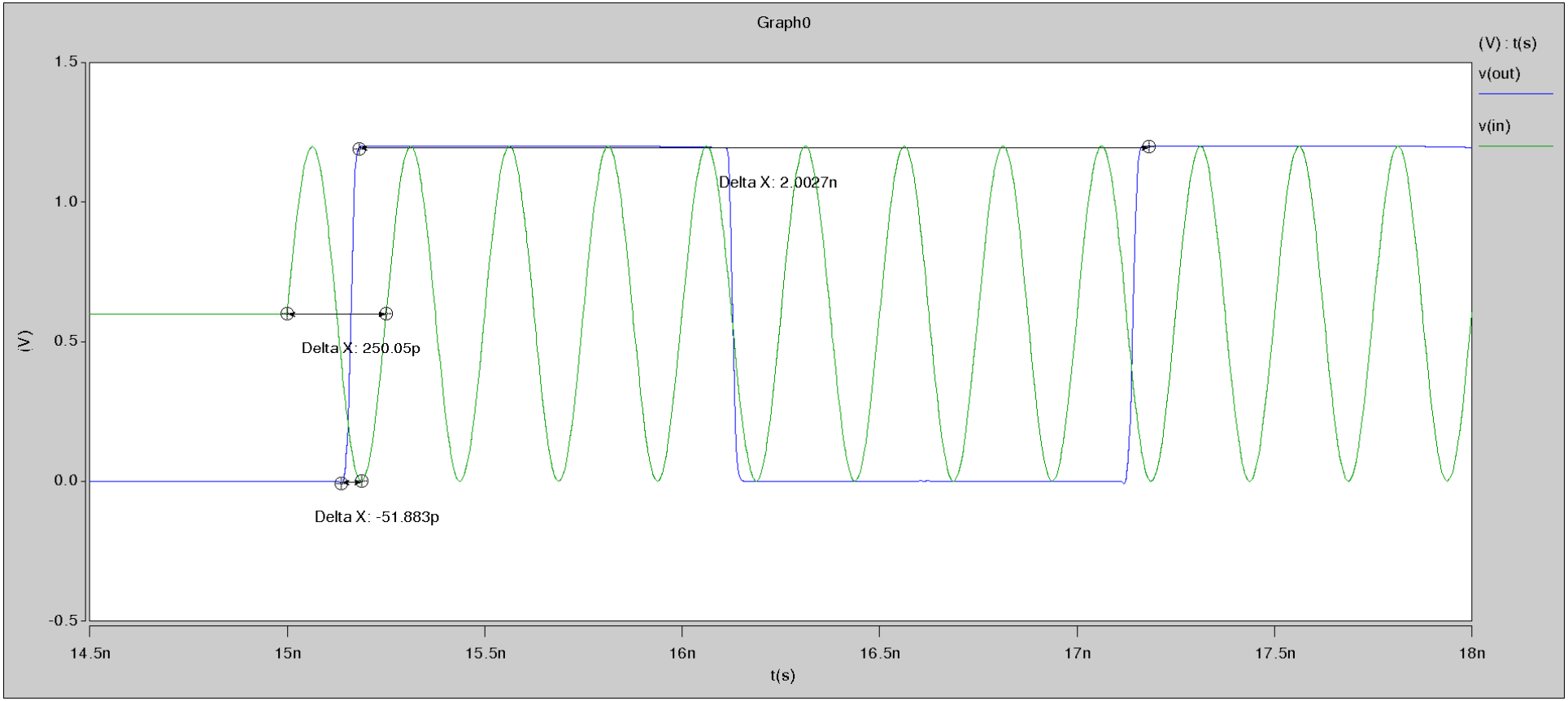




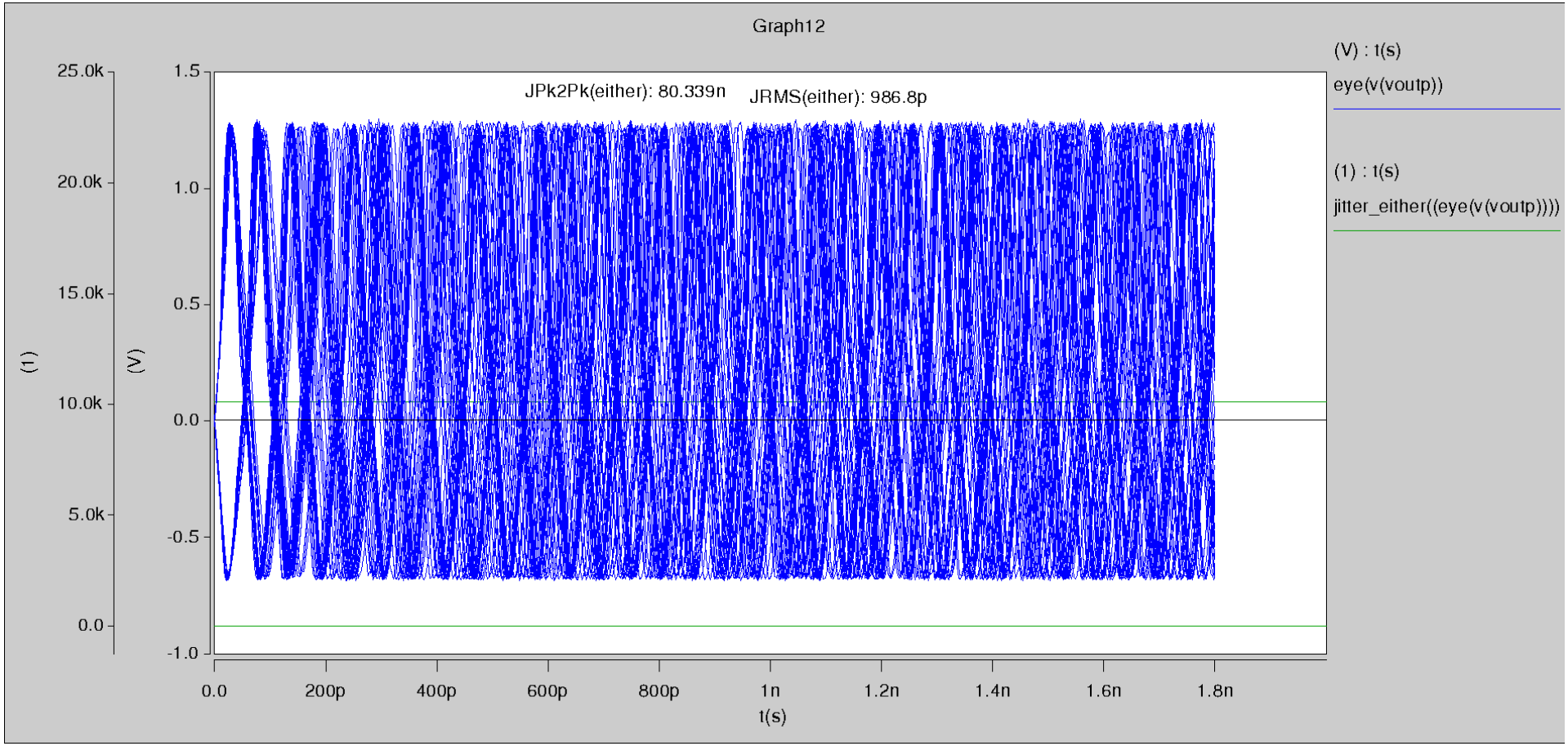
Final VCO Design Parameters

M1	L = 100n, W = 2u
M2	L = 100n, W = 2u
M3	L = 100n , W = 2u
M4	L = 100n, W = 2u
M5	L = 500n, W = 10u
M6	L = 500n, W = 10u
M7	L = 500n, W = 10u
M8	L = 500n, W = 10u
M9	L = 100n, W = 2u
M10	L = 50n, W = 2u
L	1.5nH, Q = 5
R	465 Ω

Fractional N-Divider Simulation



VCO Jitter Analysis



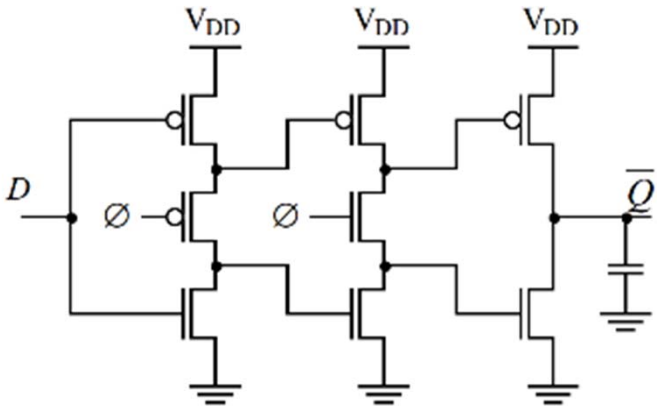
Theoretical Design Overview

- $Q = Q_L = \frac{\omega_0 L}{R} = 5$
- $\omega_0 = \frac{1}{\sqrt{LC}}\sqrt{1 - \frac{R^2 C_{var}}{L}}$
- $Choose\ g_m \geq \frac{RC_{var}}{L}\ for\ each\ transistor.$
  - Recall, $g_m = \sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right) I_{bias}}$
- $R_{PU} = -\frac{2}{g_{m1,2}}\ and\ R_{PD} = -\frac{2}{g_{m3,4}}$

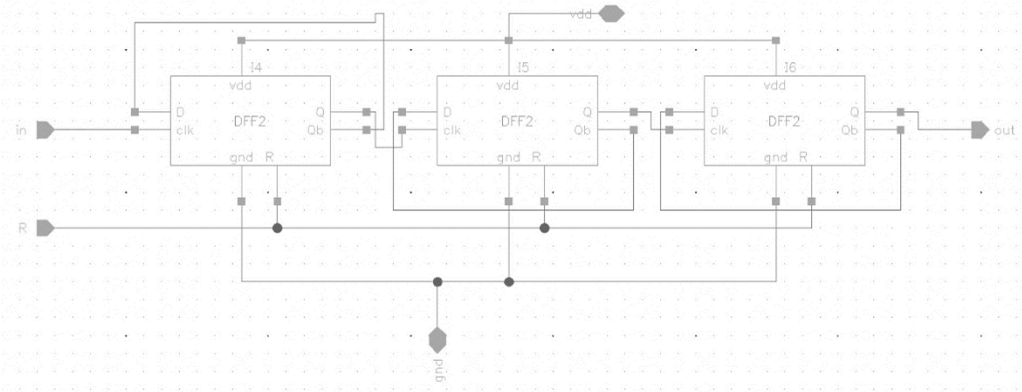
Fractional N-Divider Circuit

1. Needed to slow down the VCO's output so that PFD can compare it with reference frequency.

2. N D-FlipFlops cascaded together to achieve 2^N divider.

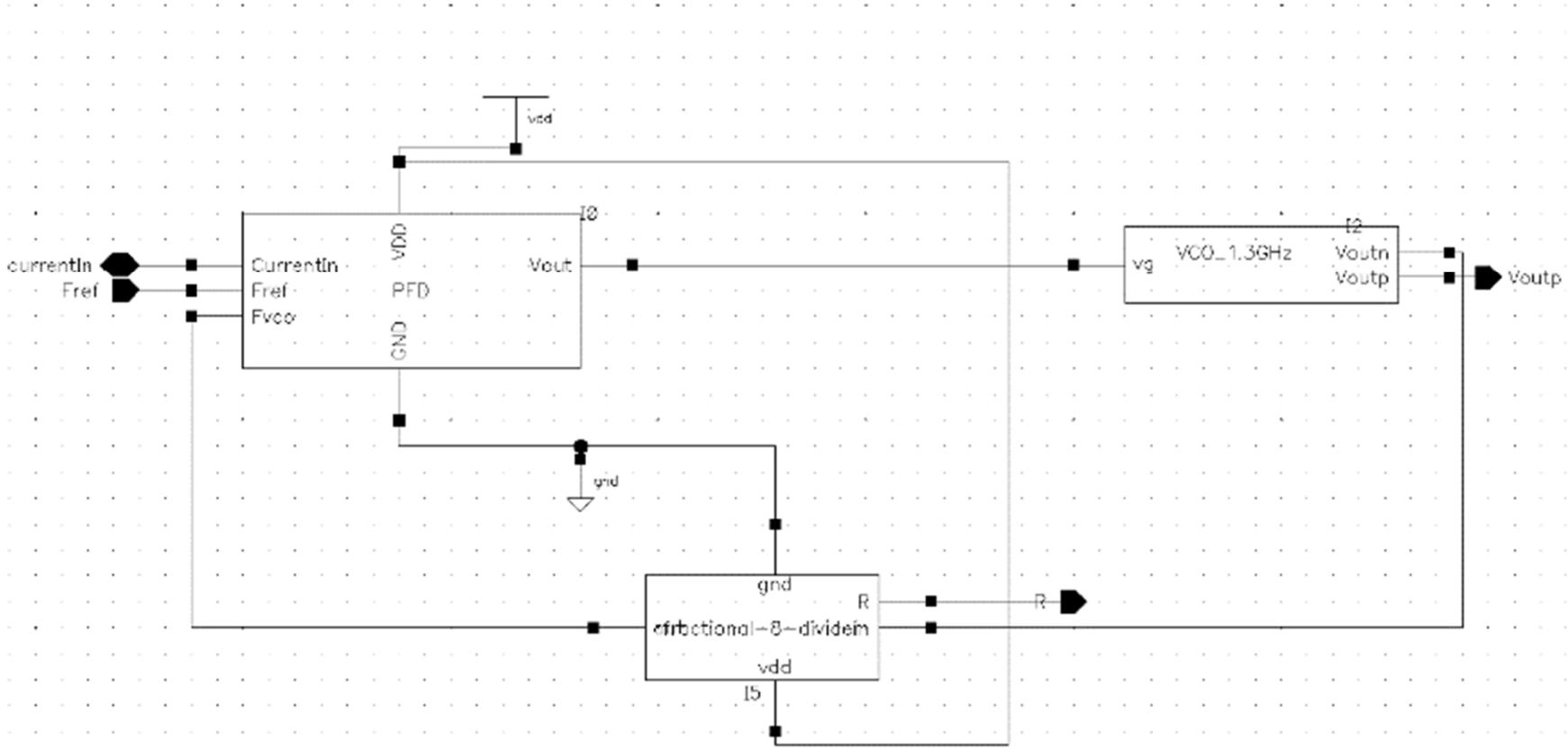


Positive edge-triggered DFF using split-output latches

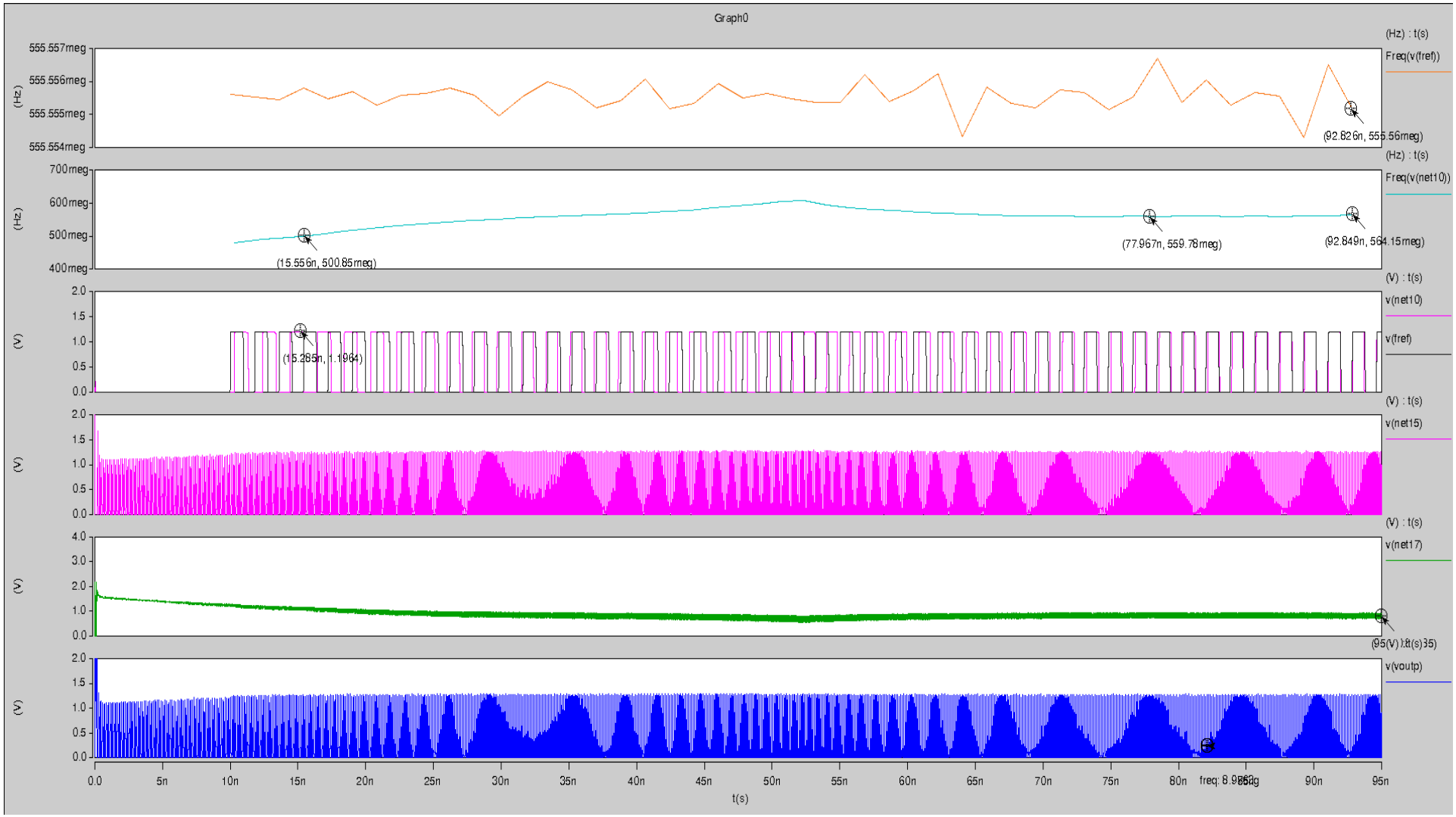


Fractional 8 Divider

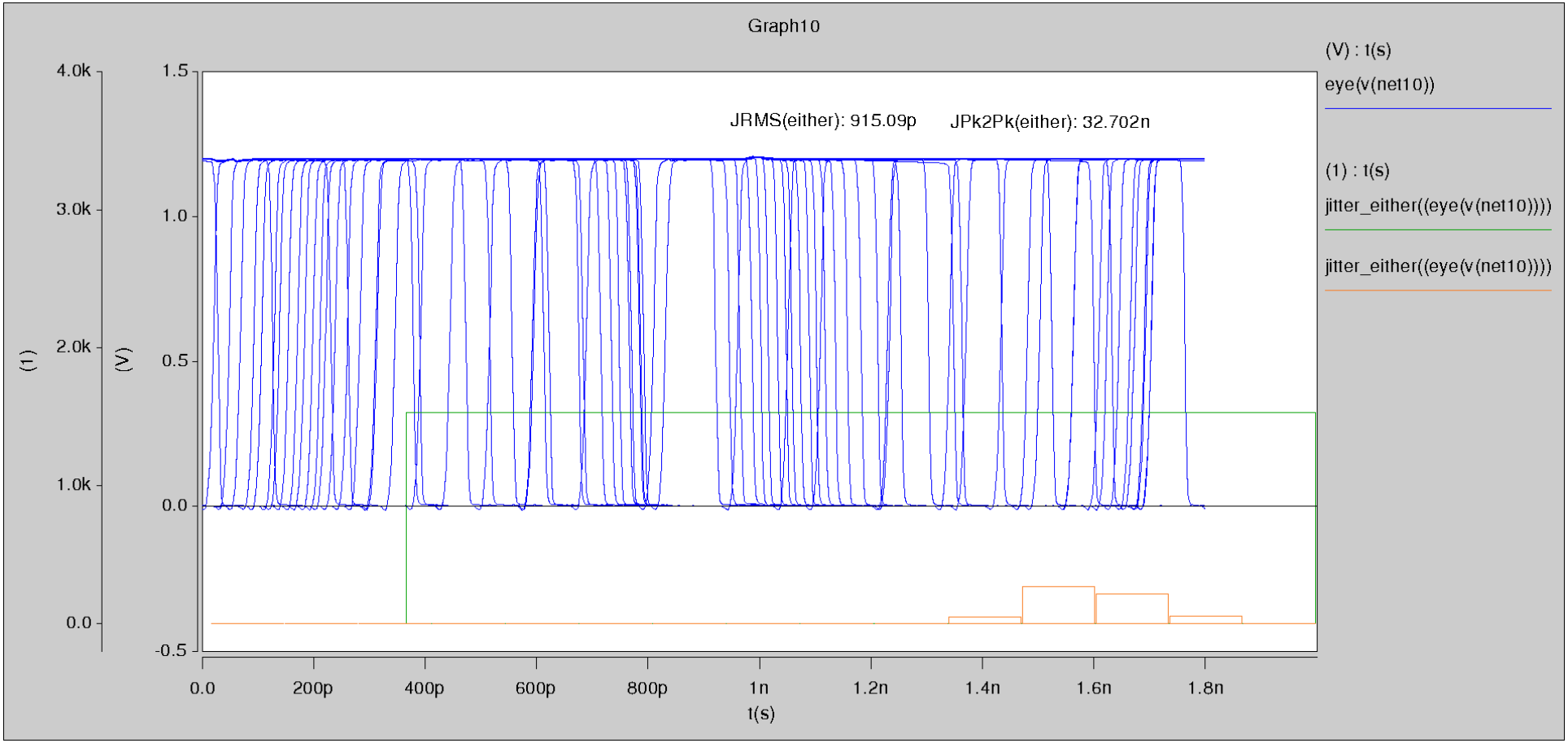
Complete PLL Circuit



Complete PLL Simulation



Complete PLL Jitter Analysis

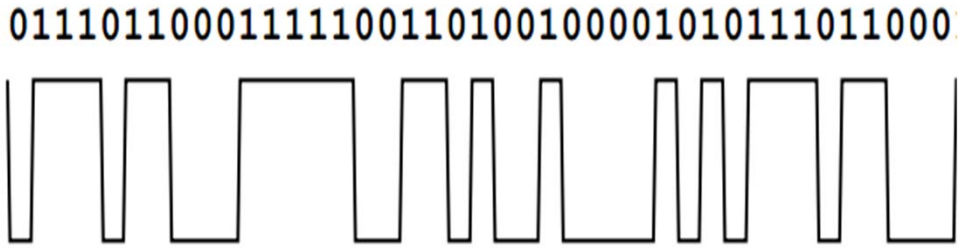


CDR Circuit Overview

- Monitor data signal transitions and select optimal sampling phase for the data at midpoint between edges.
- Extracts clock information from incoming data stream and uses this regenerated clock to resample the data waveform and recover the data.
- Non-linear circuit and key block to limit jitter, noise within the SERDES circuit.

Basic Idea

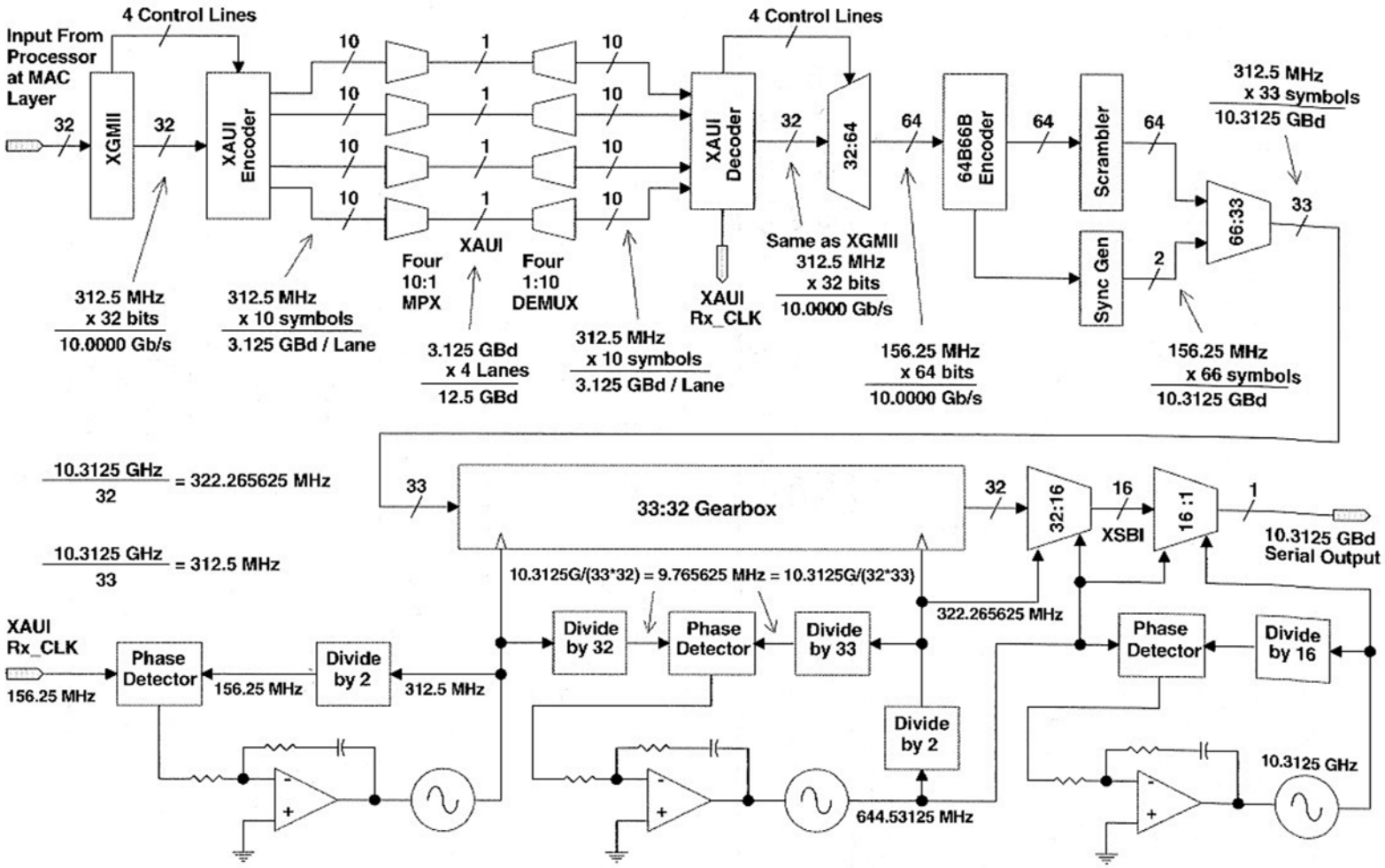
- Serial data transmission sends binary bits of information as a series of optical or electrical pulses



- The transmission channel (coax, radio, fiber) generally distorts the signal in various ways

- From this signal we must recover both clock and data

10 Gigabit Ethernet Serializer



10 Gigabit Ethernet Deserializer