ECE 546
Introduction

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Future System Needs and Functions

Auto
Digital Wireless

MEMS
Analog, RF Computer

Consumer

High bandwidth
High-speed Digital

Log (Capacity Gb/s)


Limits of Optical
# Inter-IC Communication Trends

<table>
<thead>
<tr>
<th>Decade</th>
<th>Speeds</th>
<th>Transceiver Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>1980’s</td>
<td>&gt;10Mb/s</td>
<td>Inverter out, inverter in</td>
</tr>
<tr>
<td>1990’s</td>
<td>&gt;100Mb/s</td>
<td>Termination</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Source-synchronous clk.</td>
</tr>
<tr>
<td>2000’s</td>
<td>&gt;1 Gb/s</td>
<td>Pt-to-pt serial streams</td>
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<tr>
<td></td>
<td></td>
<td>Pre-emphasis equalization</td>
</tr>
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<td></td>
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<tr>
<td>Future</td>
<td>&gt;10 Gb/s</td>
<td>Adaptive Equalization,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Advanced low power clk.</td>
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<tr>
<td></td>
<td></td>
<td>Alternate channel materials</td>
</tr>
</tbody>
</table>

Slide Courtesy of Frank O’Mahony & Brian Casper, Intel
High-Speed Bus and Networks

- **Memory Bus (Single-ended, Parallel)**
  - DDR (4.266 Gbps)
  - LPDDR4 (4.266 Gbps)
  - GDDR (7 Gbps)
  - XDR (differential, 4.8 Gbps)
  - Wide IO2, HBM

- **Front Side Bus (Differential, Parallel)**
  - QuickPath Interconnect (6.4 Gbps)
  - HyperTransport (6.4 Gbps)

- **Computer IO (Differential, Parallel)**
  - PCIe (8 Gbps)
  - InfiniBand (10 Gbps)

- **Cable (Differential, Serial)**
  - USB (4.266 Gbps)
  - HDMI (4.266 Gbps)
  - Firewire: Cat 5, Cat 5e, Cat 6

- **Storage (Differential, Serial)**
  - eMMC, UFS (6 Gbps)
  - SAS, STATA (6 Gbps)
  - FiberChannel (10 – 20 Gbps)

- **Ethernet (Differential, Serial)**
  - XAUI (10 Gbps)
  - XFI (10 Gbps)
  - CEI-6GLR
  - SONNET (10 Gbps)
  - 10GBase-x, 100GBase (25 Gbps)

High-Speed Bus and Networks
Signal Integrity

**Ideal**
Transmission Channel

**Common**
Transmission Channel

**Noisy**
Transmission Channel
Signal Integrity

• Serial data transmission sends binary bits of information as a series of optical or electrical pulses

```
0111011000111110011010010001010111011000
```

• The transmission channel (coax, radio, fiber) generally distorts the signal in various ways

• From this signal we must recover both clock and data
Signal Integrity

Eye-Diagrams

- This is a "1"
- This is a "0"

Eye Opening - space between 1 and 0

With voltage noise
With timing noise

Channel Frequency Response

Channel Responses

ECE 546 – Jose Schutt-Aine
Timing Margin

\[ t_{\text{margin}} = t_{\text{bit}} - t_{\text{os}} - t_{\text{jd}} - t_{\text{jc}} \]

Where,

- \( t_{\text{bit}} \) = bit-width of a symbol
- \( t_{\text{os}} \) = sampling error
- \( t_{\text{jd}}/t_{\text{jc}} \) = data/clock jitter
Timing Jitter

Jitter = time-domain variation in clock signal. Dominated by power-supply noise and substrate noise both of which don’t scale with technology.

<table>
<thead>
<tr>
<th>n</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>Mean</th>
<th>RMS</th>
<th>PP</th>
</tr>
</thead>
<tbody>
<tr>
<td>J_{PER}</td>
<td>-0.06</td>
<td>0.02</td>
<td>-0.06</td>
<td>0.12</td>
<td>0.005</td>
<td>0.085</td>
<td>0.18</td>
</tr>
<tr>
<td>J_C</td>
<td>0.08</td>
<td>-0.08</td>
<td>0.18</td>
<td>-</td>
<td>0.06</td>
<td>0.131</td>
<td>0.26</td>
</tr>
<tr>
<td>J_A</td>
<td>0.07</td>
<td>-0.05</td>
<td>0.31</td>
<td>0.01</td>
<td>0.055</td>
<td>0.05</td>
<td>0.12</td>
</tr>
</tbody>
</table>

J_{PER} = time difference between measured period and ideal period
J_C = time difference between two adjacent clock periods
J_A = time difference between measured clock and ideal trigger clock
Channel
Design Challenges for High-Speed Links

- Modern computer systems require Tb/s aggregate off-chip signaling throughput
  - Interconnect resources are limited
    - Parallel buses with fast edge rates must be used
  - Package size and pin count cannot keep up with speed
  - Stringent power and BER requirements to be met
  - Channel attenuation increases with the data rate
  - High-performance signaling requires high-cost channels
  - Crosstalk-induced jitter

Available number and required speed of I/Os (ITRS roadmap)

A typical controller-memory interface
Signal Integrity Impairments In High-Speed Buses

- SI issues limit system performance to well below channel Shannon capacity
- Inter-Symbol Interference (ISI) is an issue for long backplane buses

- For short, low-cost parallel links, dominant noise source is crosstalk
  - Far-end crosstalk (FEXT) induces timing jitter (CIJ), impacts timing budget

- Other SI impairments:
  - Simultaneous-switching (SSO) noise
  - Thermal noise
  - Jitter from PLL/DLL

![Insertion loss of a single DDR channel](image1)

![FEXT increases with routing density](image2)
Motherboards and Backplanes
Cables and Transmission Lines

- Coaxial cables
  - Plastic jacket
  - Dielectric insulator
  - Metallic shield
  - Centre core

- Twisted pairs
Package-Level Complexity

- Up to 16 layers
- Hundreds of vias
- Thousands of TLs
- High density
- Nonuniformity
## Semiconductor Technology Trends

<table>
<thead>
<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Chip size (mm²)</strong></td>
<td>300</td>
<td>430</td>
<td>520</td>
<td>750</td>
</tr>
<tr>
<td><strong>Number of transistors (million)</strong></td>
<td>11</td>
<td>76</td>
<td>200</td>
<td>1400</td>
</tr>
<tr>
<td><strong>Interconnect width (nm)</strong></td>
<td>200</td>
<td>100</td>
<td>70</td>
<td>35</td>
</tr>
<tr>
<td><strong>Total interconnect length (km)</strong></td>
<td>2.16</td>
<td>2.84</td>
<td>5.14</td>
<td>24</td>
</tr>
</tbody>
</table>
Signal Delay Trend

Signal Delay \[ \Rightarrow \]
\[ \begin{aligned}
gates \text{ delay} \\
interconnect \text{ delay}
\end{aligned} \]

Delay for Metal 1 and Global Wiring versus Feature Size

Source: ITRS roadmap 2004
Interconnects

• Total interconnect length (m/cm²) – active wiring only, excluding global levels will increases:

<table>
<thead>
<tr>
<th>Year</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Length</td>
<td>579</td>
<td>688</td>
<td>907</td>
<td>1002</td>
<td>1117</td>
<td>1401</td>
<td>1559</td>
</tr>
</tbody>
</table>

• Interconnect power dissipation is more than 50% of the total dynamic power consumption in 130nm and will become dominant in future technology nodes

• Interconnect centric design flows have been adopted to reduce the length of the critical signal path
5-Layer Interconnect Technology 0.25μm

<table>
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<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vertical parallel-plate capacitance</td>
<td>0.05 fF/μm²</td>
</tr>
<tr>
<td>Vertical parallel-plate capacitance (min width)</td>
<td>0.03 fF/μm</td>
</tr>
<tr>
<td>Vertical fringing capacitance (each side)</td>
<td>0.01 fF/μm</td>
</tr>
<tr>
<td>Horizontal coupling capacitance (each side)</td>
<td>0.03</td>
</tr>
</tbody>
</table>

Source: M. Bohr and Y. El-Mansy - *IEEE TED Vol. 4, March 1998*
Signal Integrity Impairments

Crosstalk  Dispersion  Attenuation
Reflection  Distortion  Loss
Delta I Noise  Ground Bounce  Radiation

[Diagram showing signal lines and waveforms]

[ oscilloscope waveforms showing voltage levels ]
Measurements

VNA: S-parameter

Spectrum Analyzer

Time-domain simulation

Eye diagram
Tools for Signal Integrity

* Electromagnetic solver
* Circuit level simulator
* Behavioral simulator
* Placement & routing
* Layout designer
* Netlist extractor
* Multiphysics simulator
* Stochastic analyzer
* Design verification
* Electromagnetic analysis
Example: SERDES

Co-Design must address I/O optimization dilemma

- 56Gbps SerDes must scale in terms of power,
- Power must scale with the data rate
- State-of-the-art: 6.4Tbit/second (256 25Gbps serdes)
- 12.8Tbit/s can use PAM-4 modulation to enable 50Gbits/s serdes
- 25.6Tbit/s optical interfaces likely will be required

[J. Hart, ISSCC13, Oracle]
Challenges

Showstoppers

- Multiphysics
- Differences in scales and resolutions
- Different design rules
- Tools are old and slow

Potential Solutions

- Behavioral, Macro Modeling (e.g., IBIS-AMI, X-parameters)
- Statistical modeling
- Hardware, FPGAs
- Artificial intelligence, machine learning
- Quantum computing?
Co-Design

VERTICAL

• Bridge IC, Package, Board
• Bridge System, Architecture, Layout
• Bridge Synthesis, Analysis, Verification
• Bridge Hardware, Software, Firmware

HORIZONTAL

• Energy aware
• Signal/power integrity aware
• Stress/thermal aware
• Security aware
• Testing aware
Power Distribution Network Design Flow

- Start
- Determination of target impedance
- Impedance calculation of PDN
- Selection of chip location
- Determination of inductance and resistance from a chip to all node points
- Determination of the number and locations of decoupling capacitors, locations and parasitic values
- Placement of components and impedance re-calculation
- End

Challenge: Present-day extraction and simulation engines make up a large portion of the computational effort in the PDN flow
Deep Submicron Timing Closure

Unbounded design iterations resulting from unpredicted timing violations

- 0.25 microns and lower
- 2 to 20 iterations
- mismatch between logic and physical designs
- greater timing variations
- dominated by interconnects
- inductive and capacitive coupling
- slows time-to-market
Design Flow

- Design for Test
- Design Verification
- Functionality
  - Behavior Design
  - RTL Design
  - Module Reuse
  - Arch. Analysis
- Timing
  - Behavior Synthesis
  - RTL Synthesis
  - Place and Route
  - Custom Design
  - Floorplanning
- Parasitic Extraction
- Tight integration required

- Chip Test
- Fab
- Layout Verif.
- Customer
Motivations for Co-Design

- Transistors
- Nonlinear
- SPICE
- Scaling with tech

- Interconnects
- Linear
- EM Tools
- Scaling with $\lambda$

- Transmission lines, sensors
- Linear+Nonlinear
- EM Extraction, SPICE, IBIS,…
- Scaling with $\lambda$
Co-Design Requirements

- Tradeoffs in advance
- Translation and domains
- Propagate information
- Manage connectivity
- Database formats

Courtesy of Zuken
Codesign for Chiplets

Gate Level Design

Partitioning

Chip-Package Floor planning and chip-package interconnect co-analysis

Timing Analysis, DC and AC Analysis

Package Design

Chiplet Design

Chiplet Design

Chip-Package Analysis: Pass?

No

Yes

Final Package

Final Chiplets

Final Heterogenous System
Pathfinding Methodologies

- Unified workflow, including partitioning, floor-planning, design of system-level interconnects, route pathway exploration and feasibility analysis. Capability to create abstract package models and virtual die models from multiple sources.

- Ability to visualize and modify component placement scenarios and make connectivity changes in a preliminary floorplan. Provision of dynamic manipulation of pin arrays within the abstract models.

- Preserving signal assignments and rules while making adjustments to the physical pin array. Support for multiple package variables and PCB form factors to verify and compare different system configurations.

- Enabling the interaction of design tools from different EDA vendors.
Traditional Co-Design: Enabling Technologies
Universal Co-Design

- Focus on minimizing energy and delay
- Move away from Von Neumann computing model
- Identify and address conflicting requirements,
- Make use of new physics and emerging technologies
- Future applications are drivers
- End of Moore’s Law necessitates new paradigm

Universal co-design implies collaboration between many disciplines with the common goal of improved performance at lower cost
CO-DESIGN: THE FUTURE OF MICROELECTRONICS

Report of the Office of Science Workshop on Basic Research Needs for Microelectronics October 23 – 25, 2018

Source: US Department of Energy
Co-Design: Holy Grail for HI

“To enable continued advances in computing technologies, a fundamental rethinking is needed of the science behind the materials, synthesis and placement technologies, architectures, and algorithms. ... these advances must be developed collectively, in a spirit of co-design, where each scientific discipline informs and engages the other to achieve orders of magnitude improvements in system-level performance.”