ECE 546
Lecture 10
MOS Transistors

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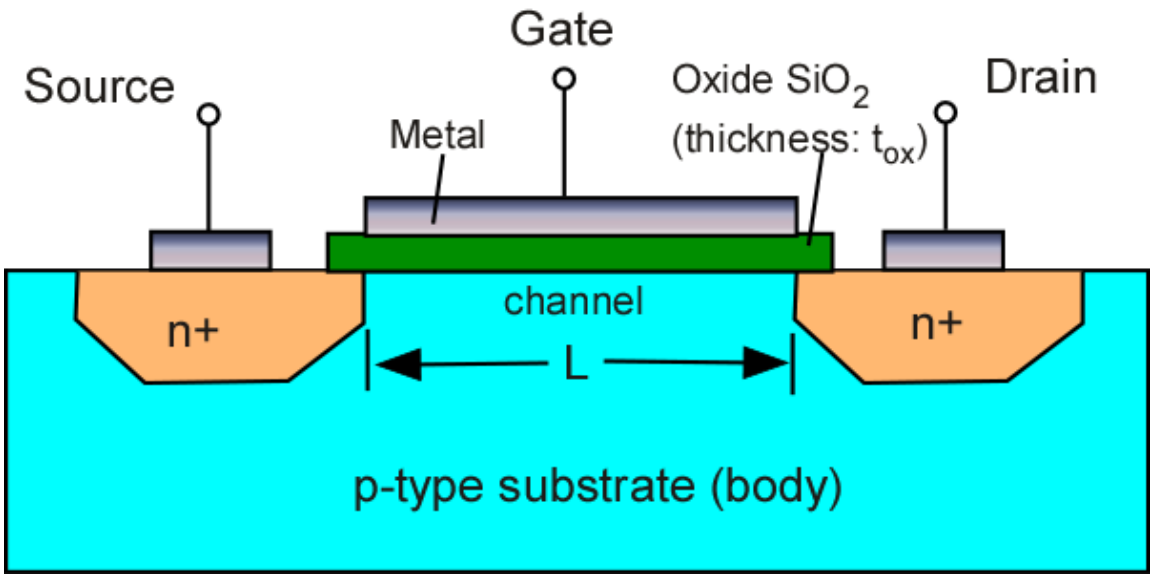
MOS Technologies

Parameter	0.8 µm NMOS	0.8 µm PMOS	0.5 µm NMOS	0.5 µm PMOS	0.25 µm NMOS	0.25 µm PMOS	0.18 µm NMOS	0.18 µm PMOS	0.13 µm NMOS	0.13 µm PMOS	65 nm NMOS	65 nm PMOS	28 nm NMOS	28 nm PMOS
t_{ox} (nm)	15	15	9	9	6	6	4	4	2.7	2.7	1.4	1.4	1.4	1.4
C_{ox}(fF/µm²)	2.3	2.3	3.8	3.8	5.8	5.8	8.6	8.6	12.8	12.8	25	25	34	34
µ(cm²/V.s)	550	250	500	180	460	160	450	100	400	100	216	40	220	200
μC_{ox}(µA/V²)	127	58	190	68	267	93	387	86	511	128	540	100	750	680
V_{to}(V)	0.7	-0.7	0.7	-0.8	0.5	-0.6	0.5	-0.5	0.4	-0.4	0.35	-0.35	0.3	-0.3
V_{DD}(V)	5	5	3.3	3.3	2.5	2.5	1.8	1.8	1.3	1.3	1	1	0.9	0.9
$\lvert V_A \rvert$(V/µm)	25	20	20	10	5	6	5	6	5	6	3	3	1.5	1.5
C_{ov}(fF/µm)	0.2	0.2	0.4	0.4	0.3	0.3	0.37	0.33	0.36	0.33	0.33	0.31	0.4	0.4

22nm BSIM4
32nm BSIM4
45nm BSIM4
65nm BSIM4
90nm BSIM4
130nm BSIM4
90nm BSIM3
130nm BSIM3
180nm BSIM3

NMOS Transistor

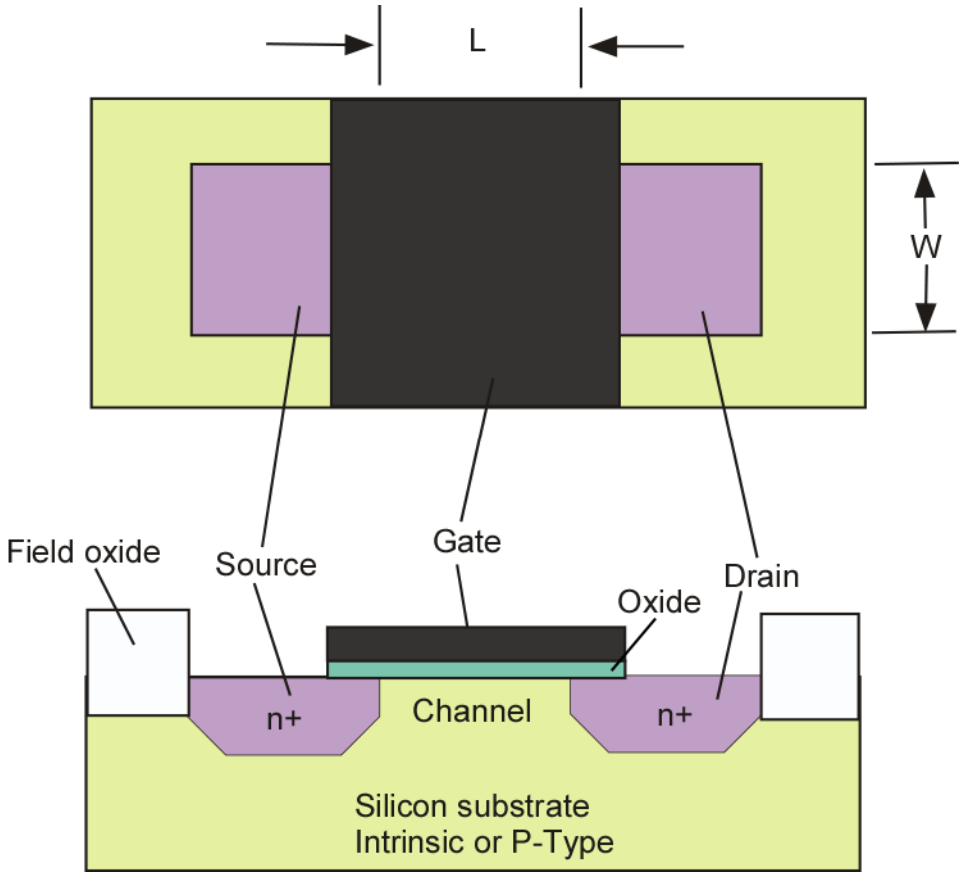


- **NMOS Transistor**
  - N-Channel MOSFET
  - Built on p-type substrate
  - MOS devices are smaller than BJTs
  - MOS devices consume less power than BJTs

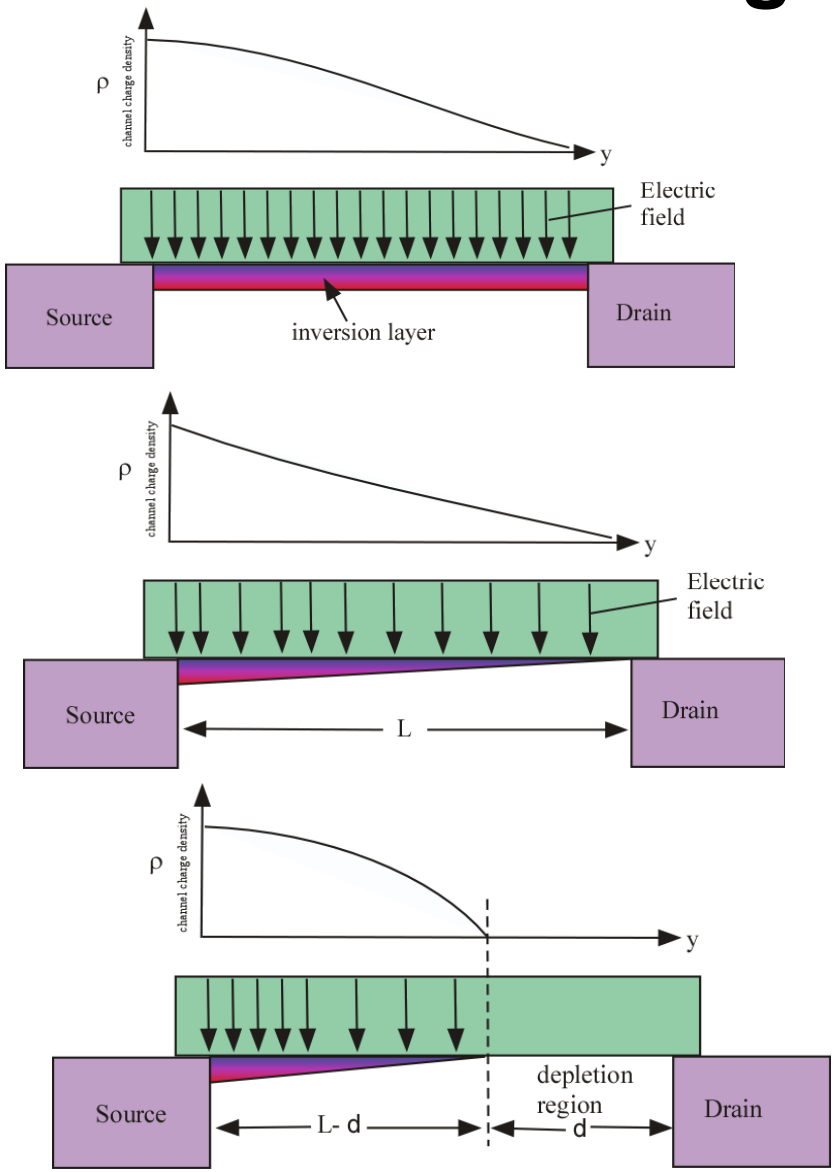
NMOS Transistor - Layout

Top View

Cross Section



MOS Regions of Operation



Triode

Resistive

$$V_{GS} > V_T$$

$$V_{DS} \ small$$

Nonlinear

$$V_{GS} > V_T$$

$$V_{DS} < (V_{GS} - V_T)$$

Active

Saturation

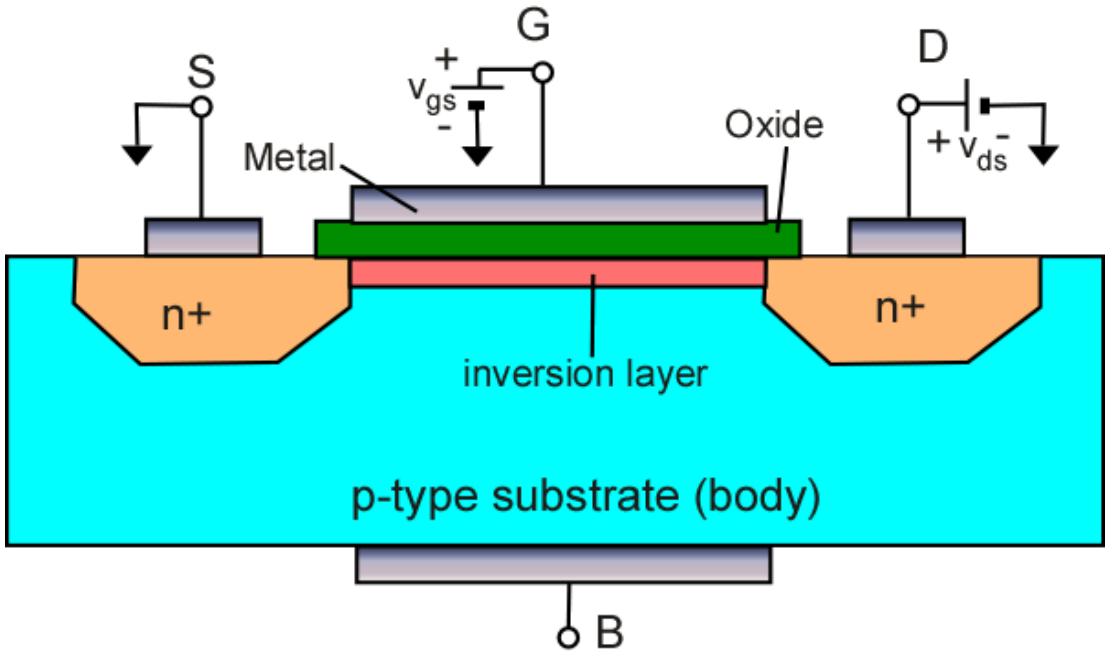
$$V_{GS} > V_T$$

$$V_{DS} \geq V_{GS} - V_T$$

MOS Transistor Operation

- **As V_G increases from zero**
  - Holes in the p substrate are repelled from the gate area leaving negative ions behind
  - A depletion region is created
  - No current flows since no carriers are available
- **As V_G increases**
  - The width of the depletion region and the potential at the oxide-silicon interface also increase
  - When the interface potential reaches a sufficiently positive value, electrons flow in the "*channel*". The transistor is turned on
- **As V_G rises further**
  - The charge in the depletion region remains relatively constant
  - The channel current continues to increase

MOS – Triode Region - 1



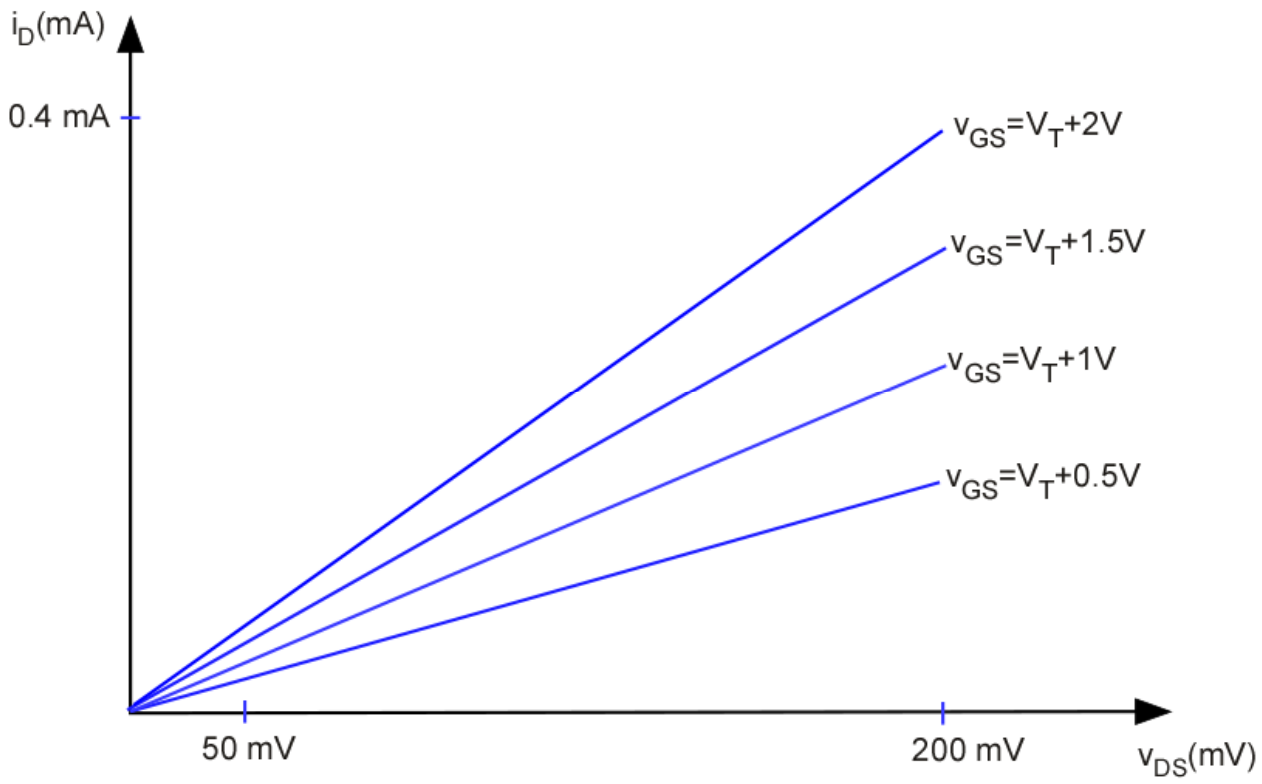
$$I_D = \mu \frac{W}{L} C_{ox} \left[(V_{GS} - V_T) V_{DS} \right]$$

$$V_{DS} << (V_{GS} - V_T)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\varepsilon_o}{t_{ox}}$$

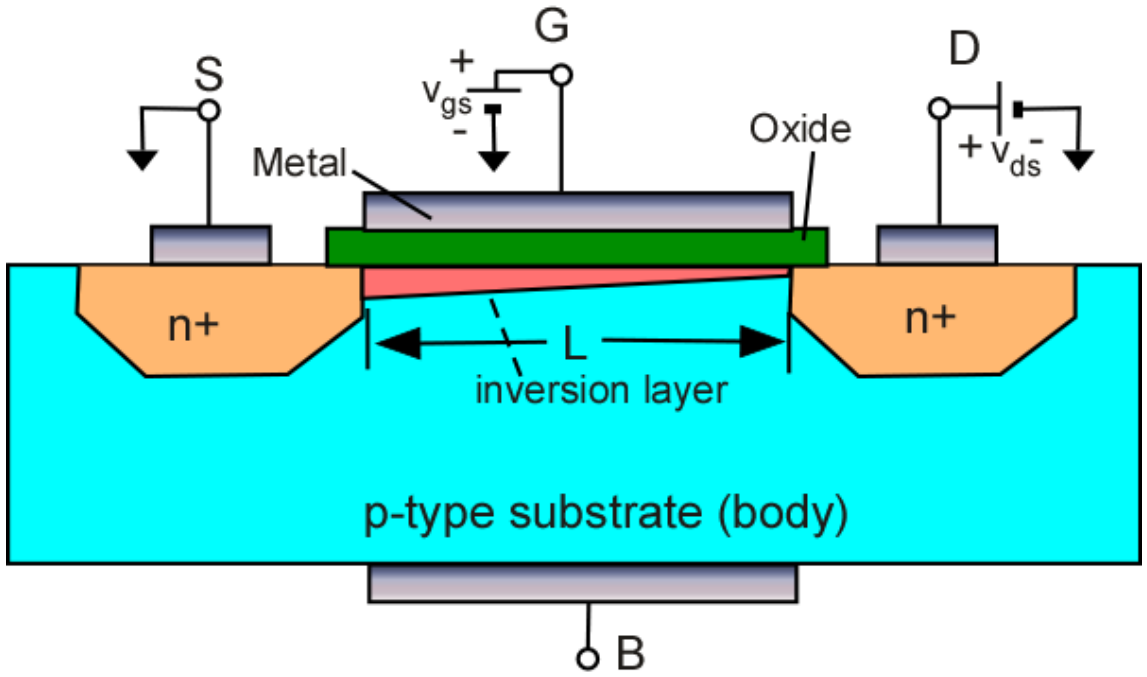
C_{ox}: gate oxide capacitance
μ: electron mobility
L: channel length
W: channel width
V_T: threshold voltage

MOS – Triode Region



FET is like a linear resistor with $r_{ds} = \dfrac{1}{\mu_n C_{ox} \dfrac{W}{L}\left(V_{GS} - V_T\right)}$

MOS – Triode Region - 2



$$V_{GS} > V_T$$

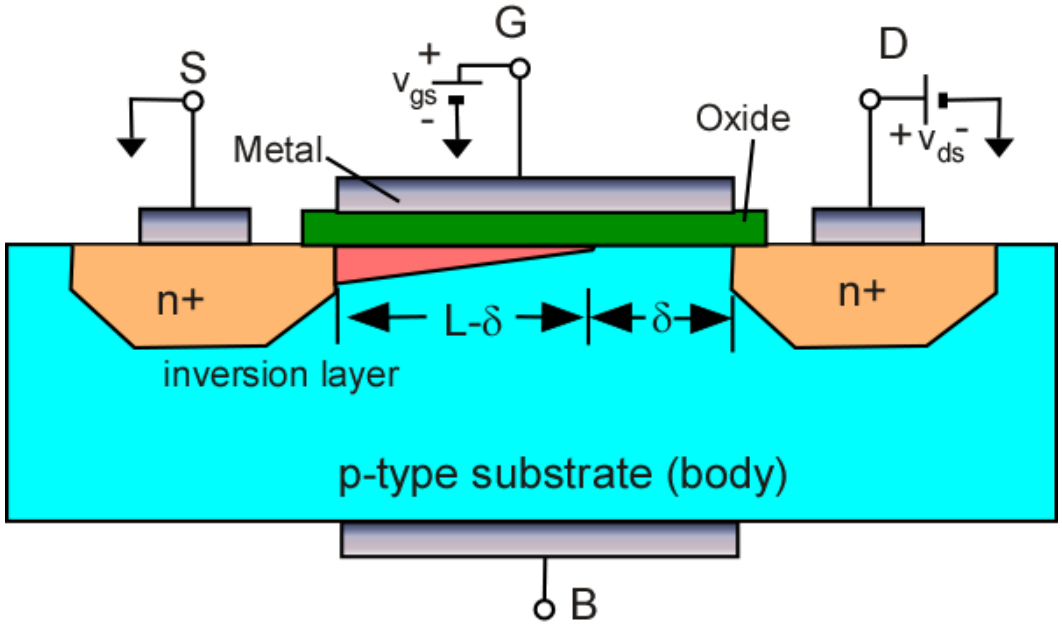
$$V_{DS} < (V_{GS} - V_T)$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

- Charge distribution is nonuniform across channel
- Less charge induced in proximity of drain

MOS – Active Region

Saturation occurs at pinch off when $V_{DS} = (V_{GS} - V_T) = V_{DSP}$



$V_{GS} > V_T$

$V_{DS} > (V_{GS} - V_T)$

(saturation)

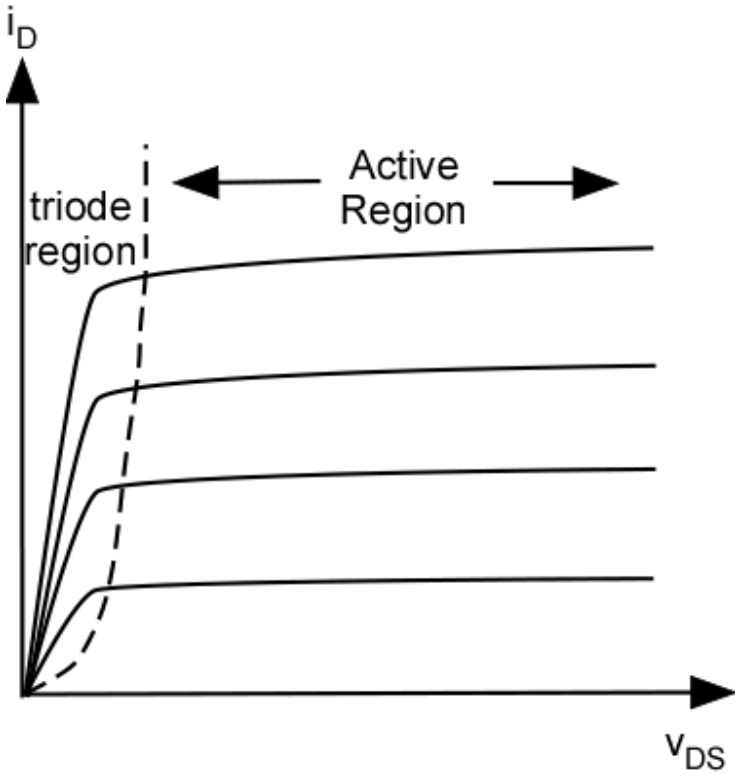
$$I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2$$

MOS Threshold Voltage

The value of V_G for which the channel is *"inverted"* is called the threshold voltage V_T (or V_t).

- **Characteristics of the threshold voltage**
  - Depends on equilibrium potential
  - Controlled by inversion in channel
  - Adjusted by implantation of dopants into the channel
  - Can be positive or negative
  - Influenced by the body effect

MOS – Active Region



- **Saturation**
  - Channel is pinched off
  - Increase in V_{DS} has little effect on i_D
  - Square-law behavior wrt $(V_{GS}-V_T)$
  - Acts like a current source

Body Effect

- **The body effect**
  - V_T varies with bias between source and body
  - Leads to modulation of V_T

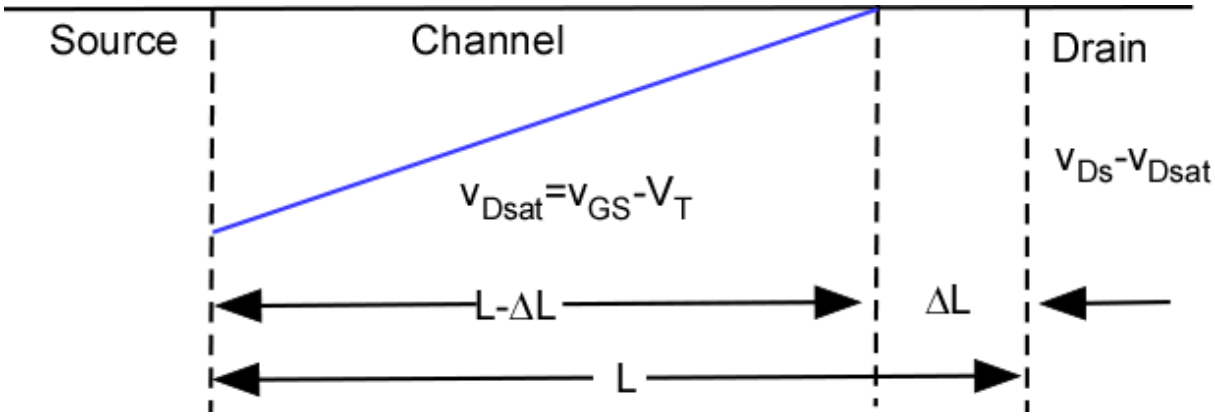
Potential on substrate affects threshold voltage

$$V_T(V_{SB}) = V_{To} + \gamma\left[\left(2|\phi_F| + V_{SB}\right)^{1/2} - \left(2|\phi_F|\right)^{1/2}\right]$$

$$|\phi_F| = \left(\frac{kT}{q}\right)\ln\left(\frac{N_a}{n_i}\right)$$ Fermi potential of material

$$\gamma = \frac{\left(2qN_a\varepsilon_s\right)^{1/2}}{C_{ox}}$$ Body bias coefficient

Channel-Length Modulation



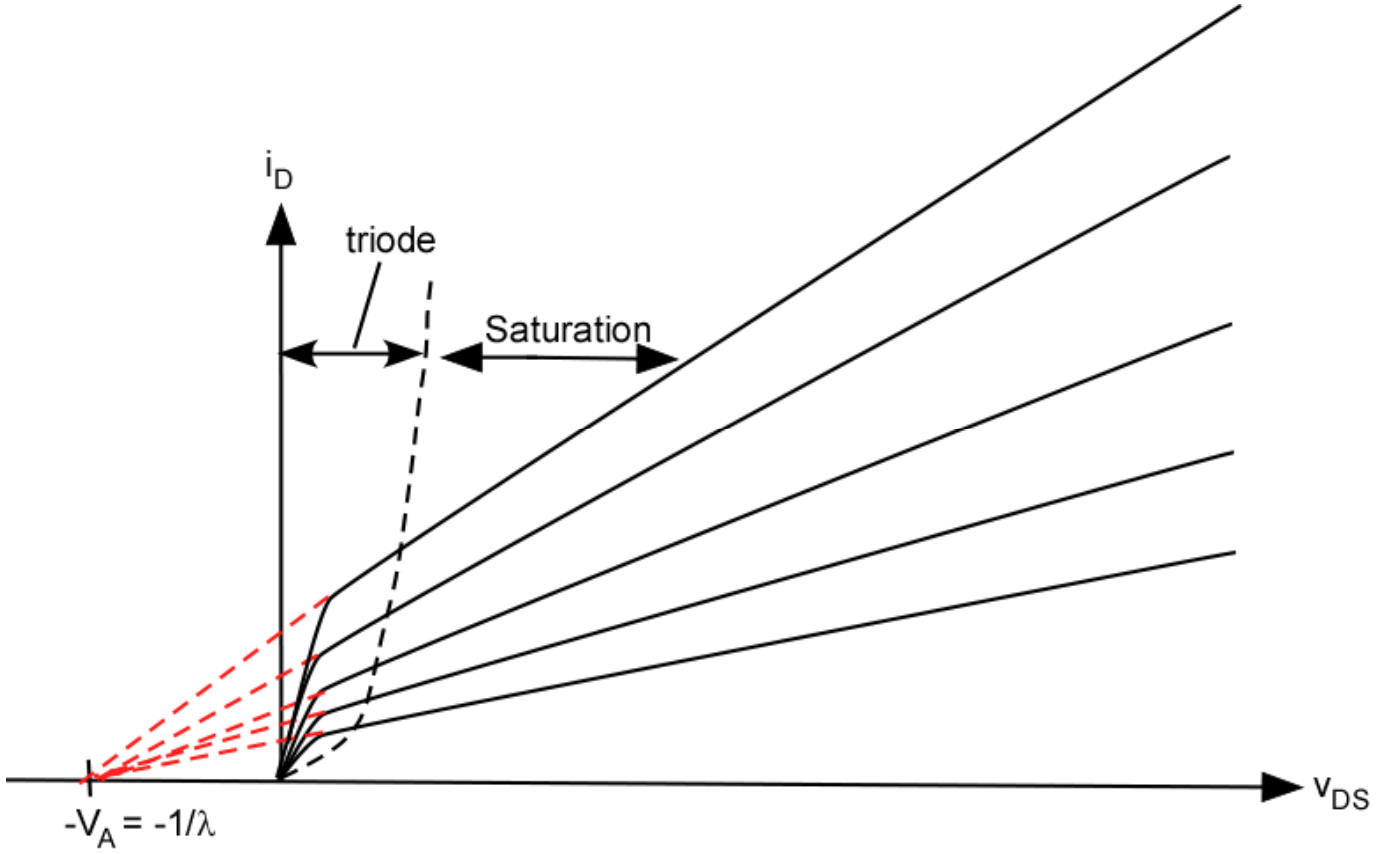
With depletion layer widening, the channel length is in effect reduced from *L* to *L*-ΔL ➔ Channel-length modulation

This leads to the following I-V relationship

$$i_D = \frac{1}{2} k_n' \frac{W}{L} \left(v_{GS} - V_T \right)^2 \left(1 + \lambda v_{DS} \right)$$

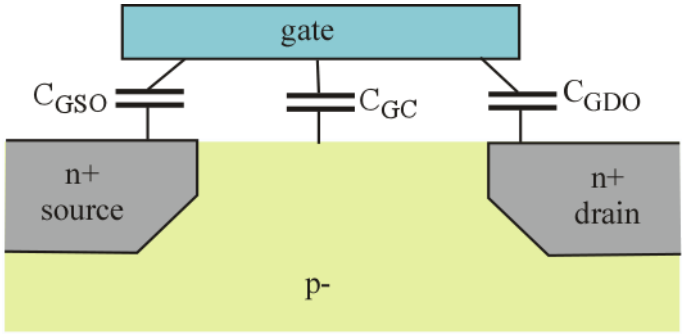
Where λ is a process technology parameter

Channel-Length Modulation

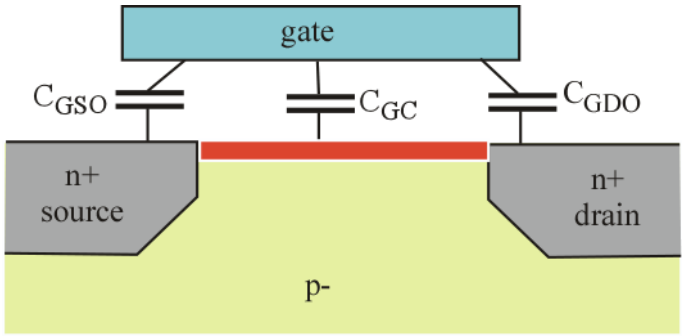


Channel-length modulation causes i_D to increase with v_{DS} in saturation region

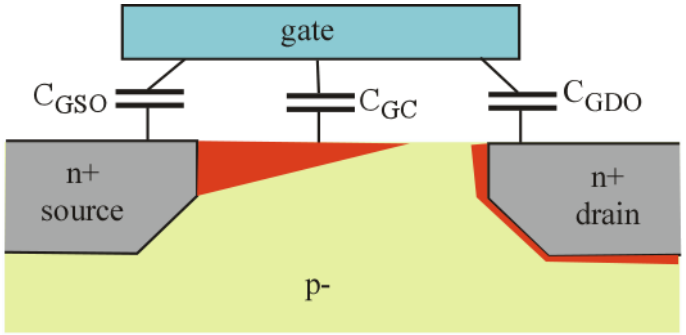
Gate Capacitance



$V_{GT} < 0$



$V_{GT} > 0,\ V_{DS}$ small



$V_{GT} > 0,\ V_{DS}$ large

- **Capacitance**
  - Depends on bias
  - Fringing fields are present
  - Account for overlap C

Capacitance

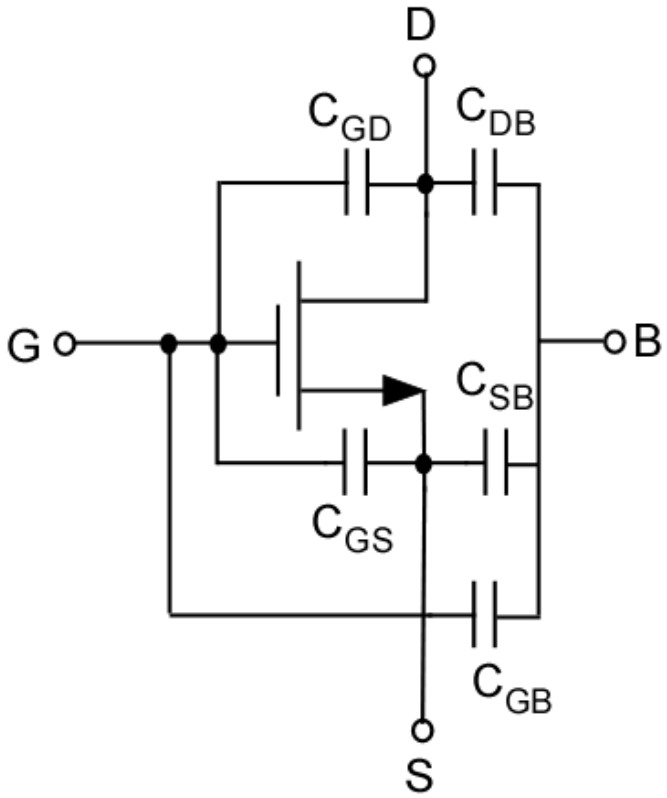
- **Gate Capacitance**
  - C_G determines the amount of charge to switch gate
  - Several distributed components
  - Large discontinuity as device turns on
  - At saturation capacitance is entirely between gate and source

$$C_{gs} = C_{gso} + \frac{2}{3} WLC_{ox} \left[1 - \left(\frac{1 - X}{2 - X} \right)^2 \right]$$

Define $$X = \frac{V_{DS}}{V_{GS} - V_T}$$

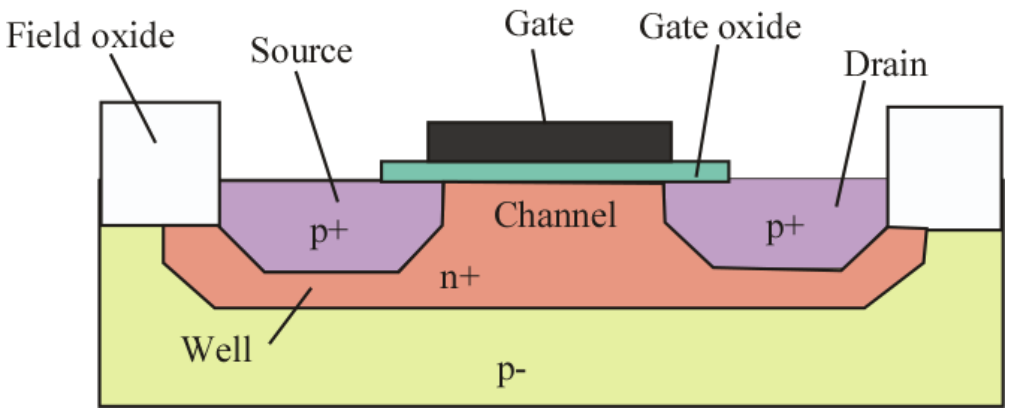
$$C_{gd} = C_{gdo} + \frac{2}{3} WLC_{ox} \left[1 - \left(\frac{1}{2 - X} \right)^2 \right]$$

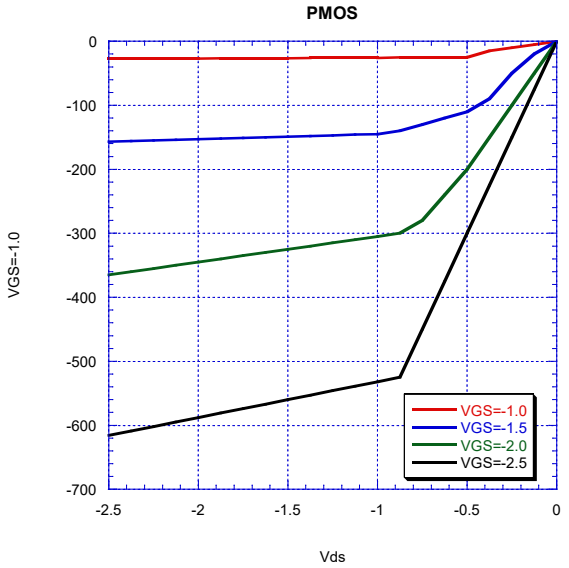
MOS Capacitances



- **Expect capacitance between every two of the four terminals.**

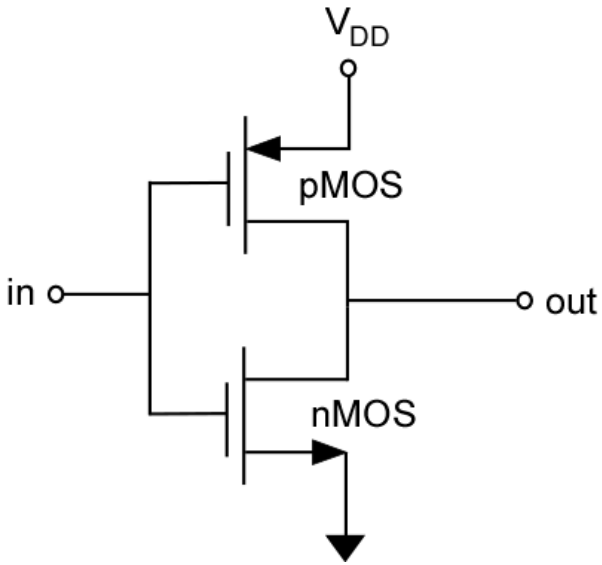
PMOS Transistor

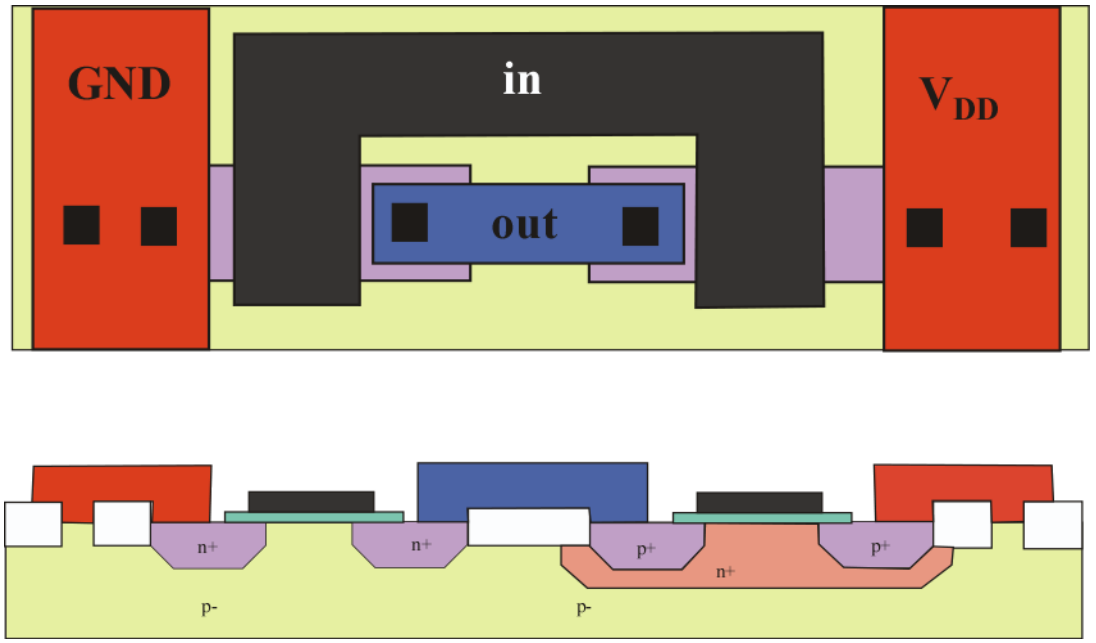




- All polarities are reversed from nMOS
- v_{GS}, v_{DS} and V_t are negative
- Current i_D enters source and leaves through drain
- Hole mobility is lower $\Rightarrow$ low transconductance
- nMOS favored over pMOS

Complementary MOS





- **CMOS Characteristics**
  - Combine nMOS and pMOS transistors
  - pMOS size is larger for electrical symmetry

CMOS

- **Advantages**
  - Virtually, no DC power consumed
  - No DC path between power and ground
  - Excellent noise margins (V_{OL}=0, V_{OH}=V_{DD})
  - Inverter has sharp transfer curve

- **Drawbacks**
  - Requires more transistors
  - Process is more complicated
  - pMOS size larger to achieve electrical symmetry
  - Latch up

Voltage Transfer Characteristics (VTC)

The static operation of a logic circuit is determined by its VTC

- **In low state: noise margin is *NM_L***

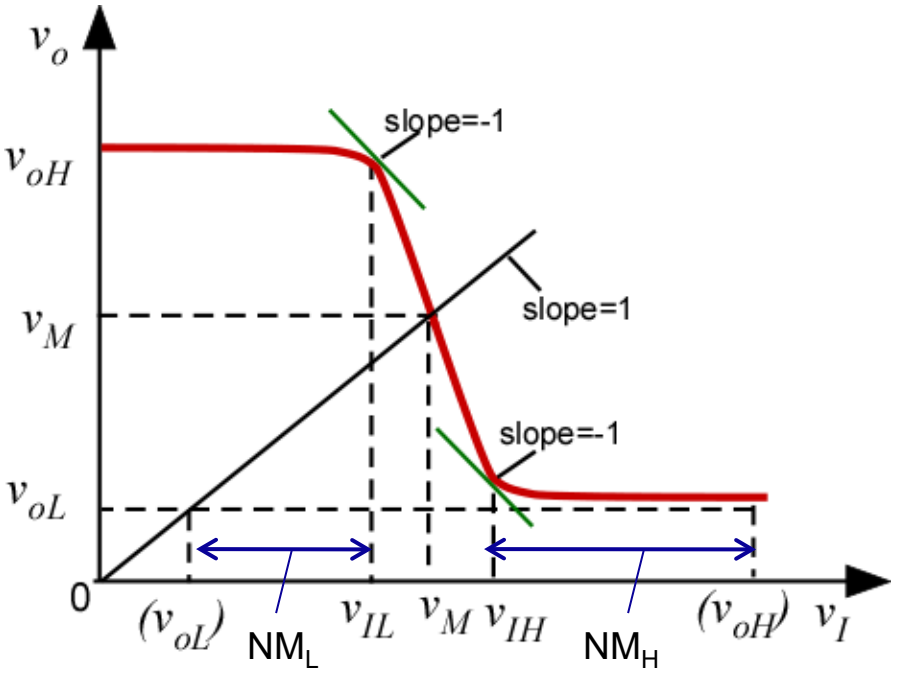
$$NM_L = V_{IL} - V_{OL}$$

- **In high state: noise margin is *NM_H***

$$NM_H = V_{OH} - V_{IH}$$

- **An ideal VTC will maximize noise margins**

Optimum: $NM_L = NM_H = V_{DD}/2$

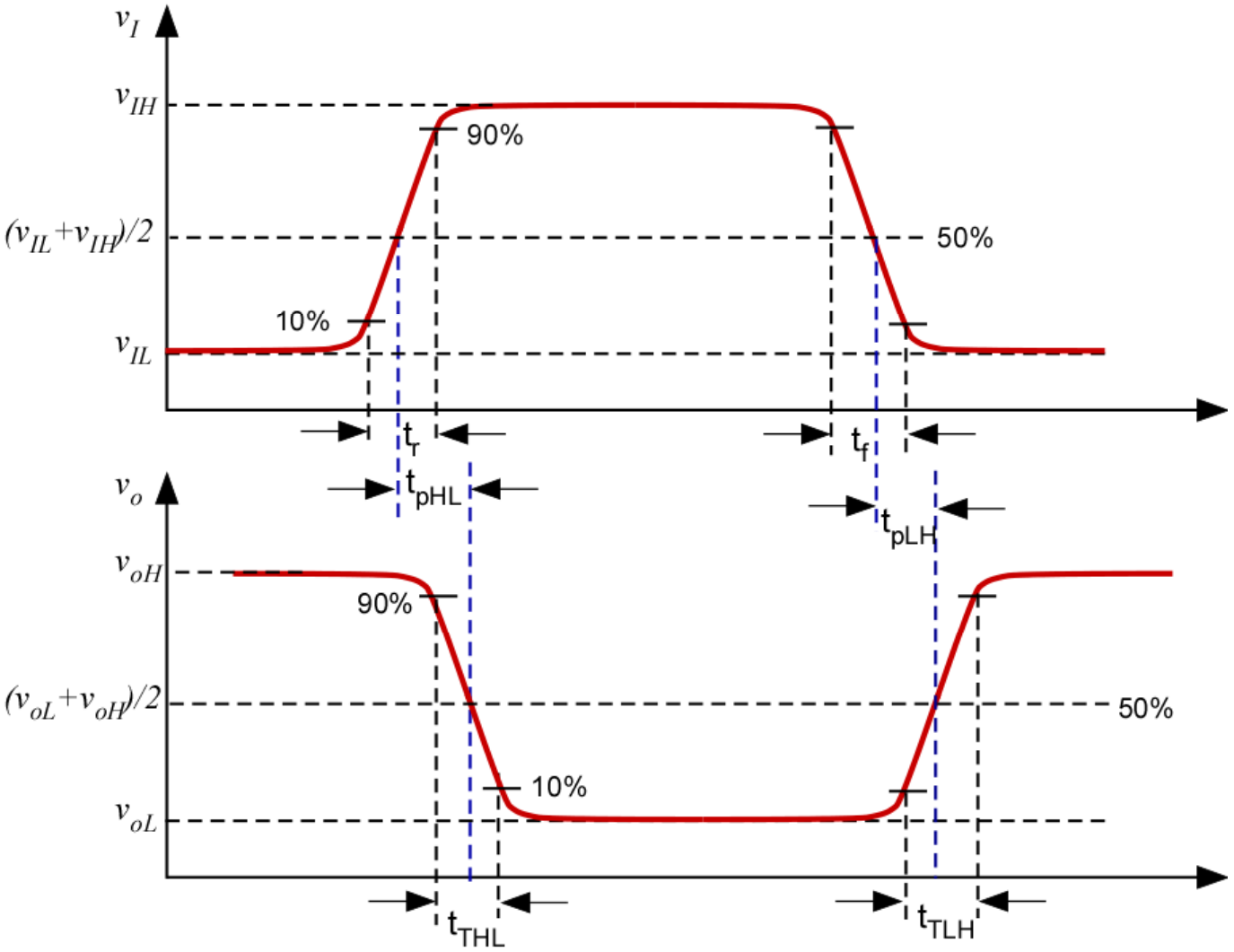


V_{IL} and V_{IH} are the points where the slope of the VTC=-1

Switching Time & Propagation Delay

input

output



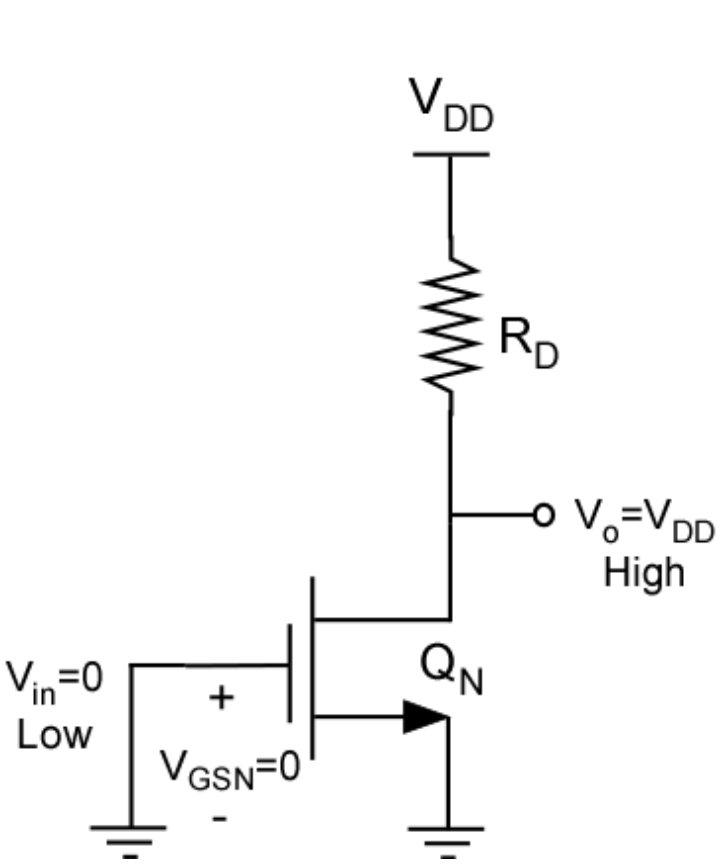
Switching Time & Propagation Delay

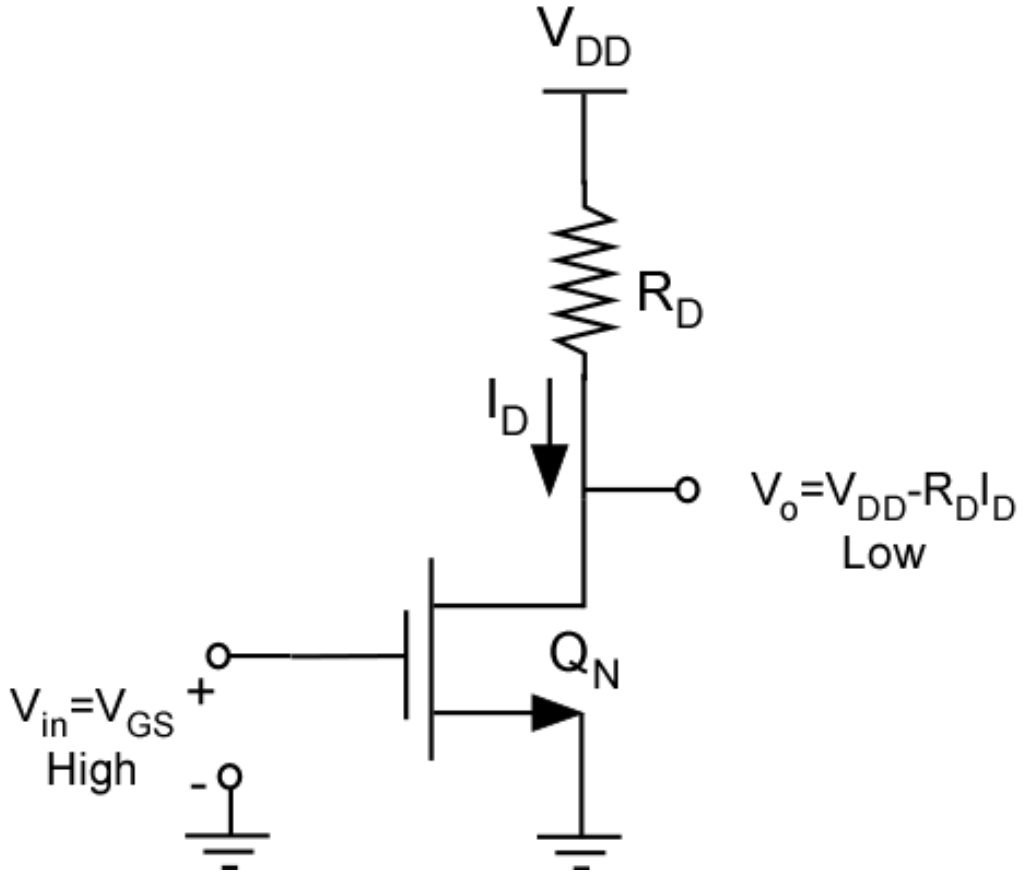
t_r=rise time (from 10% to 90%)
t_f=fall time (from 90% to 10%)
t_{pLH}=low-to-high propagation delay
t_{pHL}=high-to-low propagation delay

Inverter propagation delay:

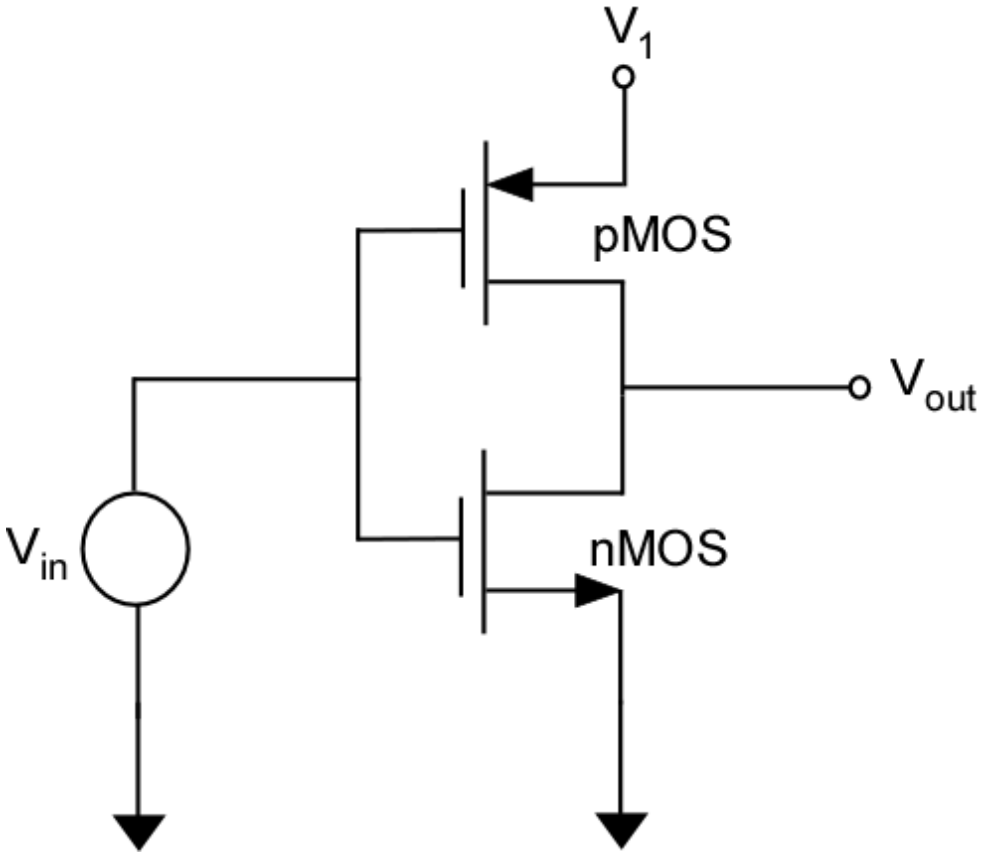
$$t_p = \frac{1}{2}\left(t_{pLH} + t_{pHL}\right)$$

NMOS Switch


V_{DD}
R_D
$V_o=V_{DD}$
High
$V_{in}=0$
Low
+
$V_{GSN}=0$
-
Q_N


V_{DD}
R_D
I_D
$V_o=V_{DD}-R_DI_D$
Low
$V_{in}=V_{GS}$
High
+
-
Q_N

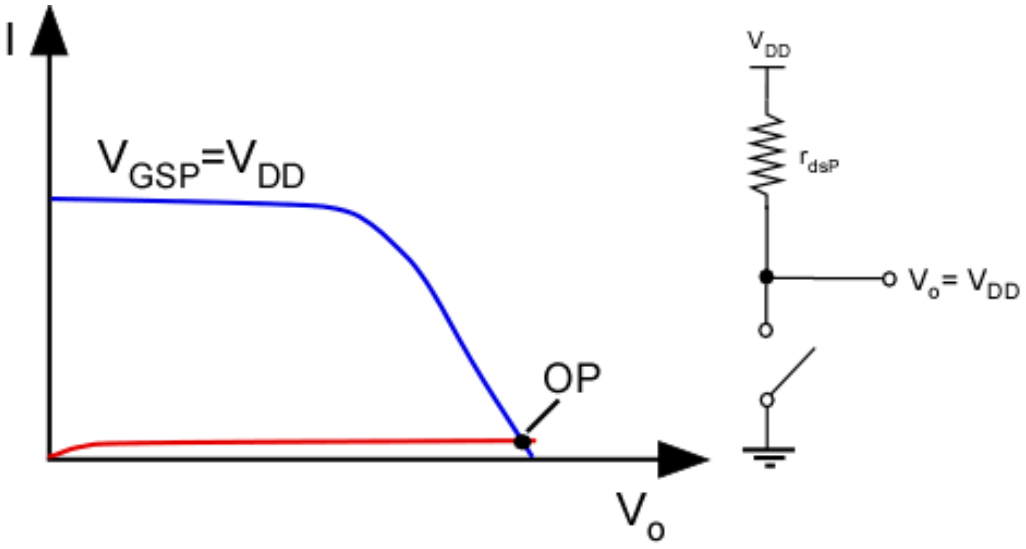
CMOS Switch



CMOS switch is called an inverter

The body of each device is connected to its source ➔ NO BODY EFFECT

CMOS Switch – Input Low



NMOS

$$V_{GSN} < V_{TN} \Rightarrow OFF$$

r_{dsn} high

PMOS

$$r_{dsp} = \frac{1}{k_p' \left(\frac{W}{L}\right)_p \left(V_{DD} - |V_{TP}|\right)}$$

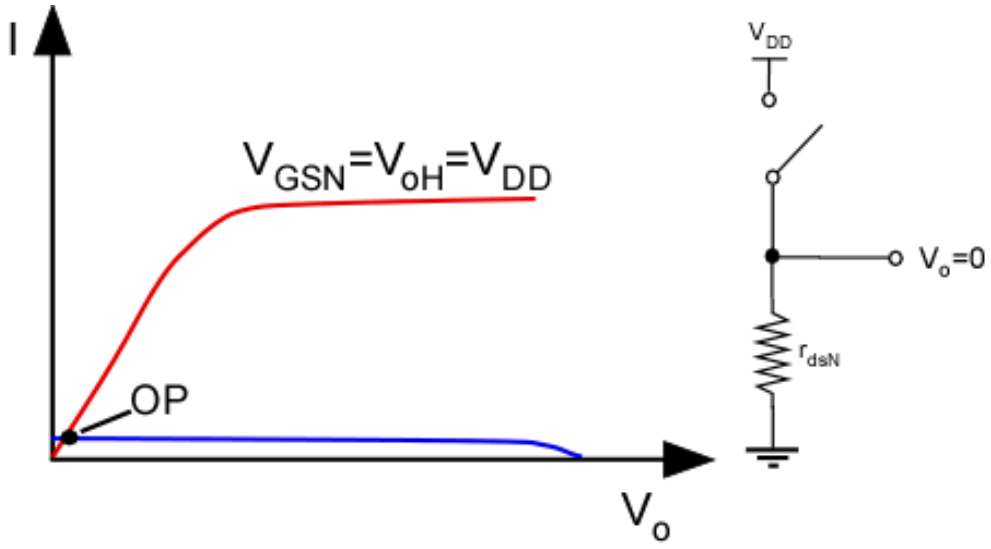
r_{dsp} is low

CMOS Switch – Input High

NMOS

$$r_{dsn} = \frac{1}{k_n'\left(\frac{W}{L}\right)_n\left(V_{DD} - V_{TN}\right)}$$

r_{dsn} is low

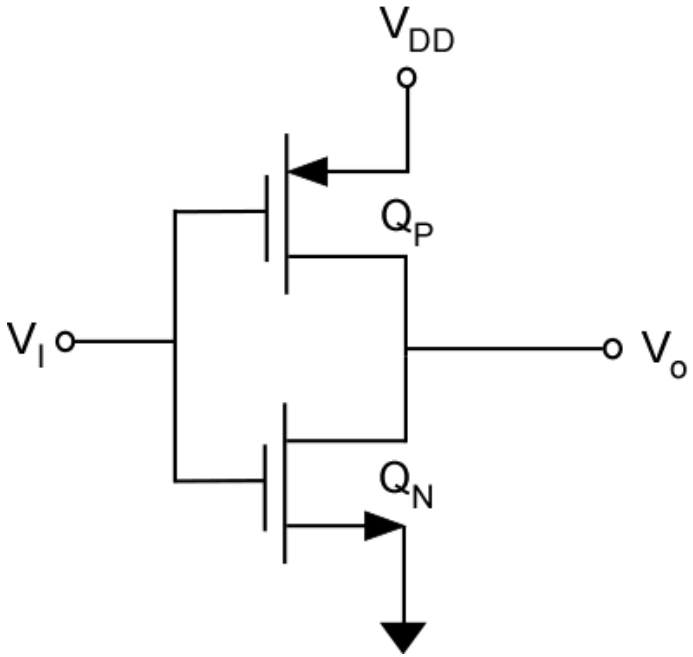


PMOS

$$V_{GSP} > V_{TP} \Rightarrow OFF$$

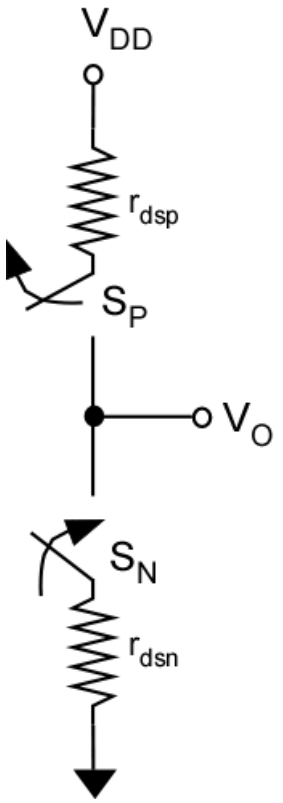
r_{dsp} high

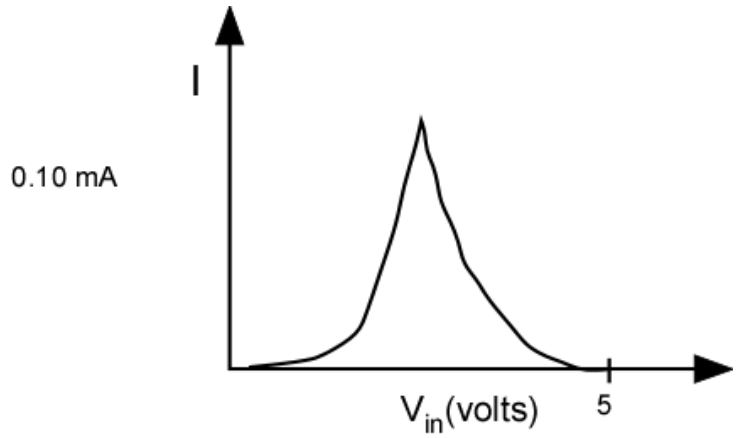
CMOS Inverter



$$r_{dsn} = \frac{1}{k_N' \left(\frac{W}{L}\right)_n \left(V_{DD} - V_T\right)}$$

$$r_{dsp} = \frac{1}{k_P' \left(\frac{W}{L}\right)_p \left(V_{DD} - V_T\right)}$$





Short switching transient current ➔ low power

CMOS Inverter

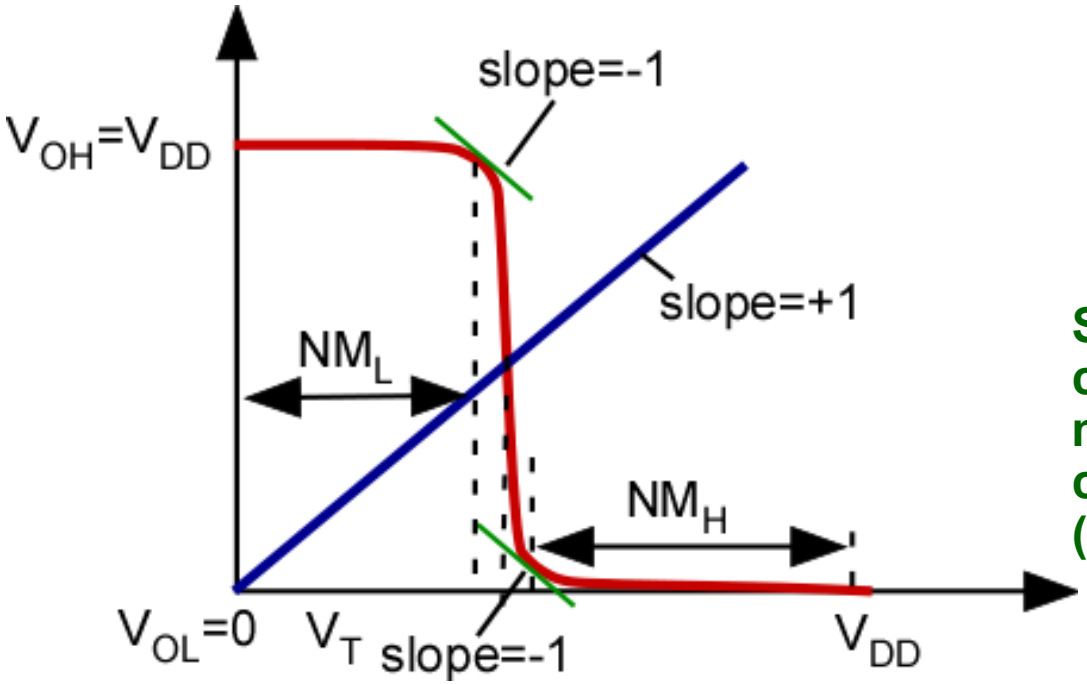
Advantages of CMOS inverter

- Output voltage levels are 0 and V_{DD}➔signal swing is maximum possible
- Static power dissipation is zero
- Low resistance paths to V_{DD} and ground when needed
- High output driving capability➔ increased speed
- Input resistance is infinite➔ high fan-out

Load driving capability of CMOS is high. Transistors can sink or source large load currents that can be used to charge and discharge load capacitances.

Matched CMOS Inverter VTC

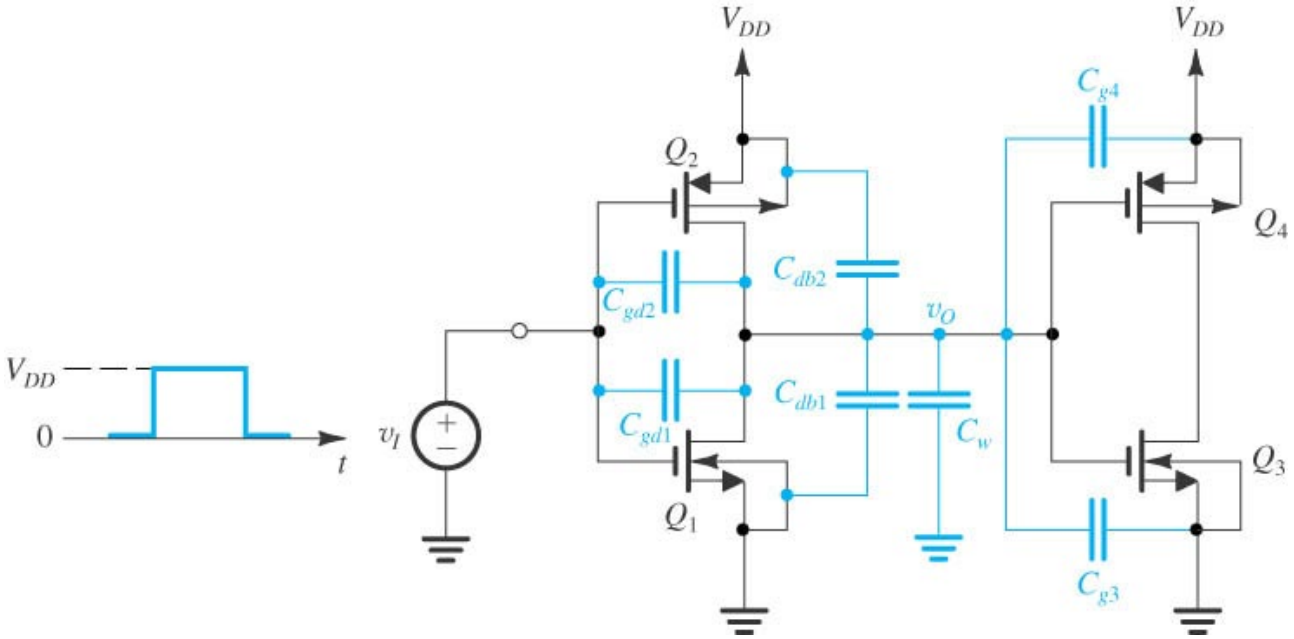
CMOS inverter can be made to switch at specific threshold voltage by appropriately sizing the transistors



$$\left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_n$$

Symmetrical transfer characteristics is obtained via matching ➔ equal current driving capabilities in both directions (pull-up and pull-down)

CMOS Dynamic Operation



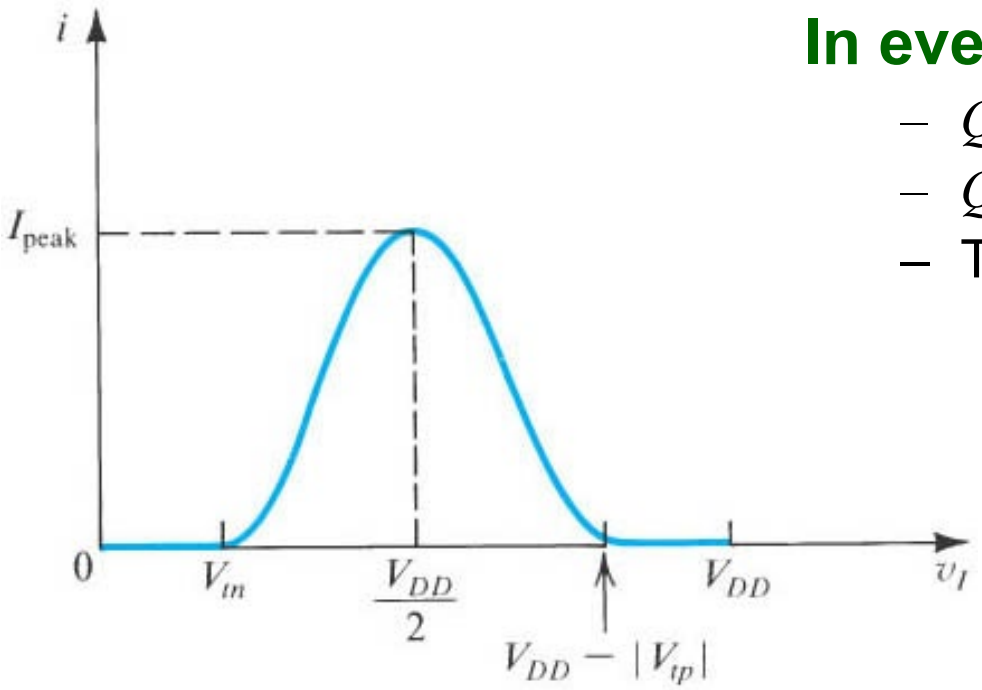
- Exact analysis is too tedious
- Replace all the capacitances in the circuit by a single equivalent capacitance C connected between the output node of the inverter and ground
- Analyze capacitively loaded inverter to determine propagation delay

CMOS Dynamic Operation

$$t_P = \frac{1}{2}\left(t_{PHL} + t_{PLH}\right)$$

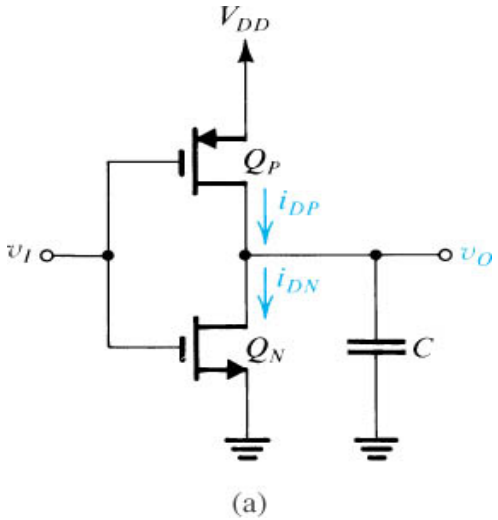
- Components can be equalized by matching transistors
- t_P is proportional to C ➔ reduce capacitance
- Larger V_{DD} means lower t_p
- Conflicting requirements exist

CMOS – Dynamic Power Dissipation



In every cycle

- Q_N dissipate ½ CV_{DD}^2 of energy
- Q_P dissipate ½ CV_{DD}^2 of energy
- Total energy dissipation is CV_{DD}^2



(a)

If inverter is switched at f cycles per second, dynamic power dissipation is: $P_D = fCV_{DD}^2$

Digital Logic - Generalization

De Morgan's Law

$$\overline{A + B + C + \ldots} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \ldots$$

$$\overline{A \cdot B \cdot C \cdot \ldots} = \overline{A} + \overline{B} + \overline{C} + \ldots$$

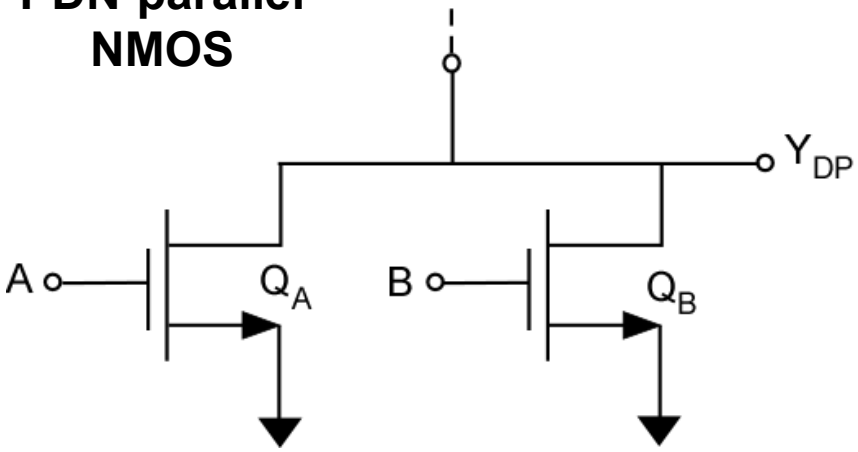
Distributive Law

$$AB + AC + BC + BD = A(B + C) + B(C + D)$$

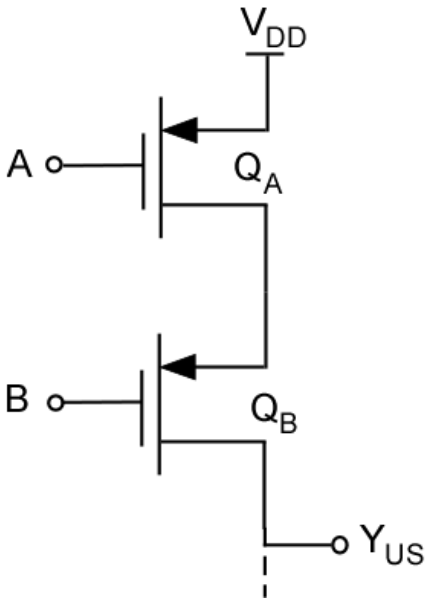
- **General Procedure**
  1. Design PDN to satisfy logic function
  2. Construct PUN to be complementary of PDN in every way
  3. Optimize using distributive rule

Pull-Down and Pull-Up

PDN-parallel NMOS



PUN-series PMOS



$$Y_{DP} = \overline{A + B}$$

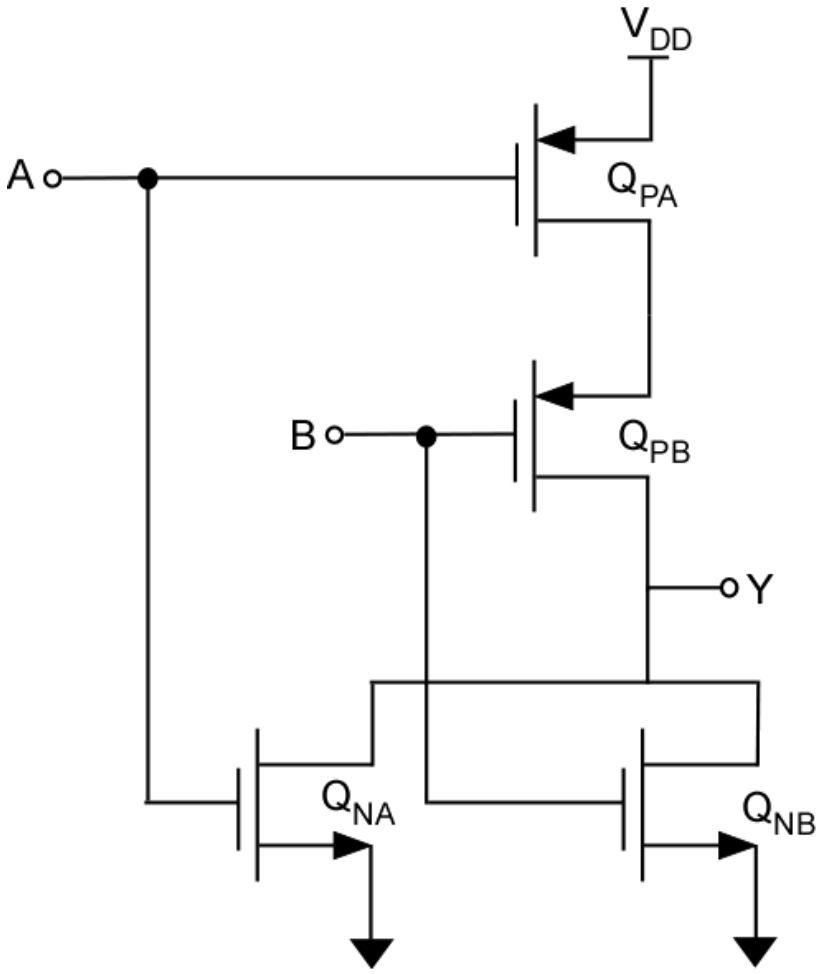
Truth Tables

A	B	Y_{DP}
0	0	1
0	1	0
1	0	0
1	1	0

$$Y_{US} = \overline{A}\,\overline{B}$$

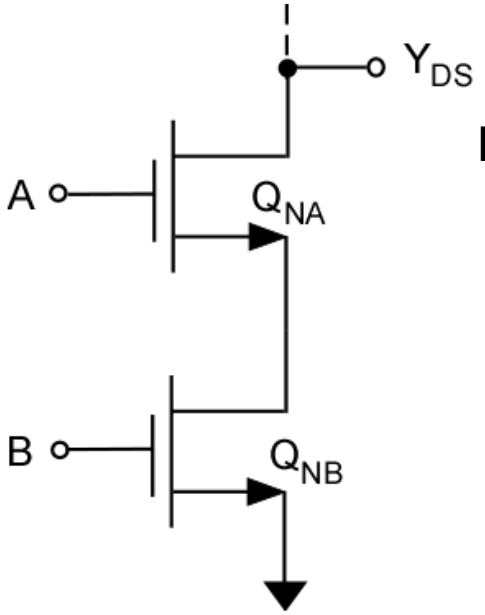
A	B	Y_{US}
0	0	1
0	1	0
1	0	0
1	1	0

Two-Input NOR Gate

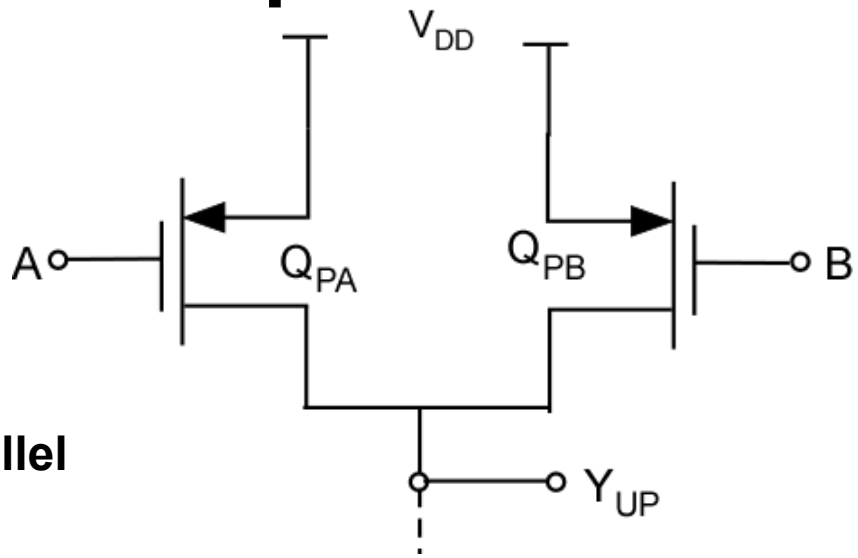


$$Y = \overline{A + B} = \overline{A}\,\overline{B}$$

Pull-Down and Pull-Up



PDN-Series NMOS



PUN-Parallel PMOS

Truth Tables

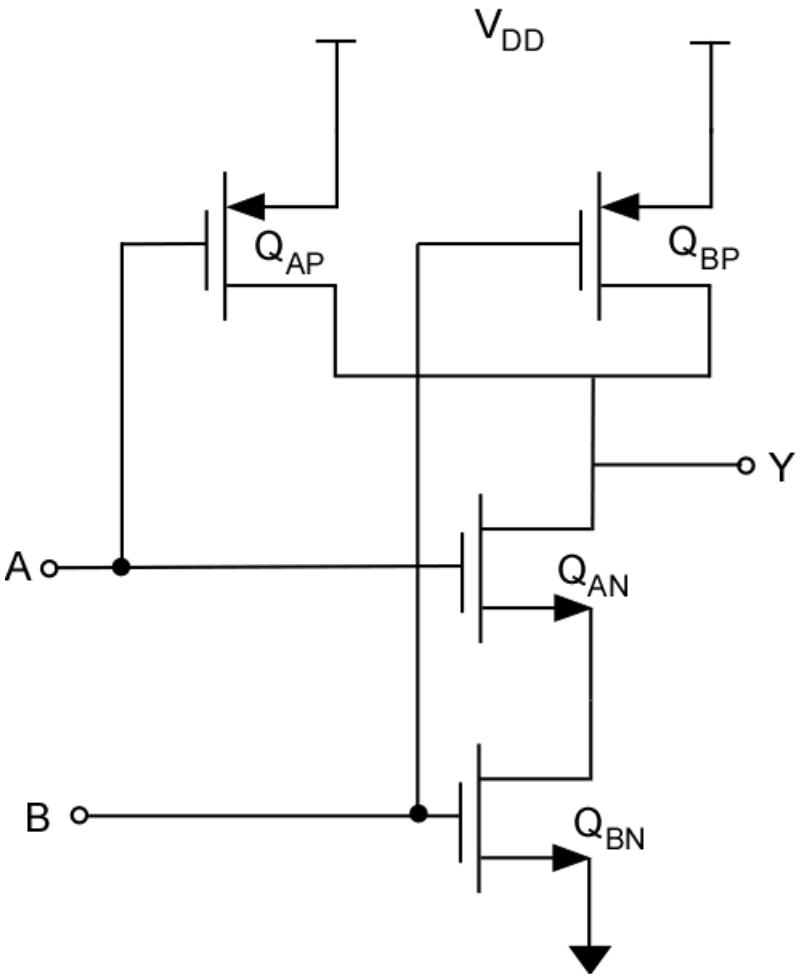
$$Y_{DS} = \overline{AB}$$

A	B	Y_{DS}
0	0	1
0	1	1
1	0	1
1	1	0

$$Y_{UP} = \overline{A} + \overline{B}$$

A	B	Y_{UP}
0	0	1
0	1	1
1	0	1
1	1	0

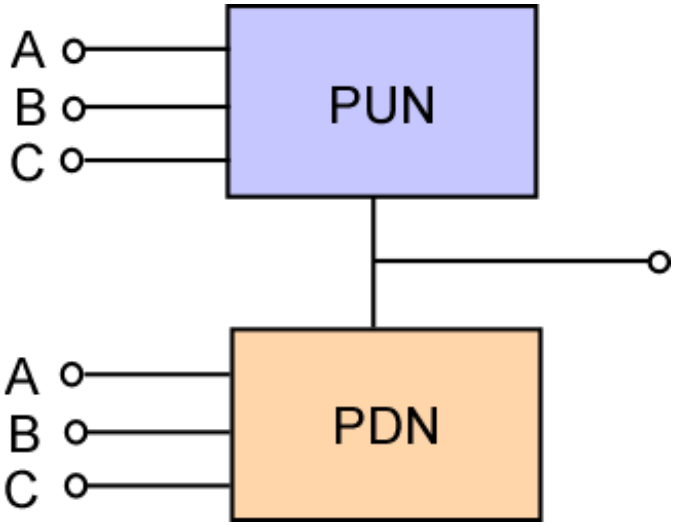
Two-Input NAND Gate



$$Y = \overline{AB} = \overline{A} + \overline{B}$$

CMOS Logic Gate Circuits

- **Two Networks**
  - Pull-down network (PDN) with NMOS
  - Pull-up network (PUN) with PMOS

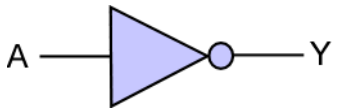
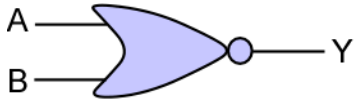
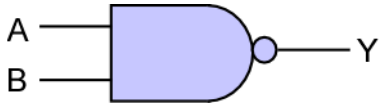
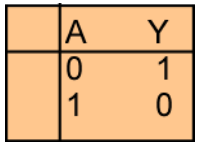
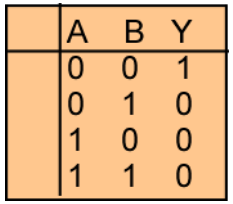
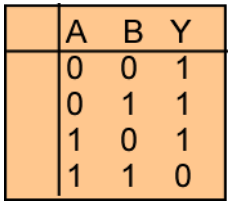


PUN conducts when inputs are low and consists of PMOS transistors

PDN consists of NMOS transistors and is active when inputs are high

- **PDN and PUN utilize devices**
  - In parallel to form OR functions
  - In series to form AND functions

Basic Logic Function

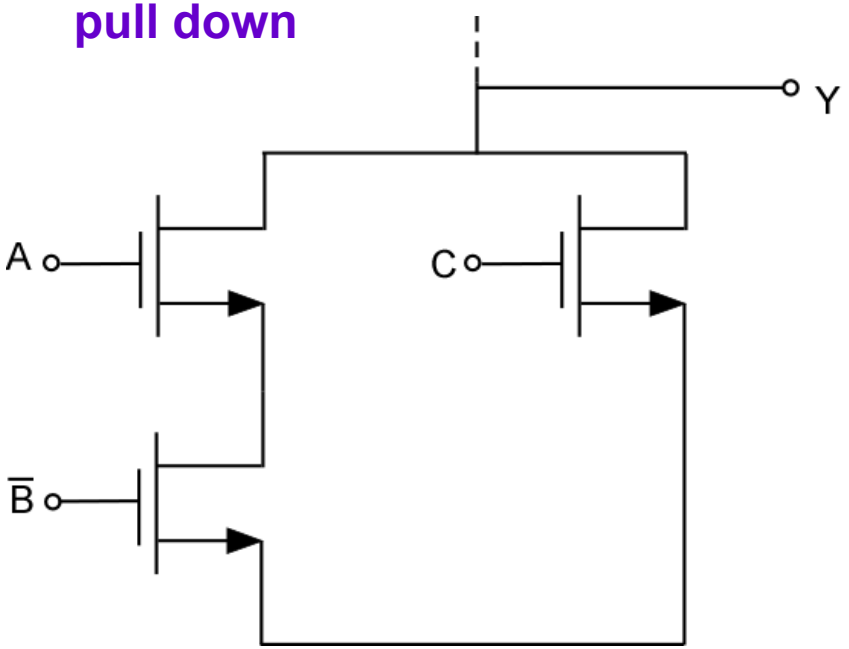
Basic Function	INVERTER	NOR	NAND
Symbol			
# Devices PUN	1 PMOS	2 PMOS-Series	2 PMOS-Parallel
# Devices PDN	1 NMOS	2 NMOS-Parallel	2 NMOS-Series
Truth Table			

Example

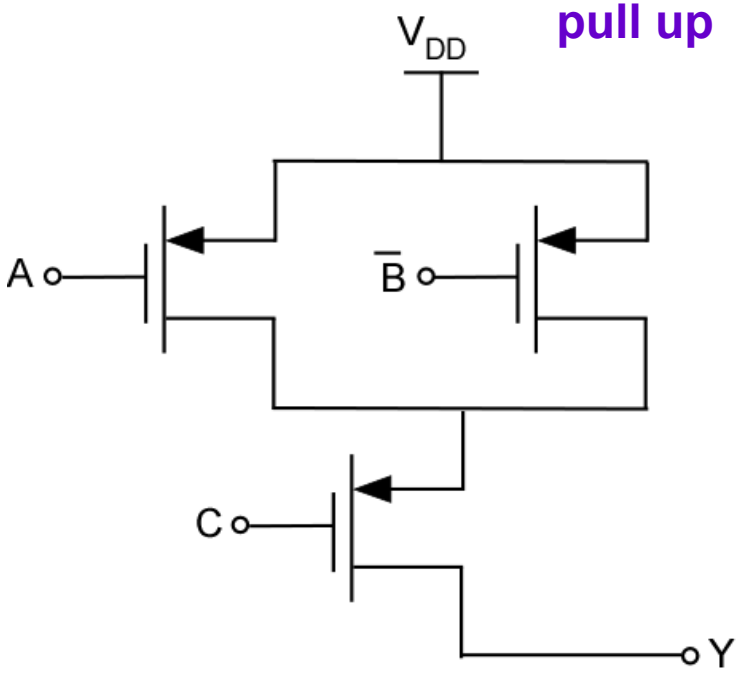
Implement the function

$$\overline{Y} = A\overline{B} + C$$

pull down



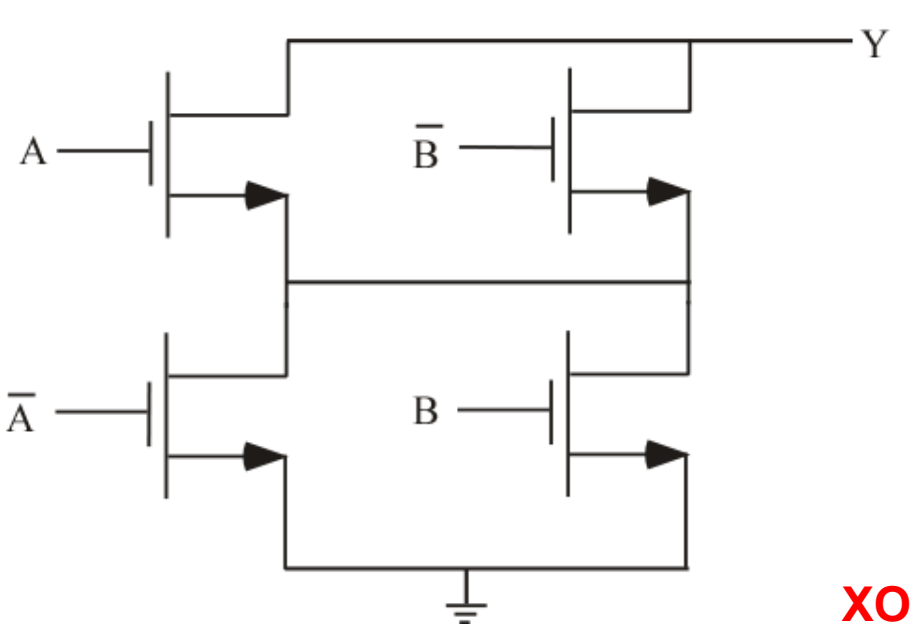
pull up



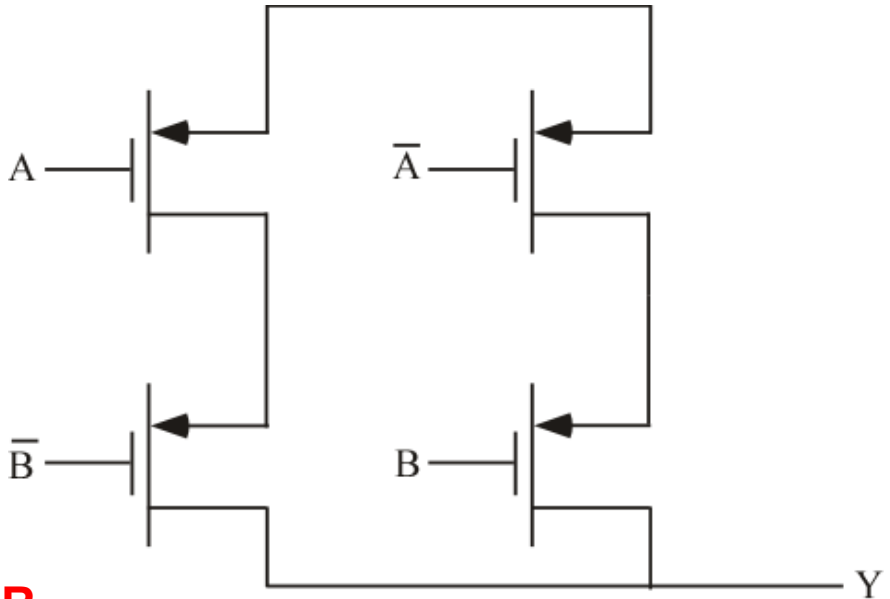
$$Y = \overline{A\overline{B} + C} = \overline{A\overline{B}} \cdot \overline{C} = (\overline{A} + B) \cdot \overline{C}$$

Exclusive-OR (XOR) Function

$$Y = A\overline{B} + \overline{A}B \qquad \overline{Y} = (\overline{A} + B)(A + \overline{B})$$



pull down



pull up

XOR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0