ECE 546
Lecture 10
Transistors

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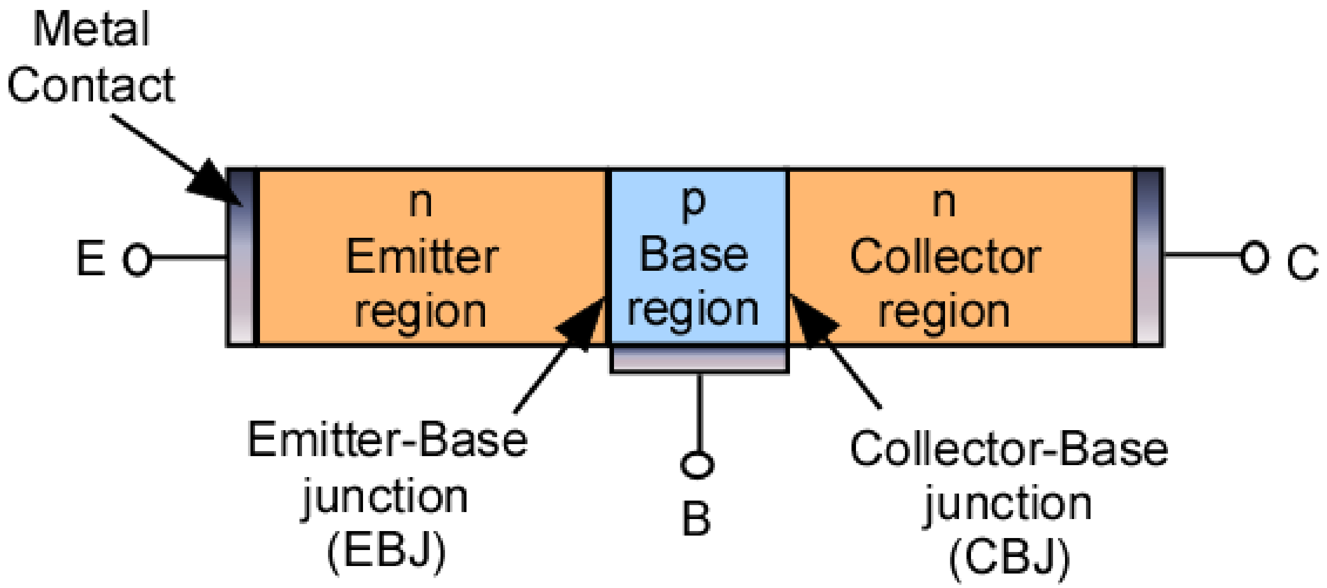
Bipolar Junction Transistor

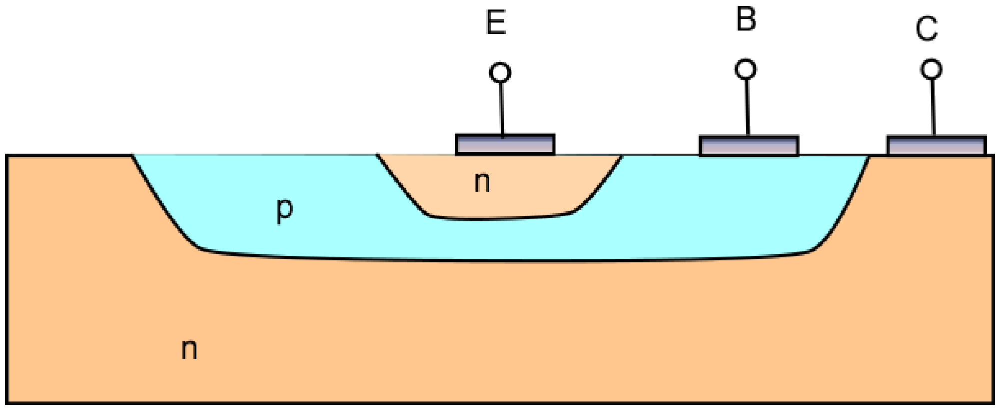
- **Bipolar Junction Transistor (BJT)**
  - First Introduced in 1948 (Bell labs)
  - Consists of 2 pn junctions
  - Has three terminals: emitter, base, collector



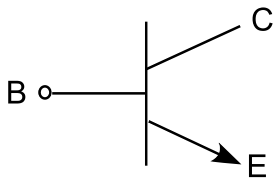
BJT – Modes of Operation

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Forw. Active	Forward	Reverse
Rev. Active	Reverse	Forward
Saturation	Forward	Forward

Structure of BJT's

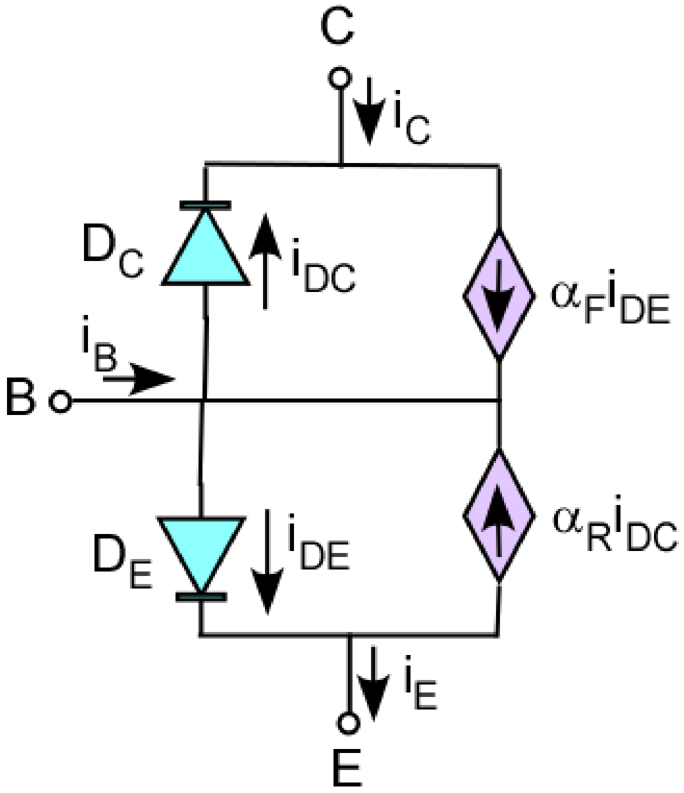


Collector surrounds emitter region ➔ electrons will be collected



Ebers-Moll Model

NPN Transistor



$$i_E = \left(\frac{I_S}{\alpha_F}\right)\left(e^{v_{BE}/V_T} - 1\right) - I_S\left(e^{v_{BC}/V_T} - 1\right)$$

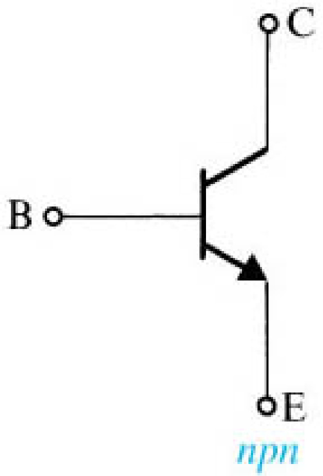
$$i_C = I_S\left(e^{v_{BE}/V_T} - 1\right) - \left(\frac{I_S}{\alpha_R}\right)\left(e^{v_{BC}/V_T} - 1\right)$$

$$i_B = \left(\frac{I_S}{\beta_F}\right)\left(e^{v_{BE}/V_T} - 1\right) + \left(\frac{I_S}{\beta_R}\right)\left(e^{v_{BC}/V_T} - 1\right)$$

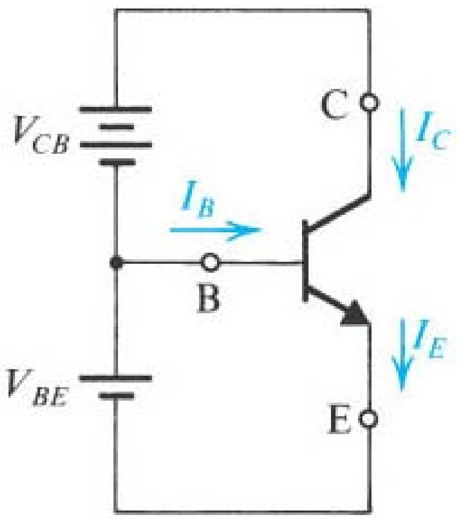
$$\beta_F = \frac{\alpha_F}{1-\alpha_F} \qquad \beta_R = \frac{\alpha_R}{1-\alpha_R}$$

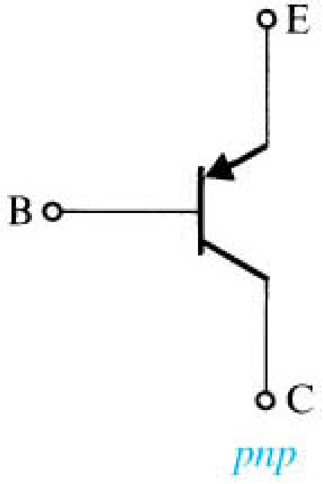
Describes BJT operation in all of its possible modes

BJT Transistor Polarities

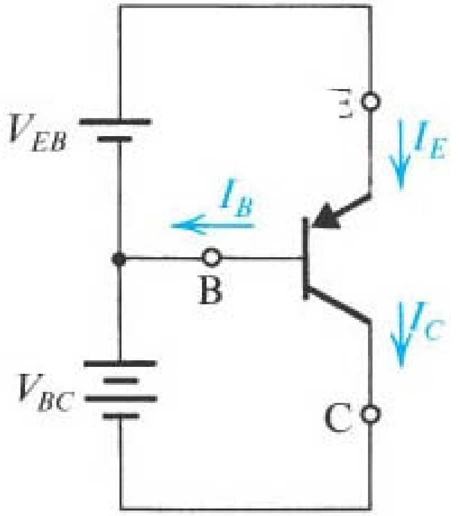


NPN

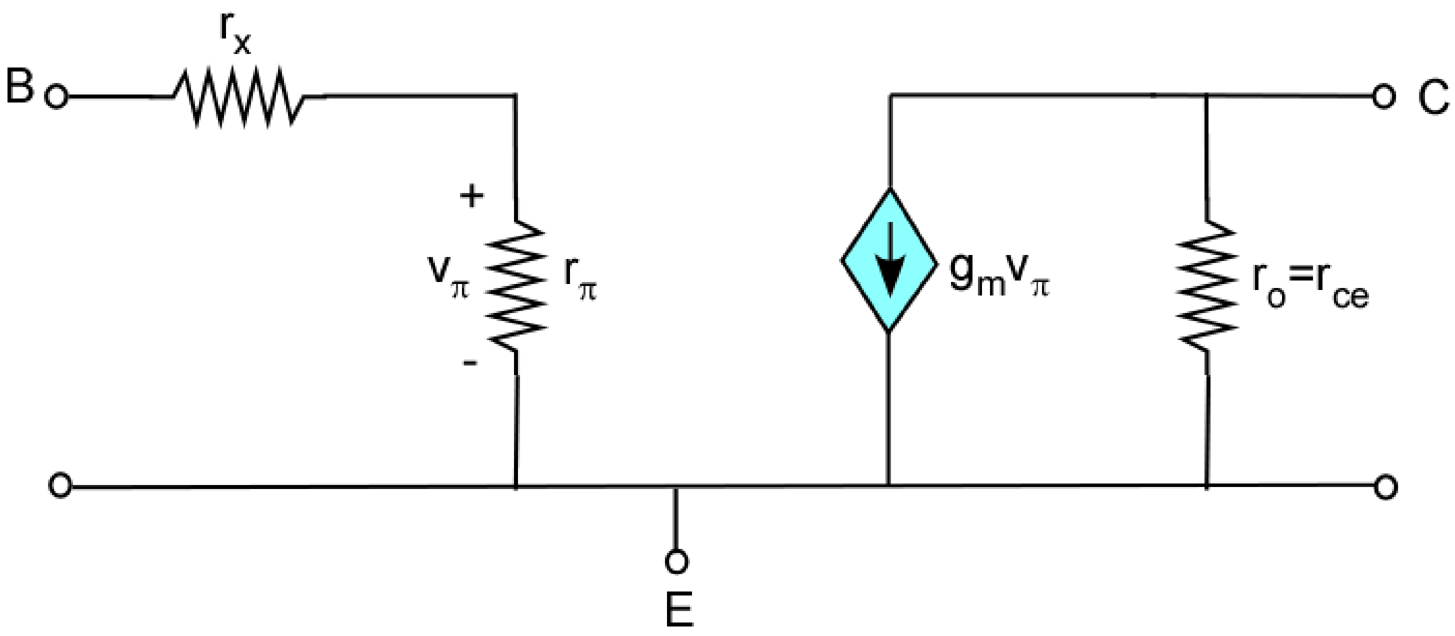




PNP



Hybrid-π Incremental Model for BJTs



r_π: input resistance looking into the base
r_x: parasitic series resistance looking into base – ohmic base resistance
g_m: BJT transconductance
$r_o=r_{ce}$: output collector resistance related to the Early effect

Hybrid-π Parameters

$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{I_C = constant} = \frac{I_C}{V_T}$$

$$r_\pi \text{ is defined as} : r_\pi = \frac{v_\pi}{i_b}$$

$$Since\ i_b = \frac{g_m v_\pi}{\beta} \quad then \quad r_\pi = \frac{\beta}{g_m}$$

Can show that

$$r_\pi = (\beta + 1) r_e$$

$$g_m = \frac{\alpha}{r_e}$$

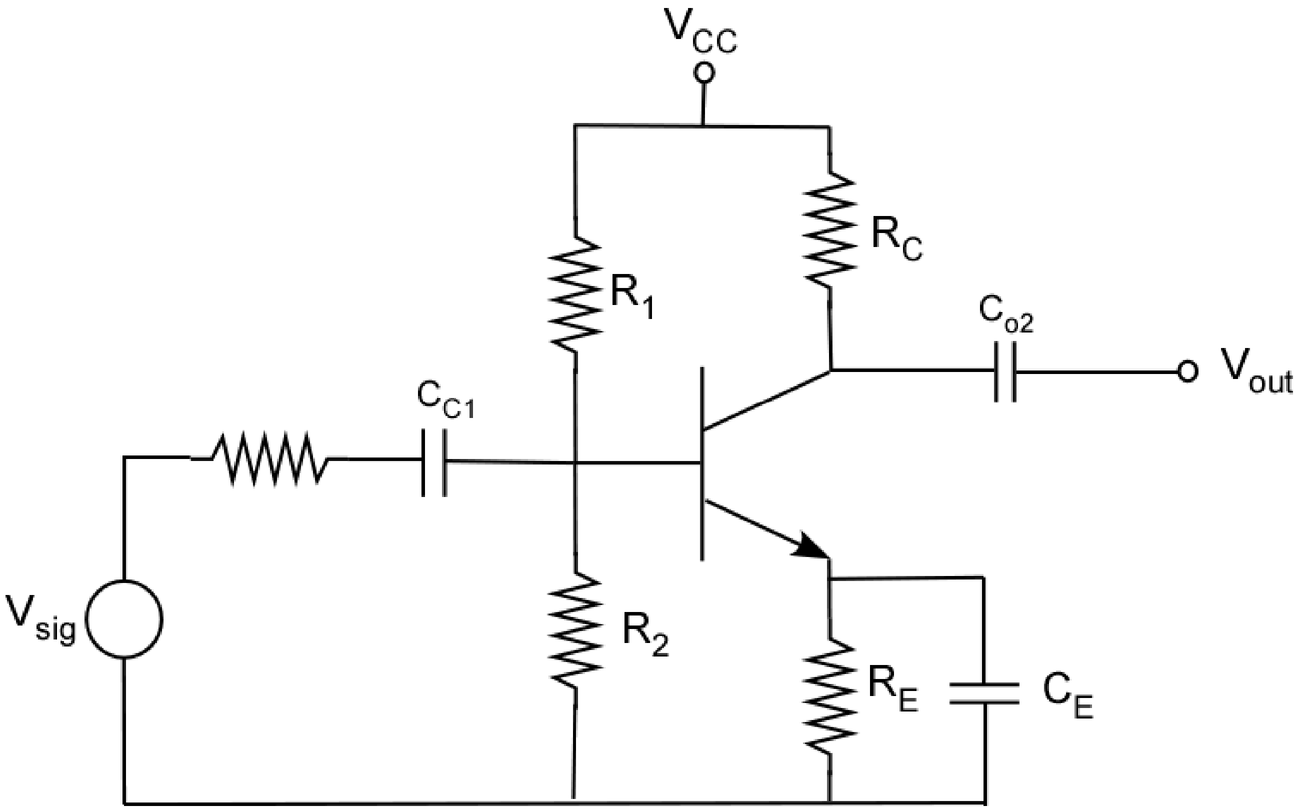
$$\beta = g_m r_\pi$$

$r_{ce} = r_o$ is associated with the Early effect

$$r_{ce} = r_o = \frac{|V_A|}{I_C} = \frac{|V_A|}{\beta I_B}$$

$$g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

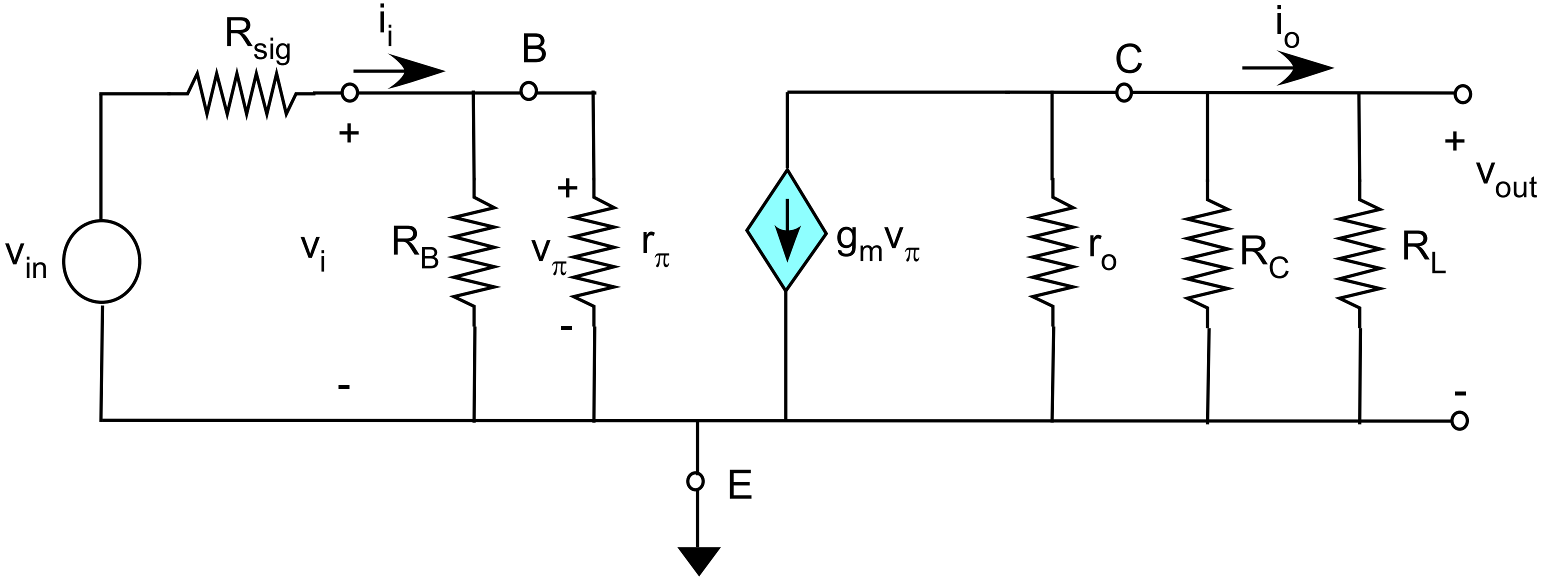
Common Emitter (CE) Amplifier



Bias: Choose R_1 & R_2 to set V_B → V_E is then set. Choose R_E to set $I_E \sim I_C$. Quiescent point of V_{out} will be determined by R_C. Emitter is an AC short.

Incremental Model for CE Amplifier

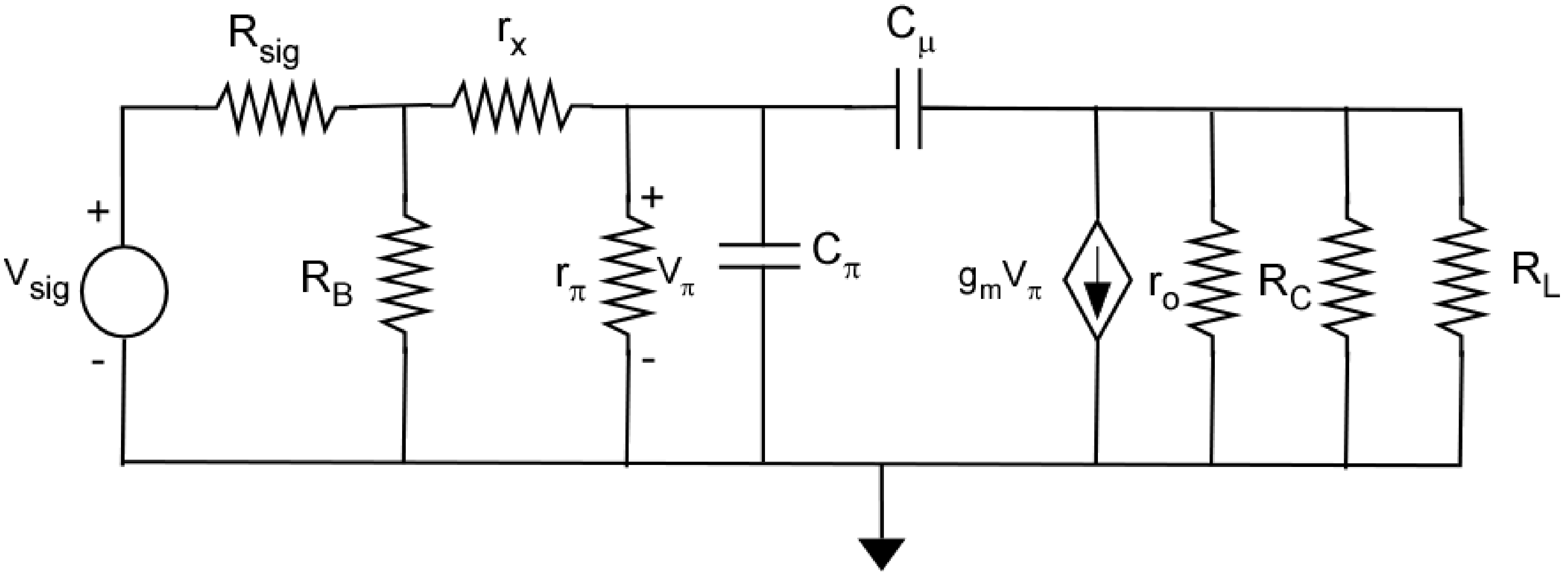
Hybrid-π model (ignoring r_x)



$$R_B = R_1 \,||\, R_2 \qquad R_{in} = \frac{v_i}{i_i} = R_B \,||\, r_\pi$$

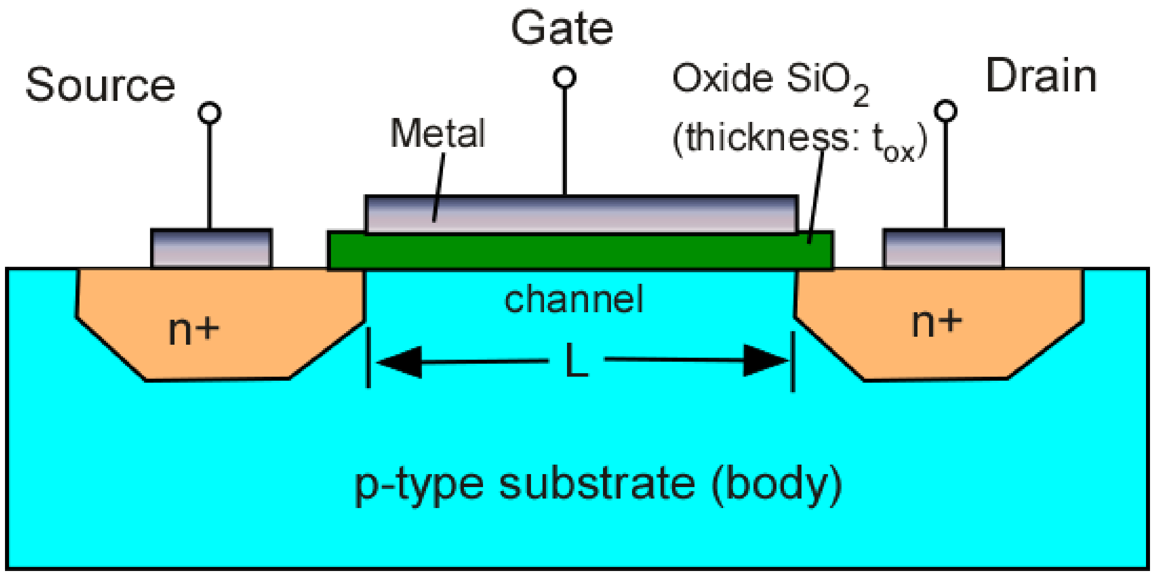
$$Sometimes\ R_B \gg r_\pi\ and\ R_{in} \simeq r_\pi$$

CE High-Frequency Model



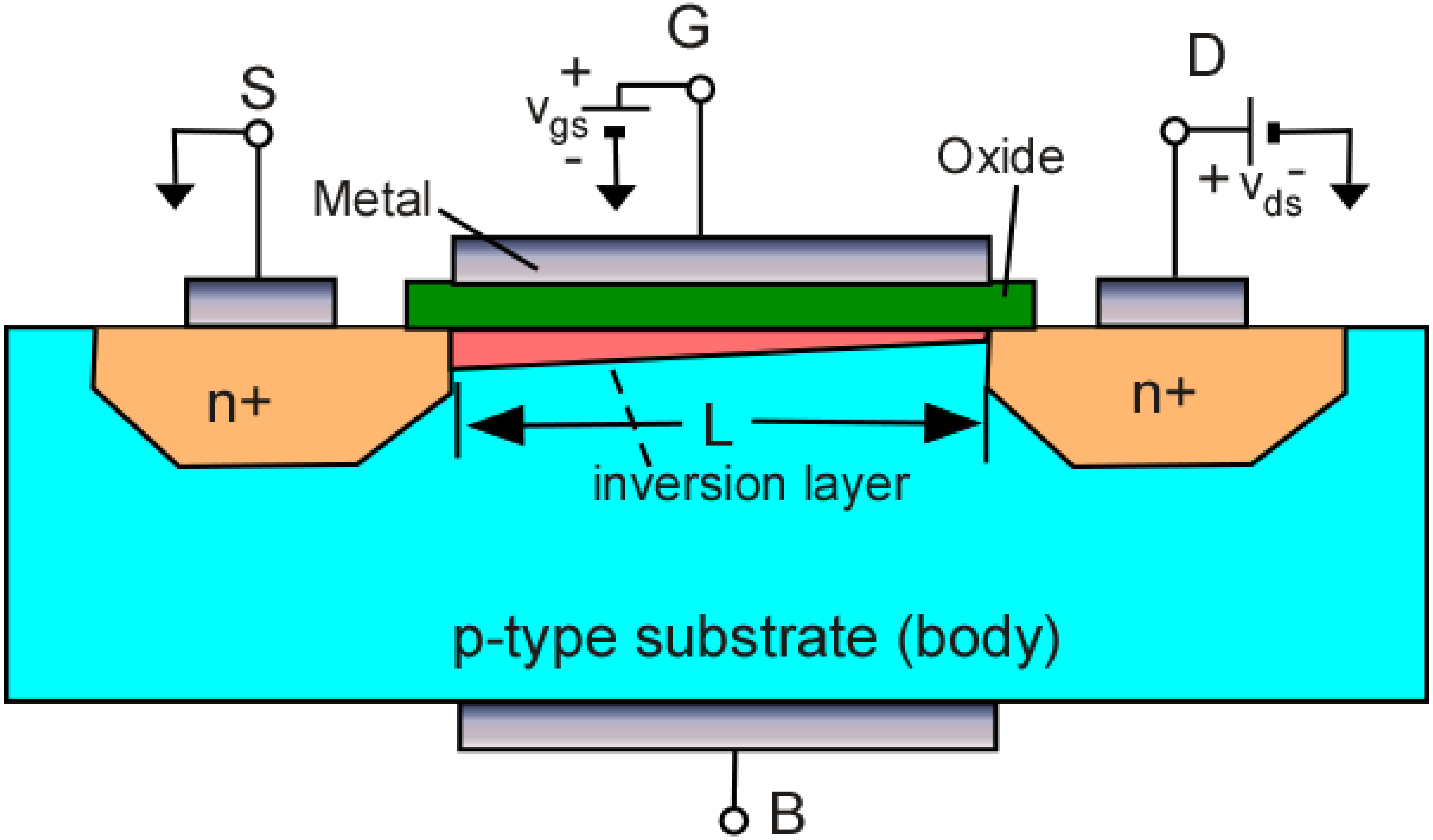
$$R_B = R_1 \,||\, R_2$$

NMOS Transistor

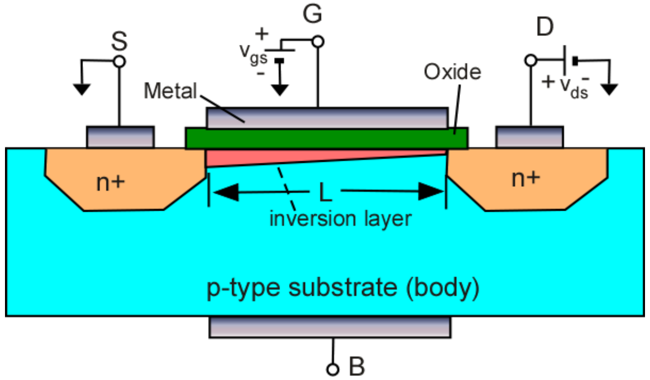


- **NMOS Transistor**
  - N-Channel MOSFET
  - Built on p-type substrate
  - MOS devices are smaller than BJTs
  - MOS devices consume less power than BJTs

MOS


G
S
D
+
v_{gs}
-
Metal
Oxide
$+ v_{ds} -$
n+
n+
L
inversion layer
p-type substrate (body)
B

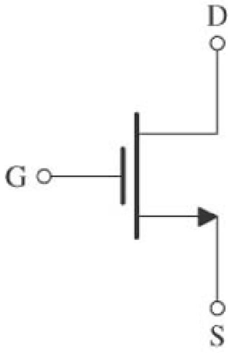
NMOS – Regions of Operation



Cut off

$$V_{GS} < V_T \qquad I_D = 0$$

Triode



$$V_{GS} > V_T$$

$$V_{DS} < (V_{GS} - V_T) \qquad I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

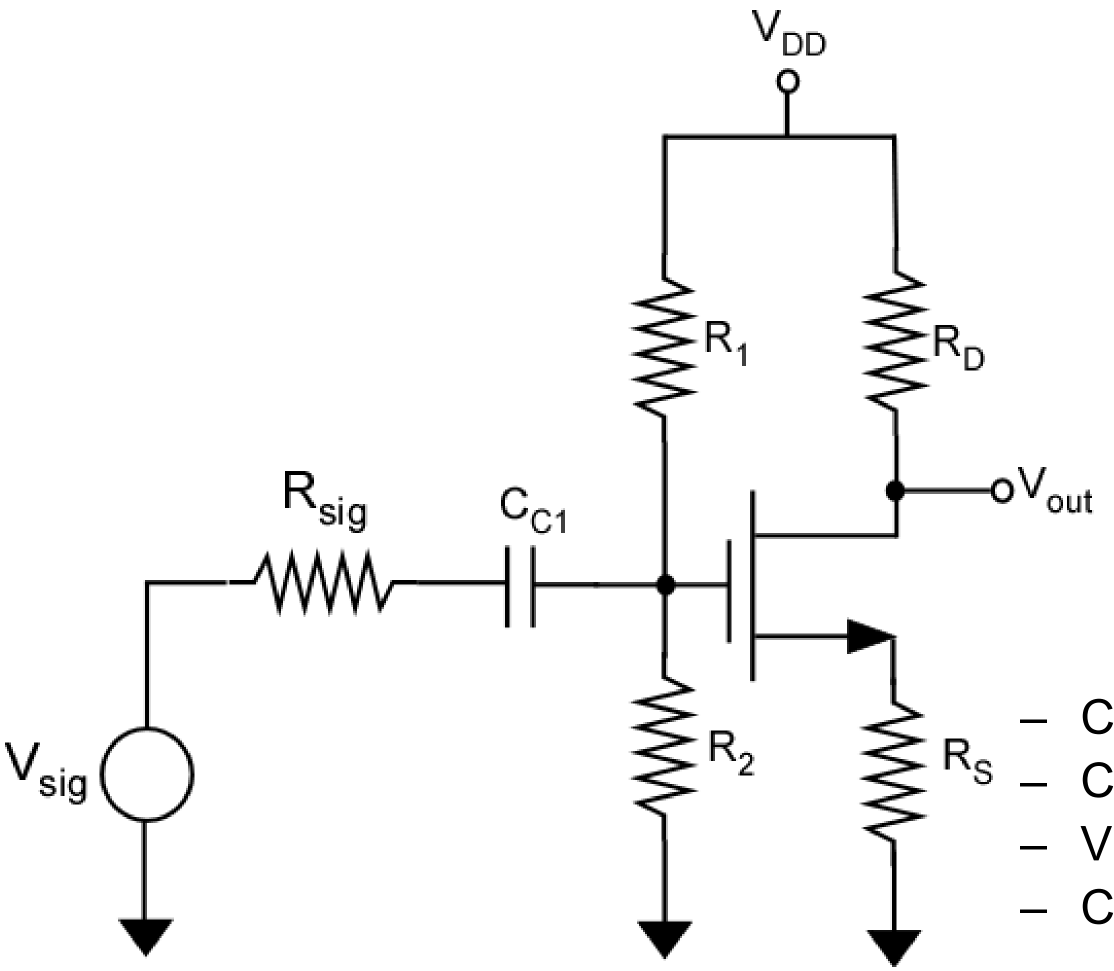
C_{ox}: gate oxide capacitance
μ: electron mobility
L: channel length
W: channel width
V_T: threshold voltage

Saturation

$$V_{GS} > V_T$$

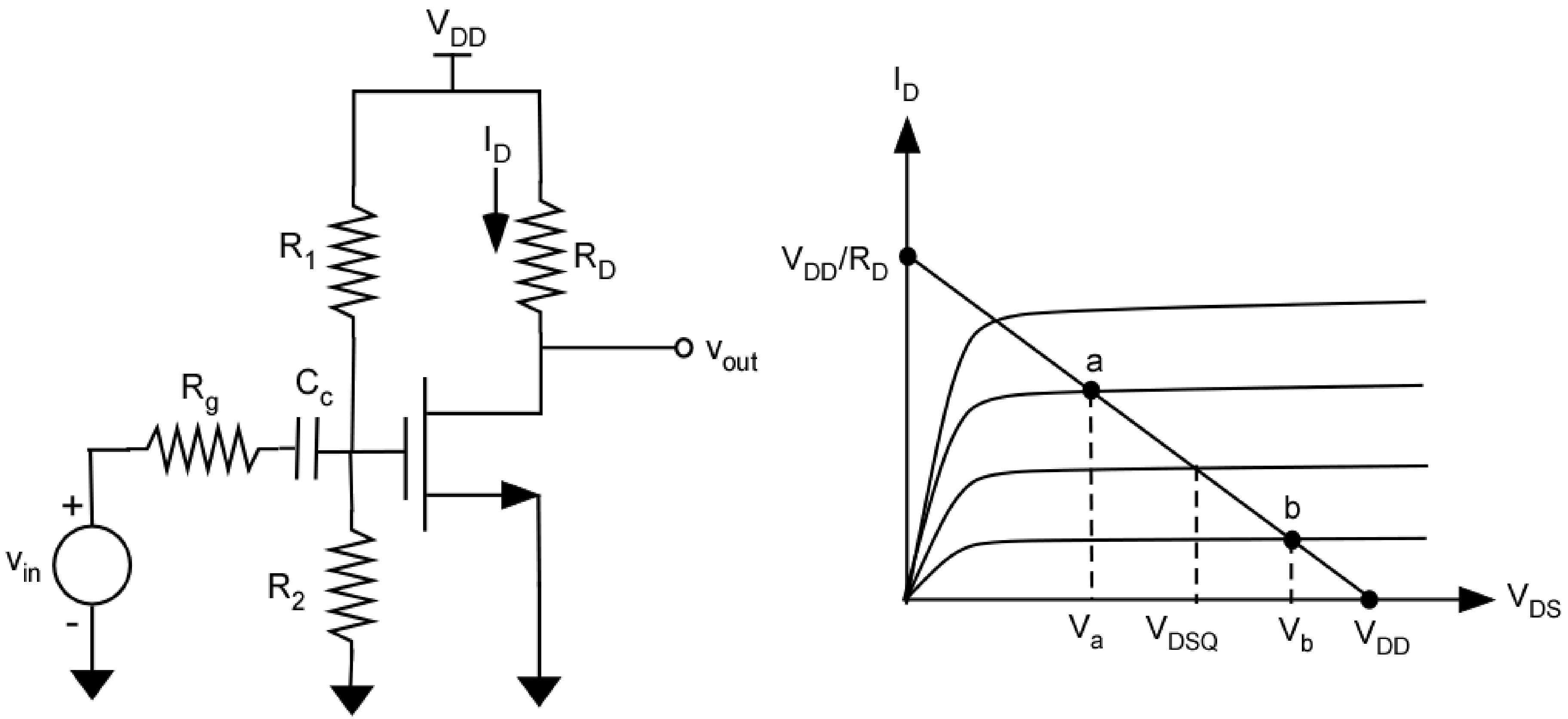
$$V_{DS} > (V_{GS} - V_T) \qquad I_D = \mu_n C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2$$

NMOS Bias



- Choose R_1 and R_2 to fix V_G
- Choose R_S and R_2 to fix V_S
- V_{GS} determines I_D
- Choose R_D to fix V_D

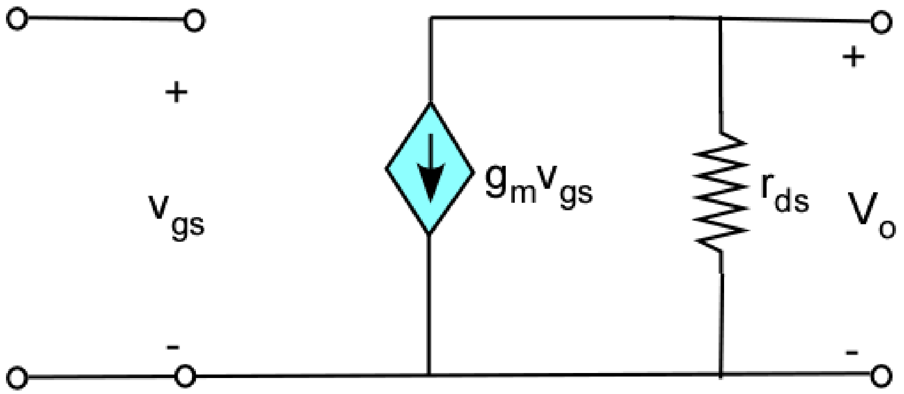
Common Source MOSFET Amplifier



Bias is to keep MOS in saturation region

Common Source MOSFET Amplifier

Small-Signal Equivalent Circuit for MOS (device only)



$$I_D = \frac{1}{2} k_n' \frac{W}{L} \left(V_{GS} - V_T \right)^2$$

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{GS} = V_{GSQ}} = \frac{2 I_D}{V_{eff}}$$

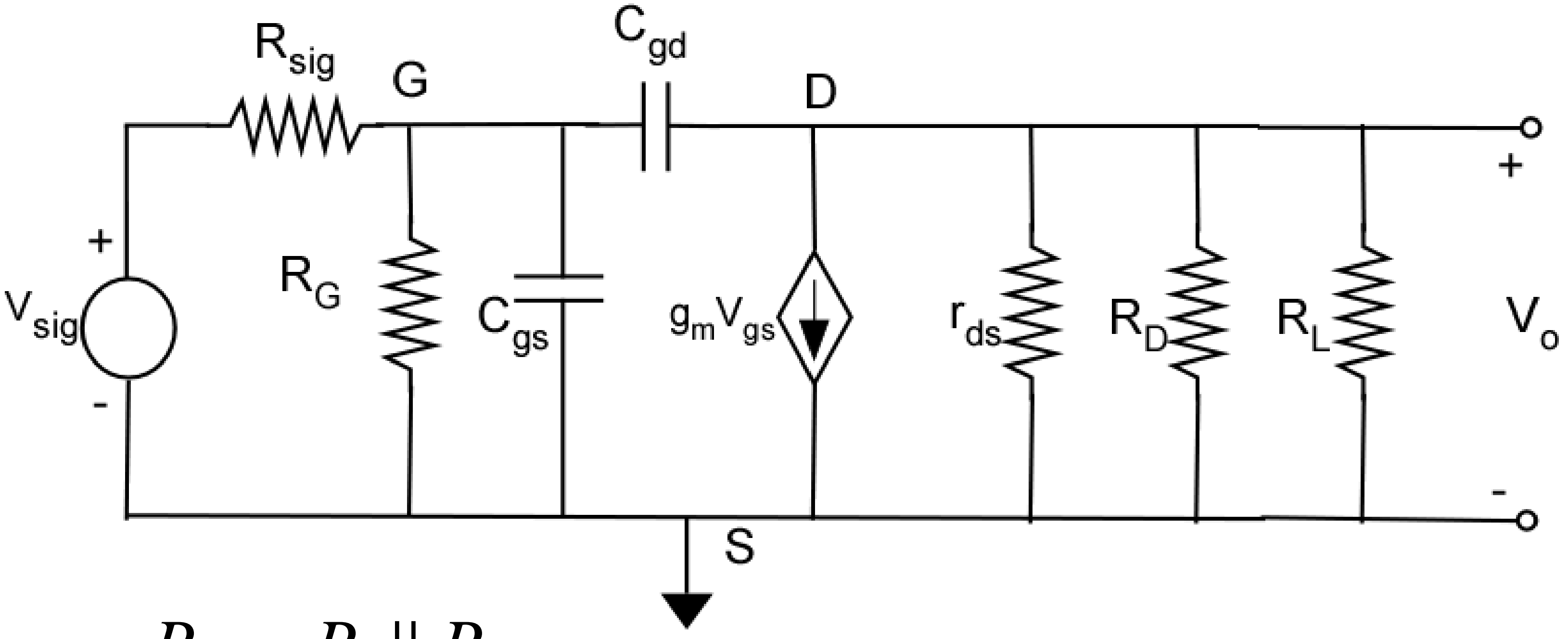
$$where\ V_{GS} - V_T = V_{eff}$$

Which leads to

$$g_m = \sqrt{2k_n'} \sqrt{W/L} \sqrt{I_D}$$

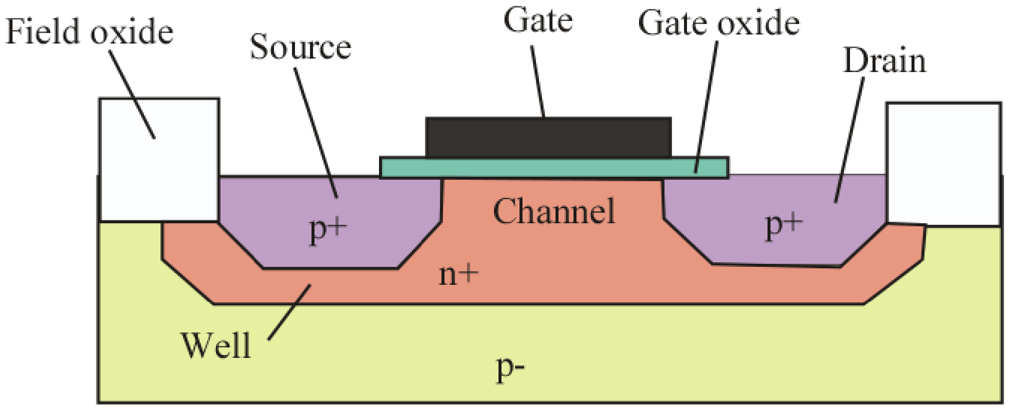
$$g_m \text{ is proportional to} = \sqrt{W/L}$$

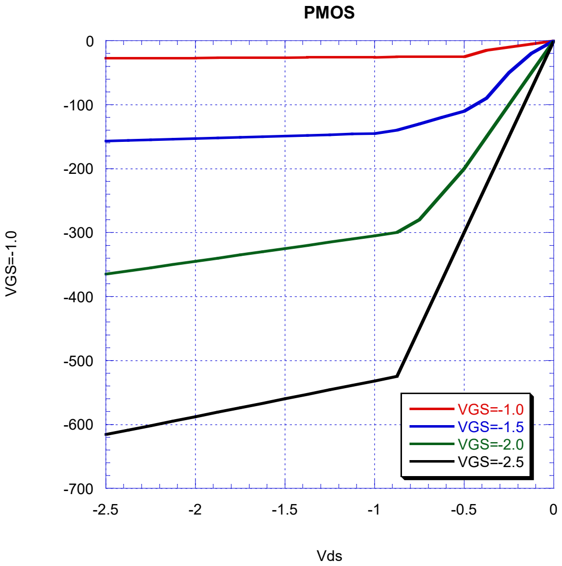
CS - High-Frequency Response



$$R_G = R_1 \,||\, R_2$$

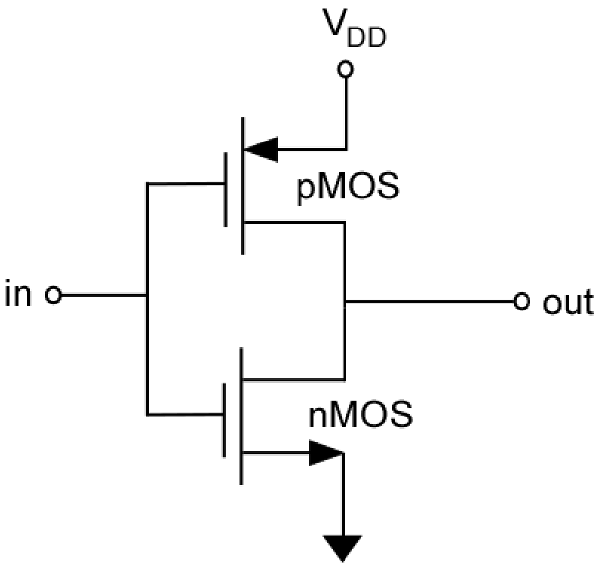
PMOS Transistor

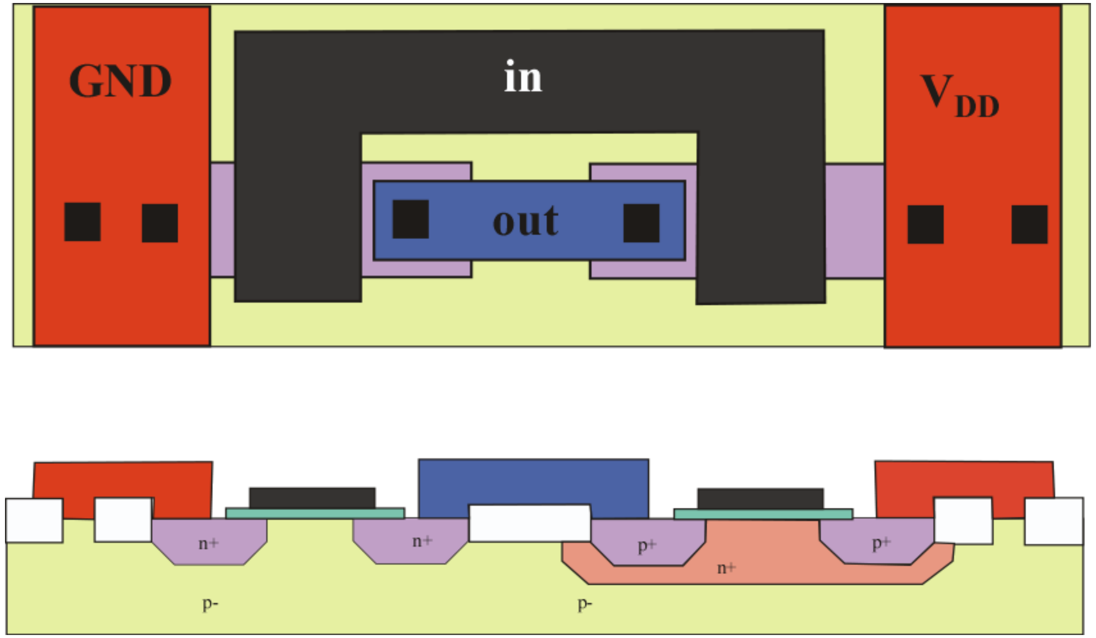




- All polarities are reversed from nMOS
- v_{GS}, v_{DS} and V_t are negative
- Current i_D enters source and leaves through drain
- Hole mobility is lower $\Rightarrow$ low transconductance
- nMOS favored over pMOS

Complementary MOS





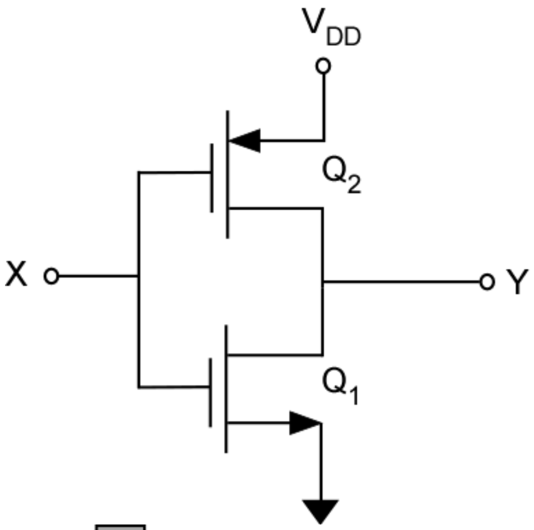
- **CMOS Characteristics**
  - Combine nMOS and pMOS transistors
  - pMOS size is larger for electrical symmetry

CMOS

- **Advantages**
  - Virtually, no DC power consumed
  - No DC path between power and ground
  - Excellent noise margins (V_{OL}=0, V_{OH}=V_{DD})
  - Inverter has sharp transfer curve

- **Drawbacks**
  - Requires more transistors
  - Process is more complicated
  - pMOS size larger to achieve electrical symmetry
  - Latch up

CMOS Layout



■ n Well

🟪 Active region (LOCOS)

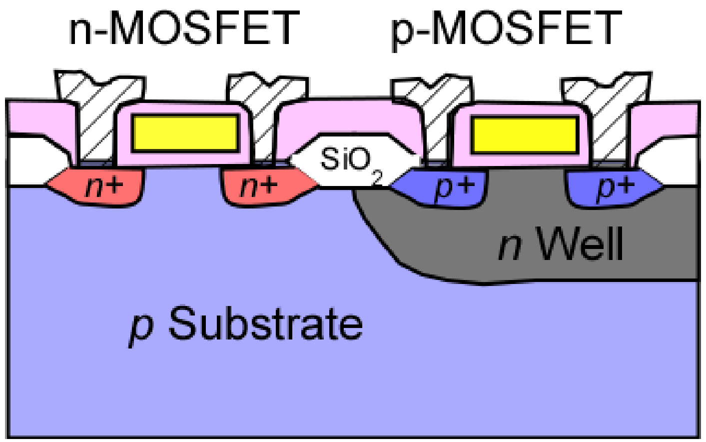
🟨 Poly 1 (poly-Si gate)

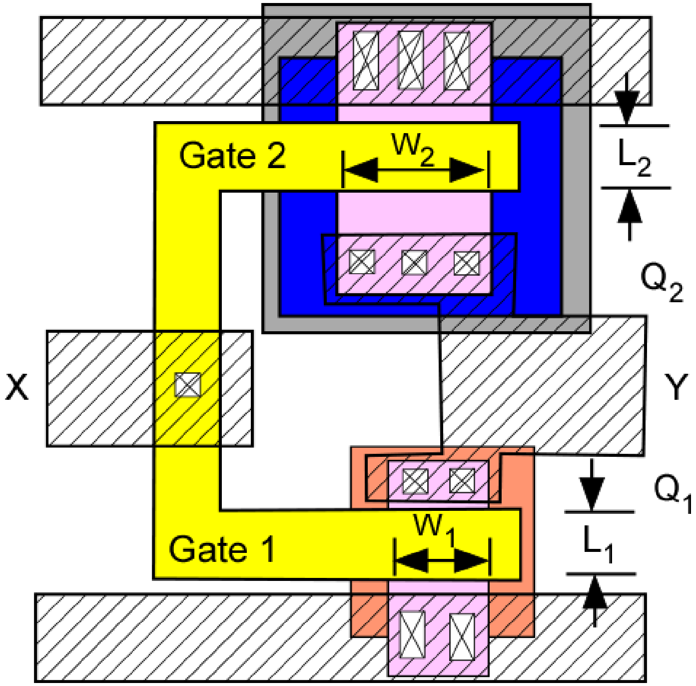
🟧 n+ diffusion

🟦 p+ diffusion

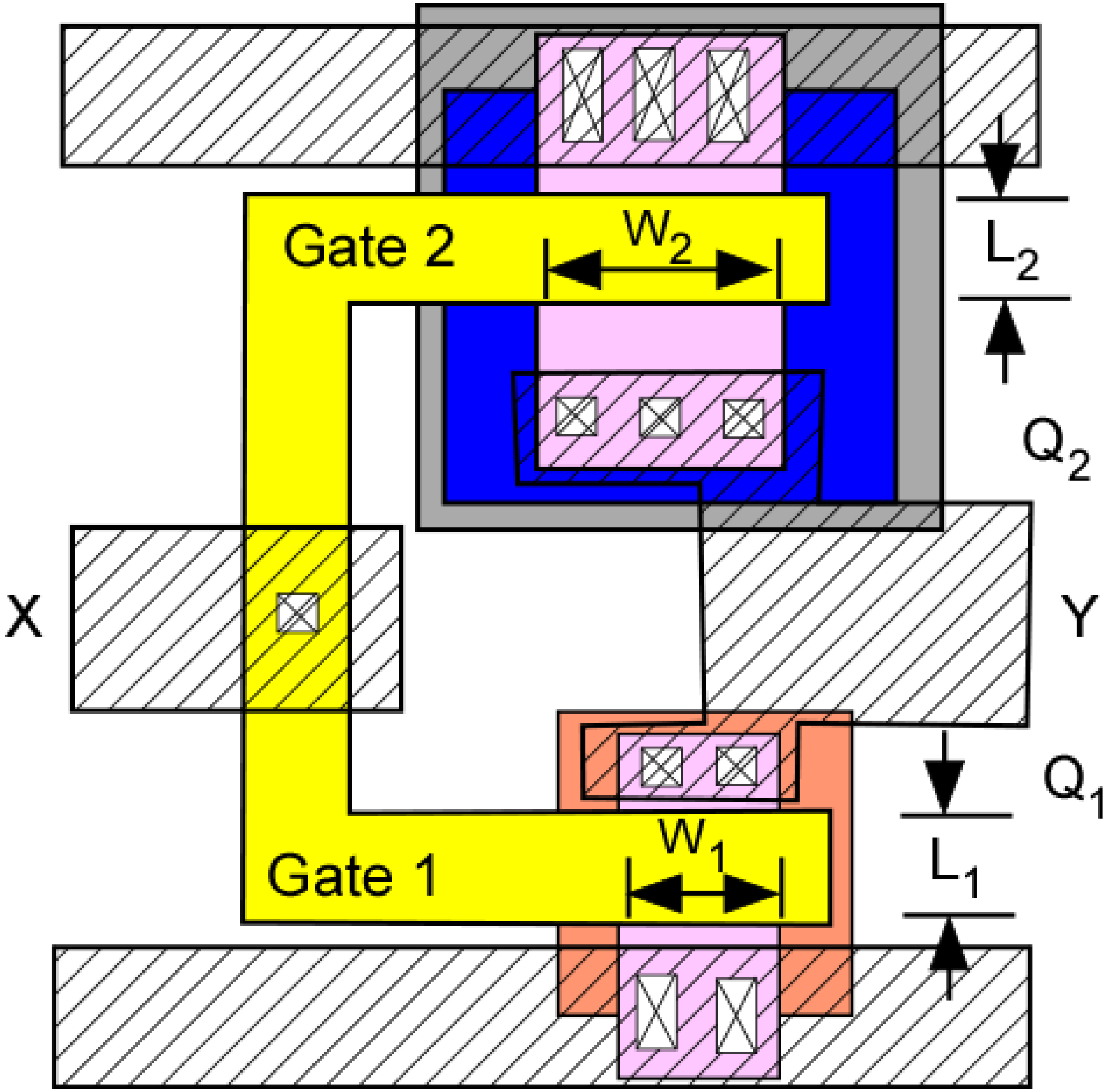
☒ Contact hole

▨ Metal 1





CMOS Layout



Voltage Transfer Characteristics (VTC)

The static operation of a logic circuit is determined by its VTC

- **In low state: noise margin is *NM_L***

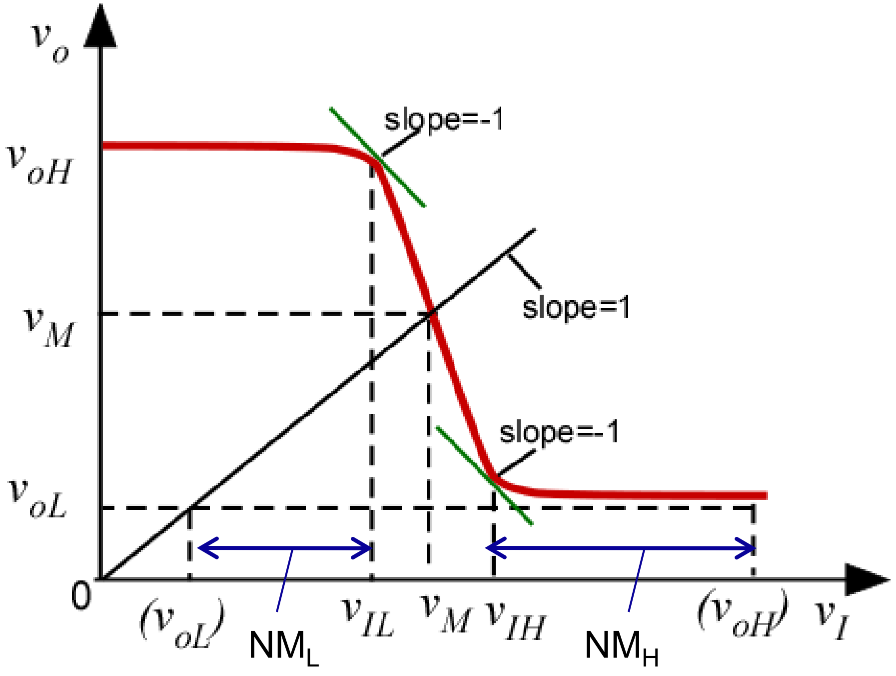
$$NM_L = V_{IL} - V_{OL}$$

- **In high state: noise margin is *NM_H***

$$NM_H = V_{OH} - V_{IH}$$

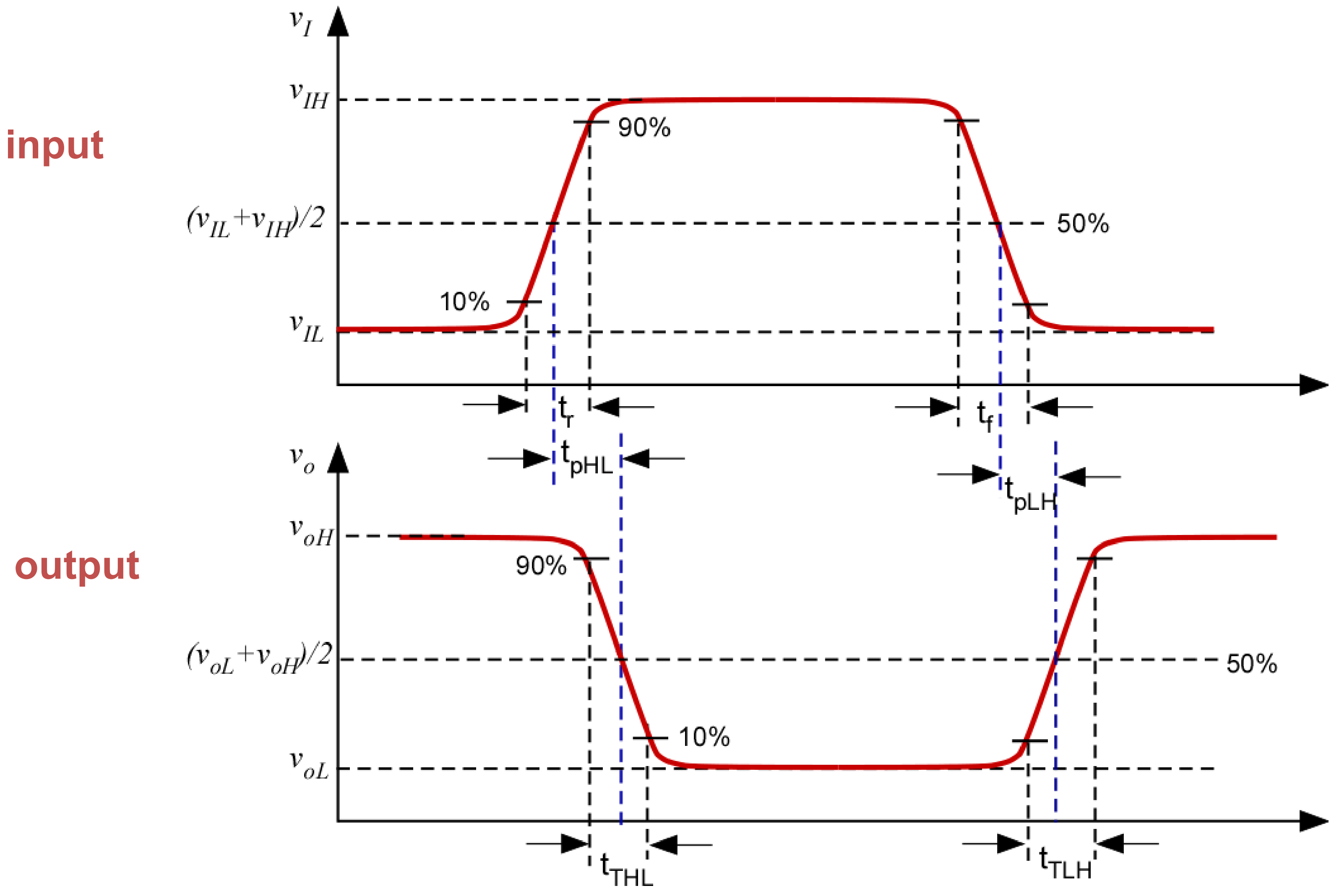
- **An ideal VTC will maximize noise margins**

Optimum: $NM_L = NM_H = V_{DD}/2$



V_{IL} and V_{IH} are the points where the slope of the VTC=-1

Switching Time & Propagation Delay

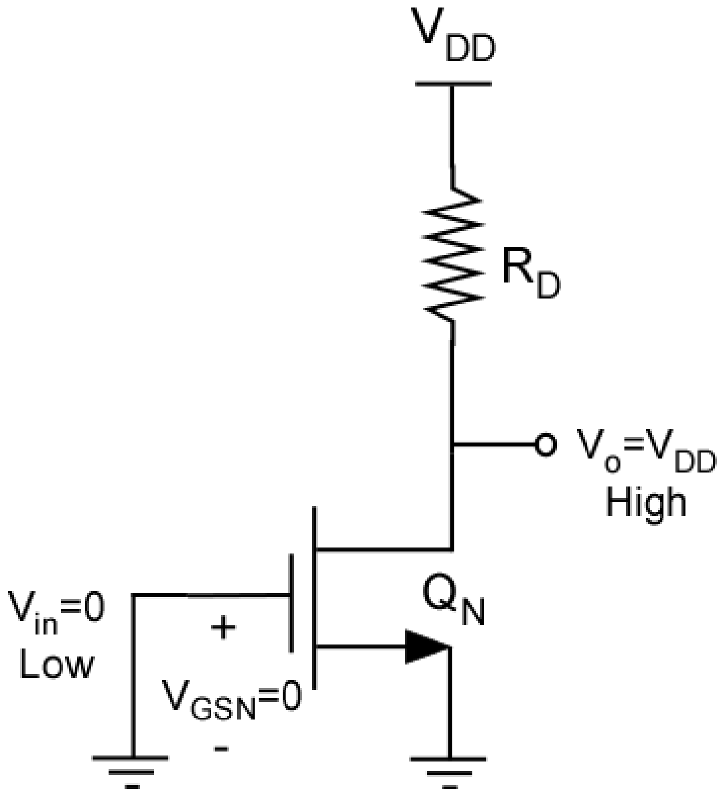


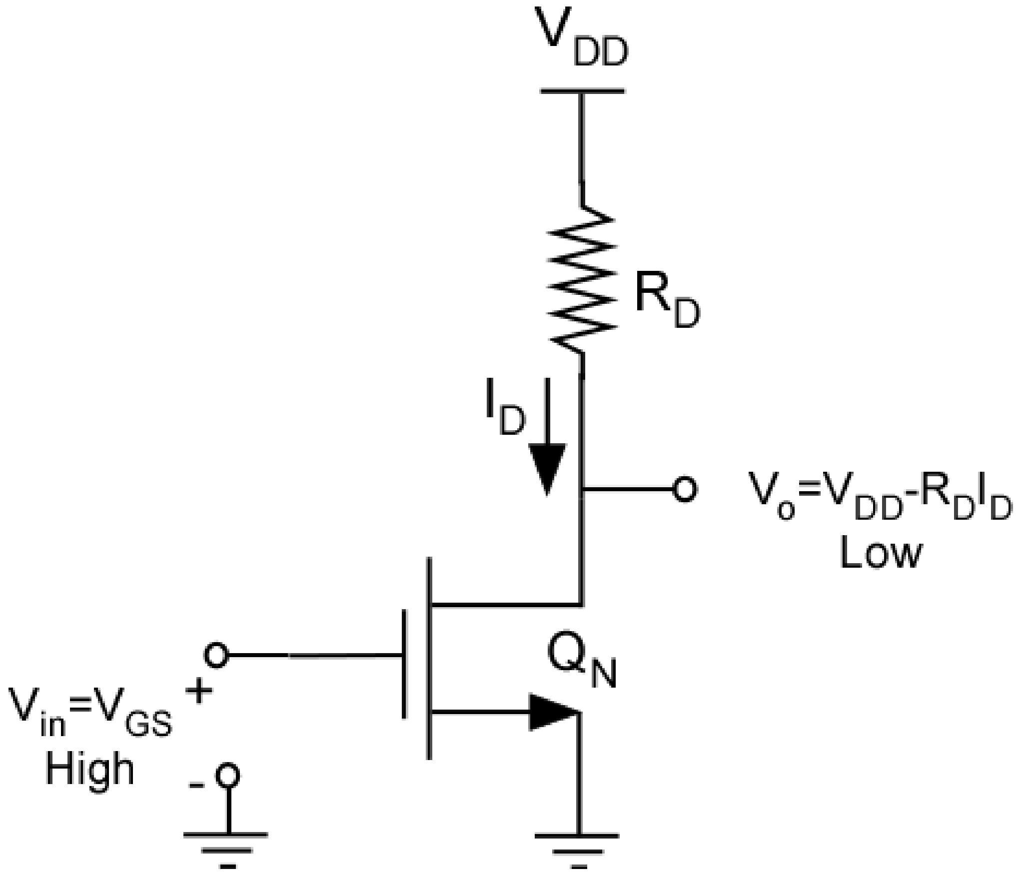
Switching Time & Propagation Delay

t_r=rise time (from 10% to 90%)
t_f=fall time (from 90% to 10%)
t_{pLH}=low-to-high propagation delay
t_{pHL}=high-to-low propagation delay

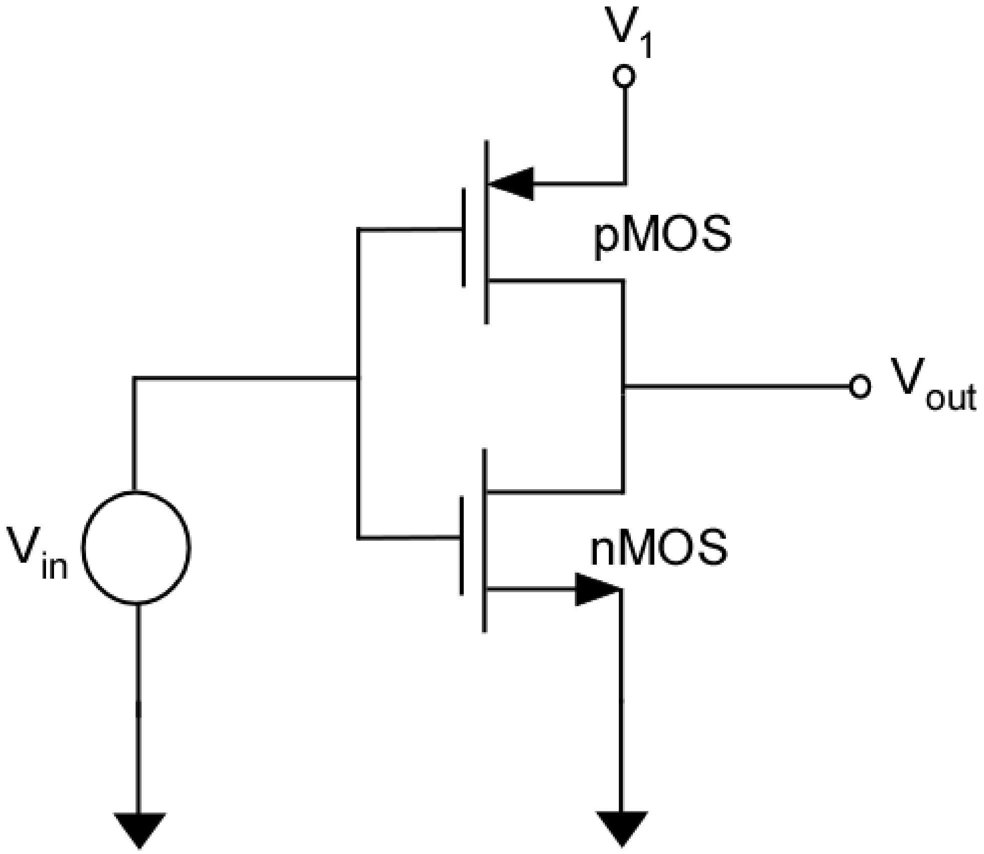
Inverter propagation delay: $$t_p = \frac{1}{2}\left(t_{pLH} + t_{pHL}\right)$$

NMOS Switch


V_{DD}
R_D
$V_o=V_{DD}$
High
Q_N
$V_{in}=0$
Low
+
$V_{GSN}=0$
-


V_{DD}
R_D
I_D
$V_o=V_{DD}-R_DI_D$
Low
Q_N
$V_{in}=V_{GS}$
High
+
-

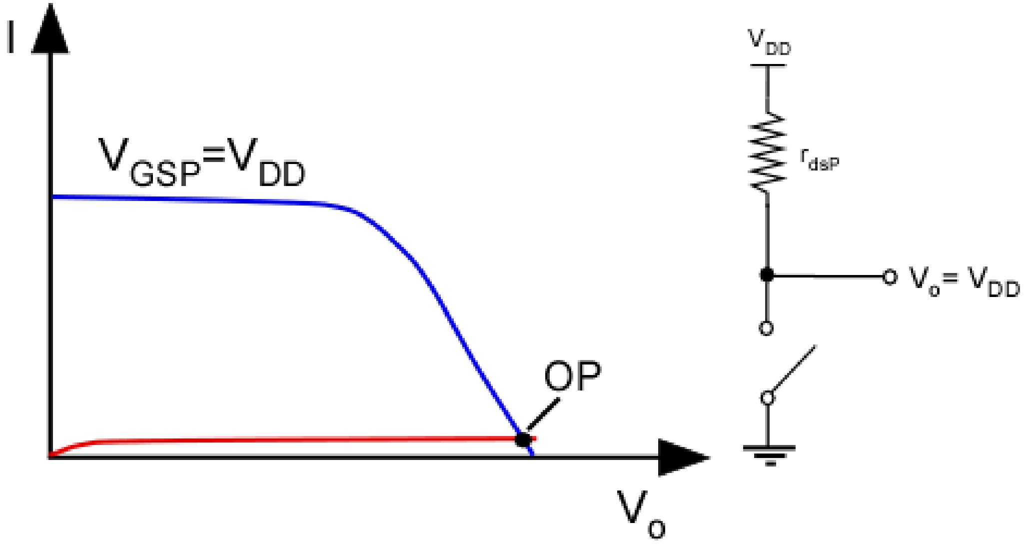
CMOS Switch



CMOS switch is called an inverter

The body of each device is connected to its source ➔ NO BODY EFFECT

CMOS Switch – Input Low



NMOS

$$V_{GSN} < V_{TN} \Rightarrow OFF$$

r_{dsn} high

PMOS

$$r_{dsp} = \frac{1}{k_p^{'}\left(\frac{W}{L}\right)_p \left(V_{DD} - \left|V_{TP}\right|\right)}$$

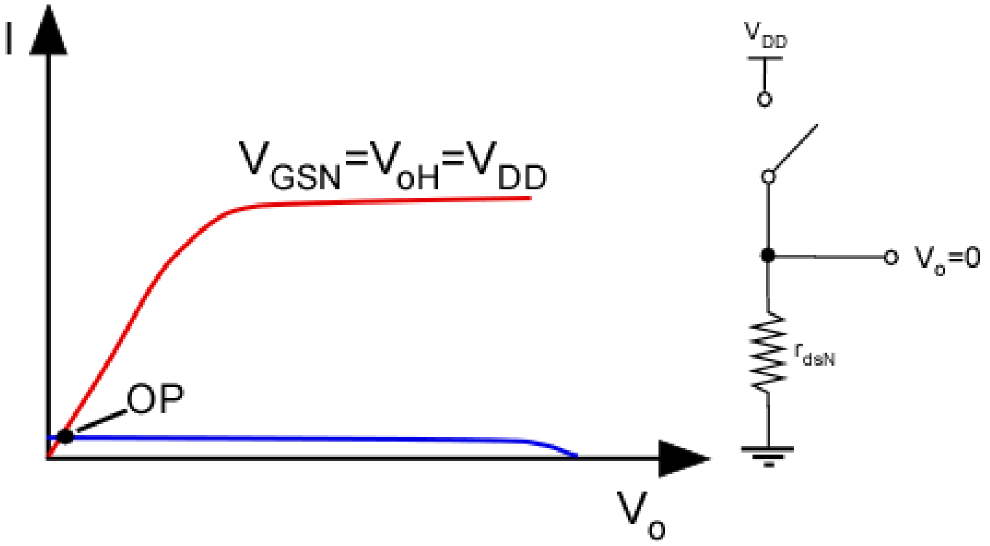
r_{dsp} is low

CMOS Switch – Input High

NMOS

$$r_{dsn} = \frac{1}{k_n^{'}\left(\frac{W}{L}\right)_n\left(V_{DD} - V_{TN}\right)}$$

r_{dsn} is low

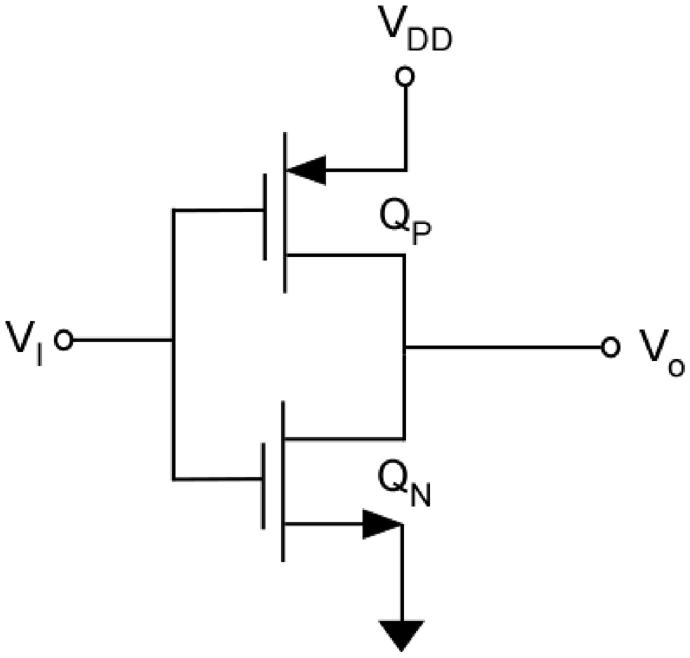


PMOS

$$V_{GSP} > V_{TP} \Rightarrow OFF$$

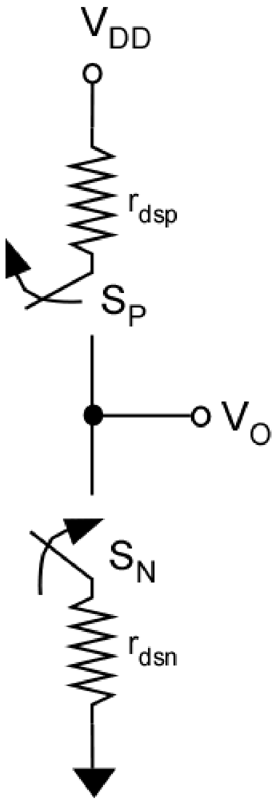
r_{dsp} high

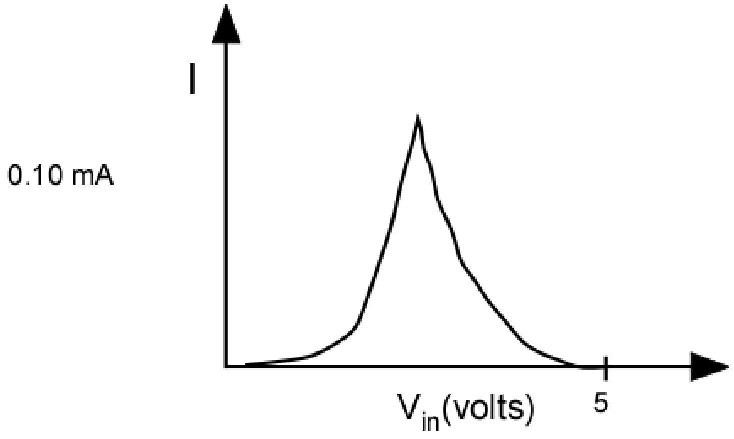
CMOS Inverter



$$r_{dsn} = \frac{1}{k_N^{'}\left(\frac{W}{L}\right)_n (V_{DD} - V_T)}$$

$$r_{dsp} = \frac{1}{k_P^{'}\left(\frac{W}{L}\right)_p (V_{DD} - V_T)}$$





Short switching transient current
➔ low power

CMOS Inverter

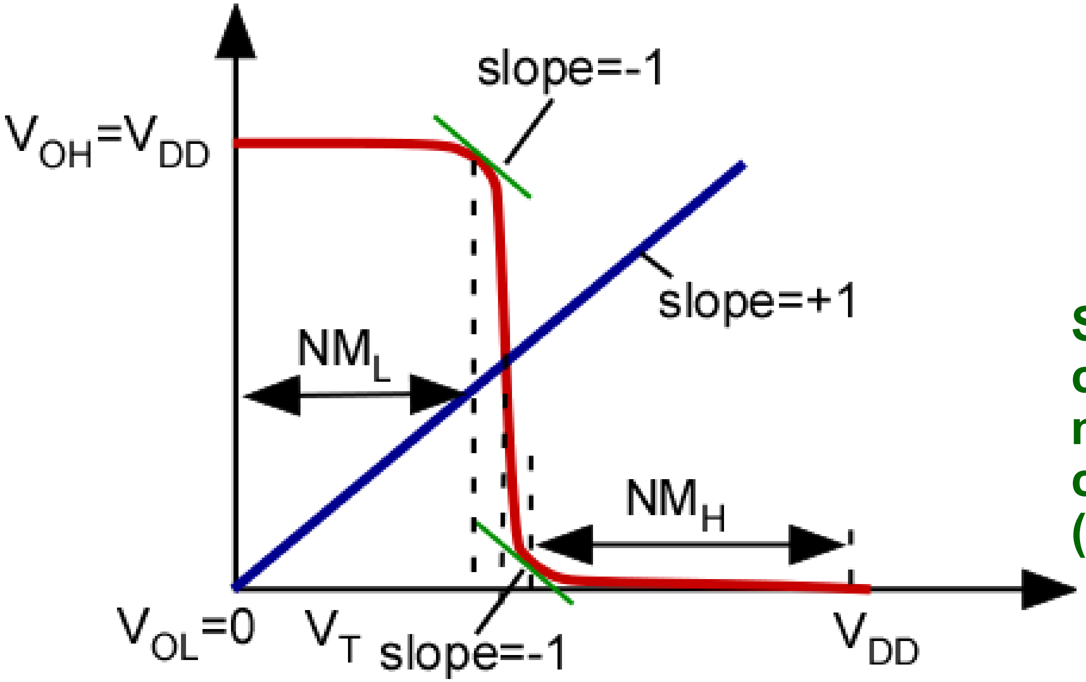
Advantages of CMOS inverter

- Output voltage levels are 0 and V_{DD} ➔ signal swing is maximum possible
- Static power dissipation is zero
- Low resistance paths to V_{DD} and ground when needed
- High output driving capability ➔ increased speed
- Input resistance is infinite ➔ high fan-out

Load driving capability of CMOS is high. Transistors can sink or source large load currents that can be used to charge and discharge load capacitances.

Matched CMOS Inverter VTC

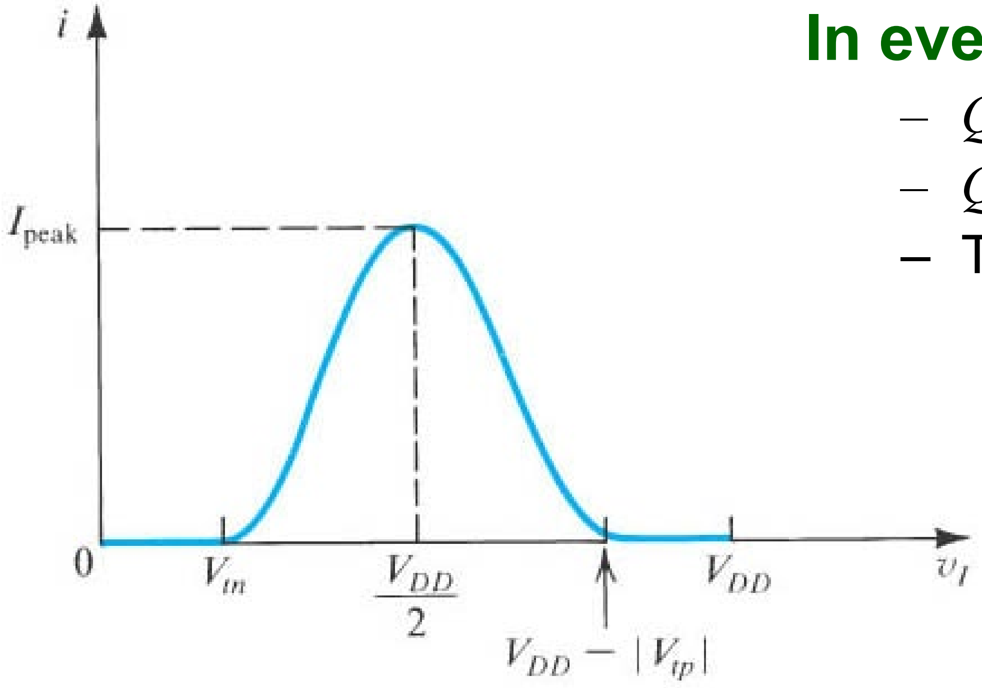
CMOS inverter can be made to switch at specific threshold voltage by appropriately sizing the transistors



$$\left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_n$$

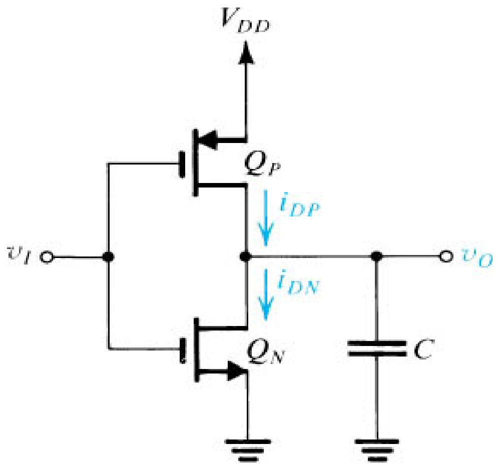
Symmetrical transfer characteristics is obtained via matching ➔ equal current driving capabilities in both directions (pull-up and pull-down)

CMOS – Dynamic Power Dissipation



In every cycle

- Q_N dissipate ½ CV_{DD}^2 of energy
- Q_P dissipate ½ CV_{DD}^2 of energy
- Total energy dissipation is CV_{DD}^2



(a)

If inverter is switched at *f* cycles per second, dynamic power dissipation is: $P_D = fCV_{DD}^2$

Digital Logic - Generalization

De Morgan's Law

$$\overline{A+B+C+\ldots}=\bar{A}\cdot\bar{B}\cdot\bar{C}\cdot\ldots$$

$$\overline{A\cdot B\cdot C\cdot\ldots}=\bar{A}+\bar{B}+\bar{C}+\ldots$$

Distributive Law

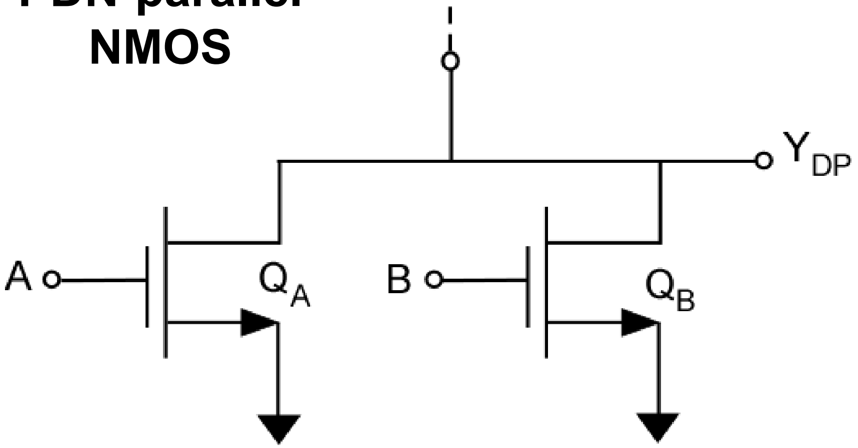
$$AB+AC+BC+BD=A(B+C)+B(C+D)$$

- **General Procedure**

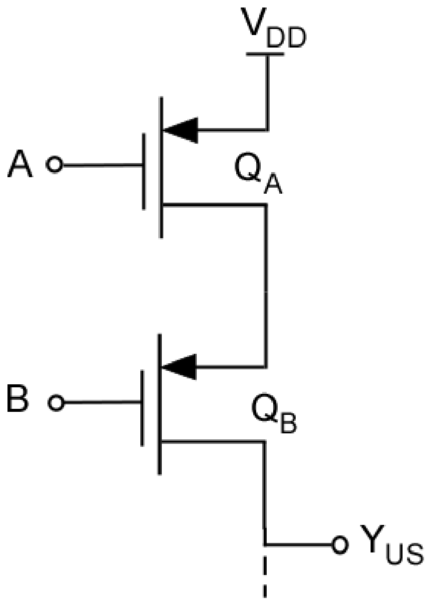
1. Design PDN to satisfy logic function
2. Construct PUN to be complementary of PDN in every way
3. Optimize using distributive rule

Pull-Down and Pull-Up

PDN-parallel NMOS



PUN-series PMOS



Truth Tables

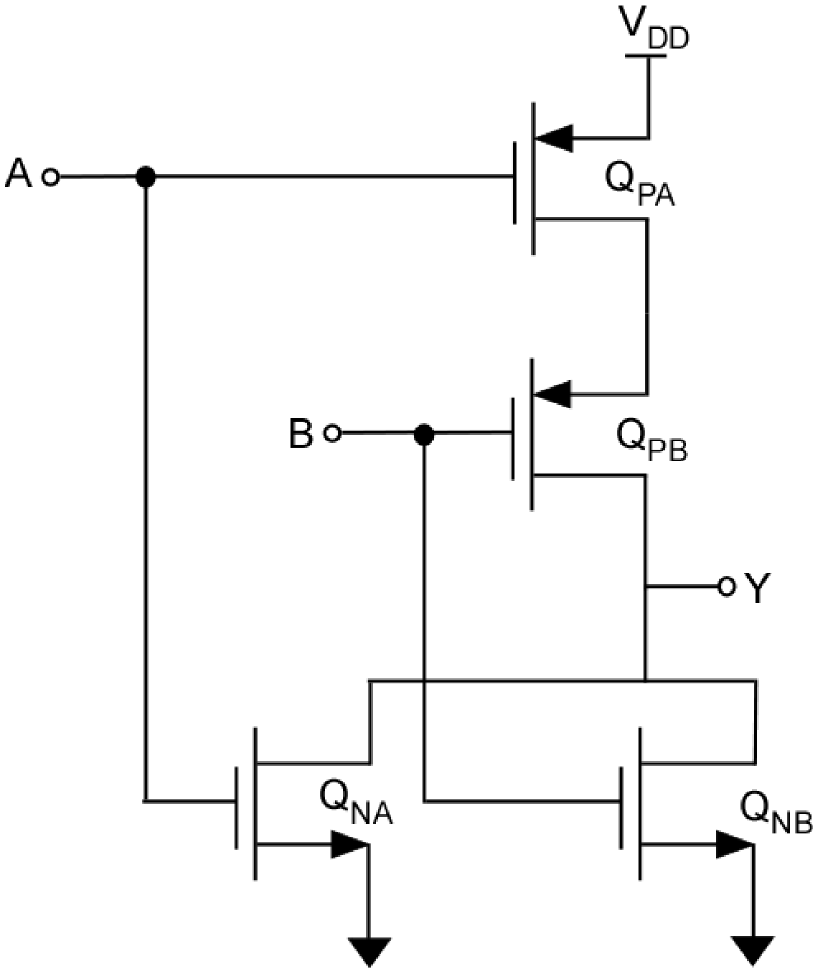
$$Y_{DP} = \overline{A+B}$$

	A	B	Y_{DP}
	0	0	1
	0	1	0
	1	0	0
	1	1	0

$$Y_{US} = \overline{A}\,\overline{B}$$

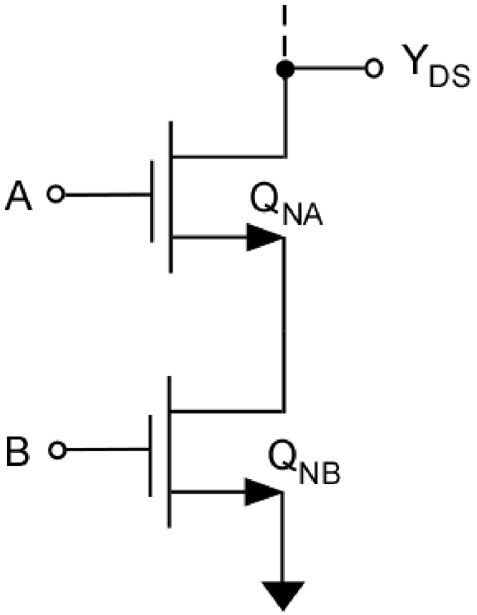
	A	B	Y_{US}
	0	0	1
	0	1	0
	1	0	0
	1	1	0

Two-Input NOR Gate

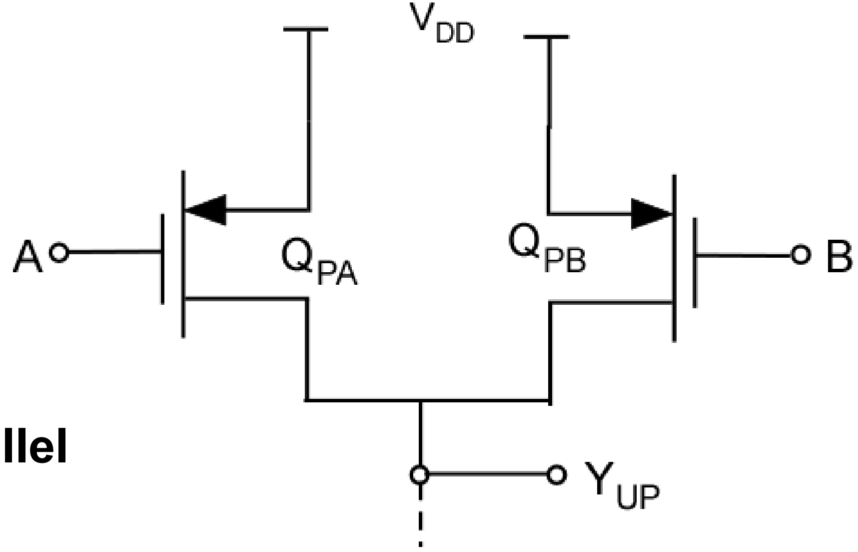


$$Y=\overline{A+B}=\overline{A}\,\overline{B}$$

Pull-Down and Pull-Up



PDN-Series
NMOS



PUN-Parallel
PMOS

Truth Tables

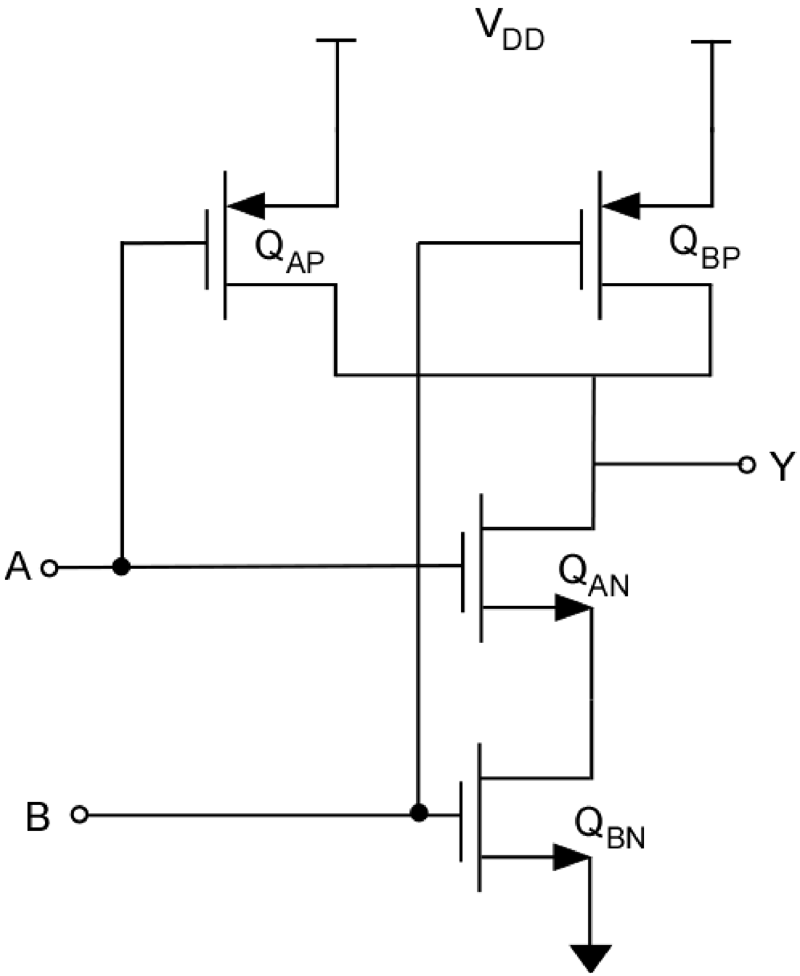
$$Y_{DS} = \overline{AB}$$

	A	B	Y_{DS}
	0	0	1
	0	1	1
	1	0	1
	1	1	0

$$Y_{UP} = \overline{A} + \overline{B}$$

	A	B	Y_{UP}
	0	0	1
	0	1	1
	1	0	1
	1	1	0

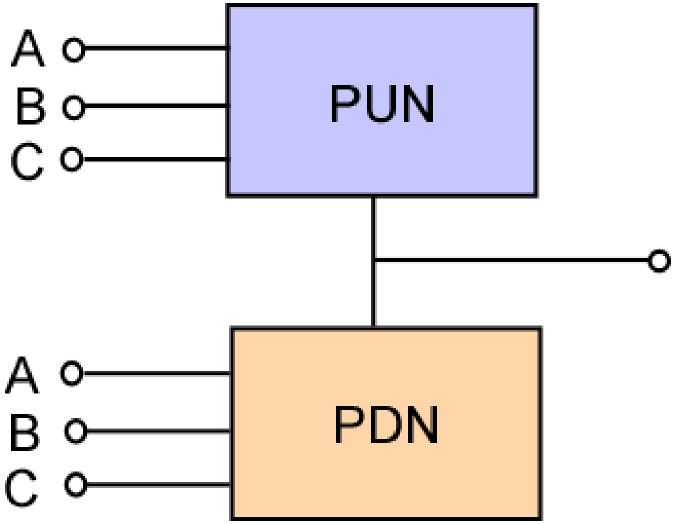
Two-Input NAND Gate



$$Y = \overline{AB} = \overline{A} + \overline{B}$$

CMOS Logic Gate Circuits

- **Two Networks**
  - Pull-down network (PDN) with NMOS
  - Pull-up network (PUN) with PMOS

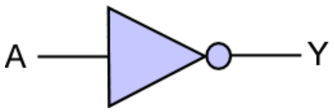
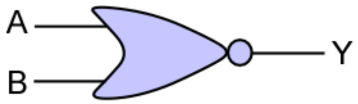
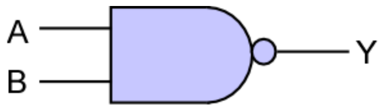


PUN conducts when inputs are low and consists of PMOS transistors

PDN consists of NMOS transistors and is active when inputs are high

- **PDN and PUN utilize devices**
  - In parallel to form OR functions
  - In series to form AND functions

Basic Logic Function

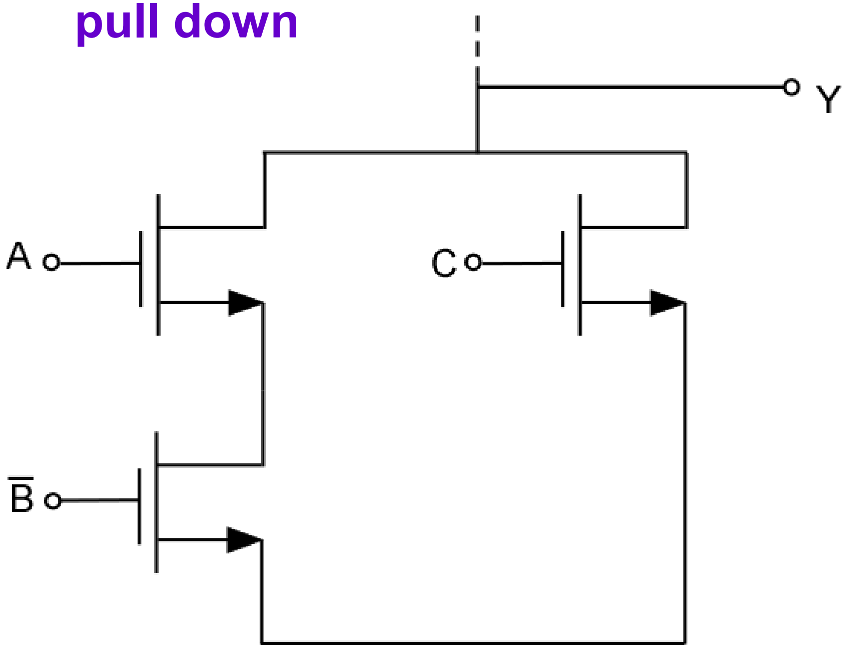
Basic Function	**INVERTER**	**NOR**	**NAND**
Symbol			
# Devices PUN	1 PMOS	2 PMOS-Series	2 PMOS-Parallel
# Devices PDN	1 NMOS	2 NMOS-Parallel	2 NMOS-Series
Truth Table	A Y 0 1 1 0	A B Y 0 0 1 0 1 0 1 0 0 1 1 0	A B Y 0 0 1 0 1 1 1 0 1 1 1 0

Example

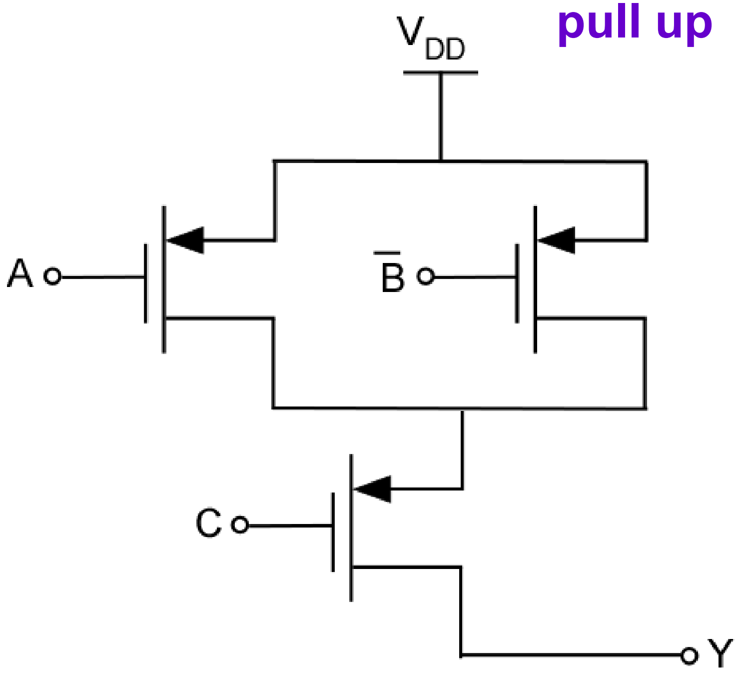
Implement the function

$$\overline{Y} = A\overline{B} + C$$

pull down



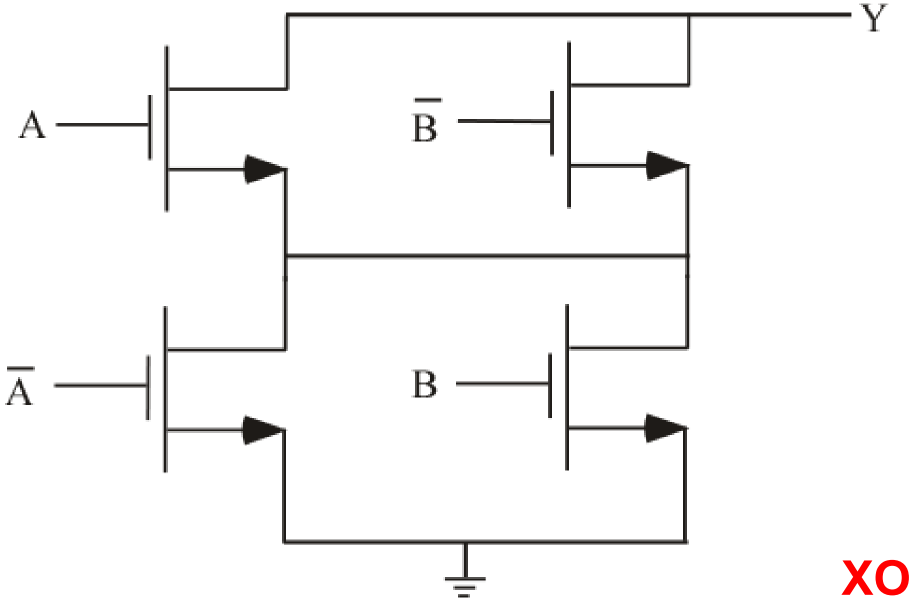
pull up

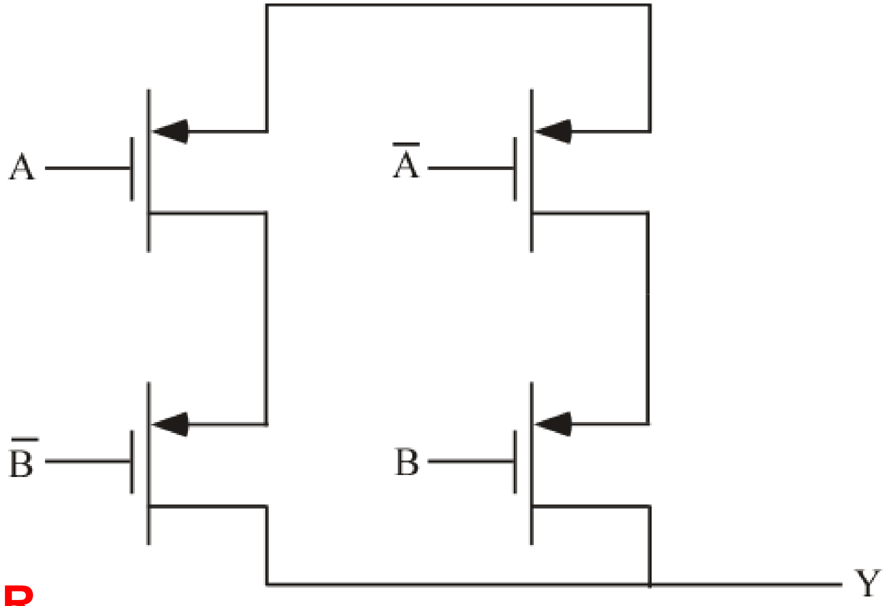


$$Y = \overline{A\overline{B} + C} = \overline{A\overline{B}} \cdot \overline{C} = (\overline{A} + B) \cdot \overline{C}$$

Exclusive-OR (XOR) Function

$$Y = A\overline{B} + \overline{A}B \qquad \overline{Y} = (\overline{A} + B)(A + \overline{B})$$





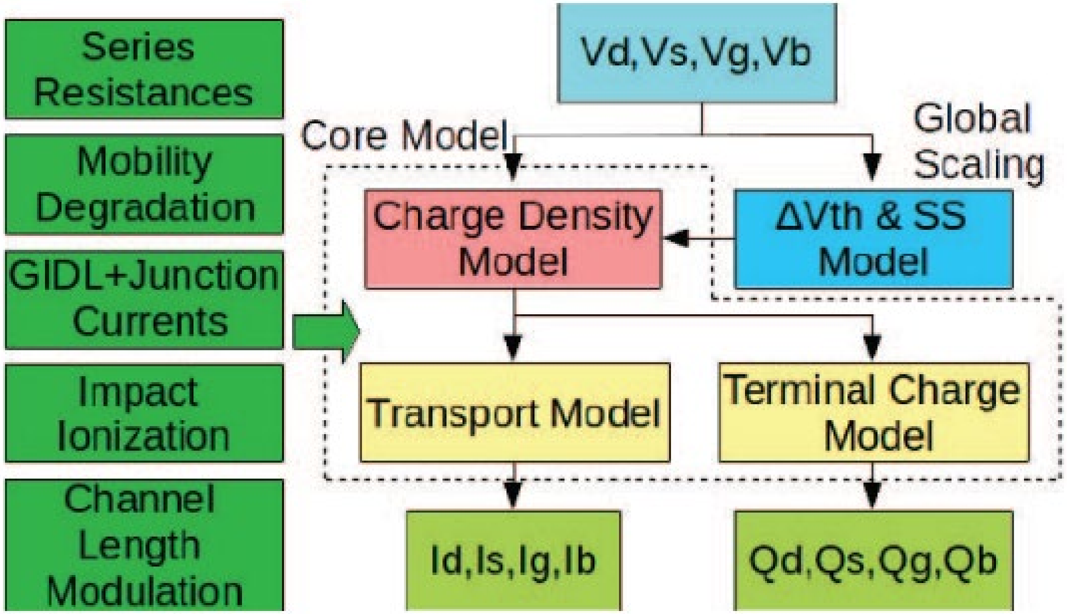
pull down

XOR

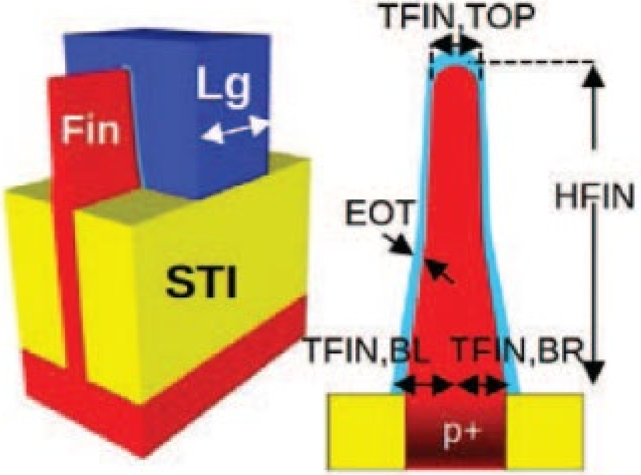
	A	B	Y
	0	0	0
	0	1	1
	1	0	1
	1	1	0

pull up

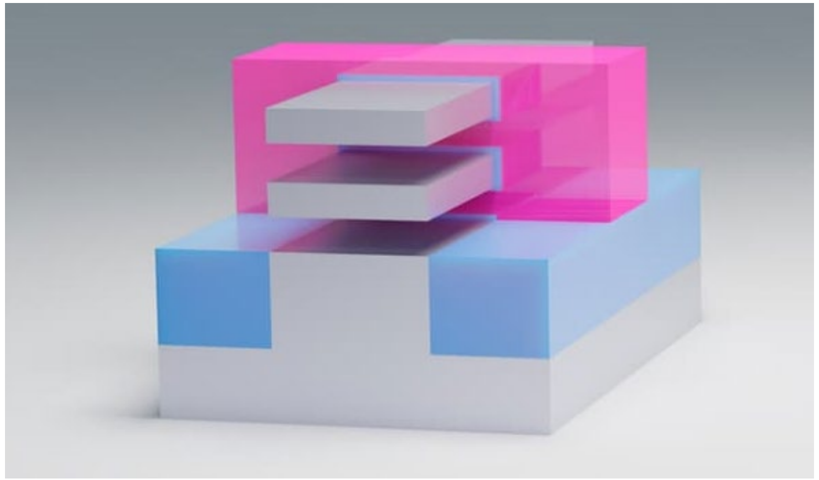
FinFet Technology



FinFET Transistor



Nanosheet Transistor



MOS Technologies

Parameter	0.8 μm NMOS	0.8 μm PMOS	0.5 μm NMOS	0.5 μm PMOS	0.25 μm NMOS	0.25 μm PMOS	0.18 μm NMOS	0.18 μm PMOS	0.13 μm NMOS	0.13 μm PMOS	65 nm NMOS	65 nm PMOS	28 nm NMOS	28 nm PMOS
t_{ox} (nm)	15	15	9	9	6	6	4	4	2.7	2.7	1.4	1.4	1.4	1.4
C_{ox}(fF/μm²)	2.3	2.3	3.8	3.8	5.8	5.8	8.6	8.6	12.8	12.8	25	25	34	34
μ(cm²/V.s)	550	250	500	180	460	160	450	100	400	100	216	40	220	200
μC_{ox}(μA/V²)	127	58	190	68	267	93	387	86	511	128	540	100	750	680
V_{to}(V)	0.7	-0.7	0.7	-0.8	0.5	-0.6	0.5	-0.5	0.4	-0.4	0.35	-0.35	0.3	-0.3
V_{DD}(V)	5	5	3.3	3.3	2.5	2.5	1.8	1.8	1.3	1.3	1	1	0.9	0.9
$\|V_A\|$(V/μm)	25	20	20	10	5	6	5	6	5	6	3	3	1.5	1.5
C_{ov}(fF/μm)	0.2	0.2	0.4	0.4	0.3	0.3	0.37	0.33	0.36	0.33	0.33	0.31	0.4	0.4