# ECE 546
# Lecture 12
# Integrated Circuits

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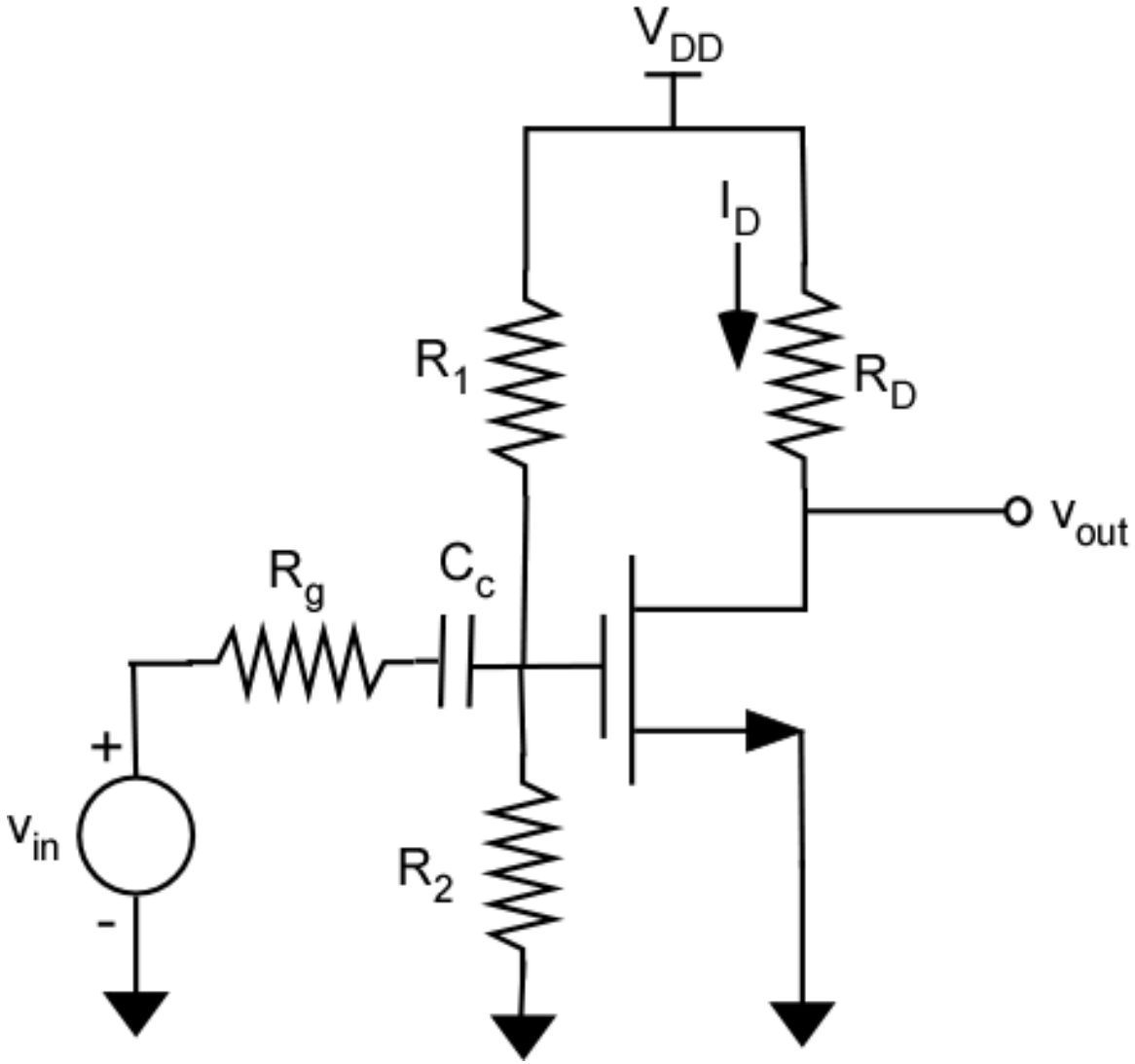
# Integrated Circuits

- **IC Requirements**
  - Biasing of ICs is based on the use of constant current sources
  - Use current mirrors
  - Source circuits are used as loads

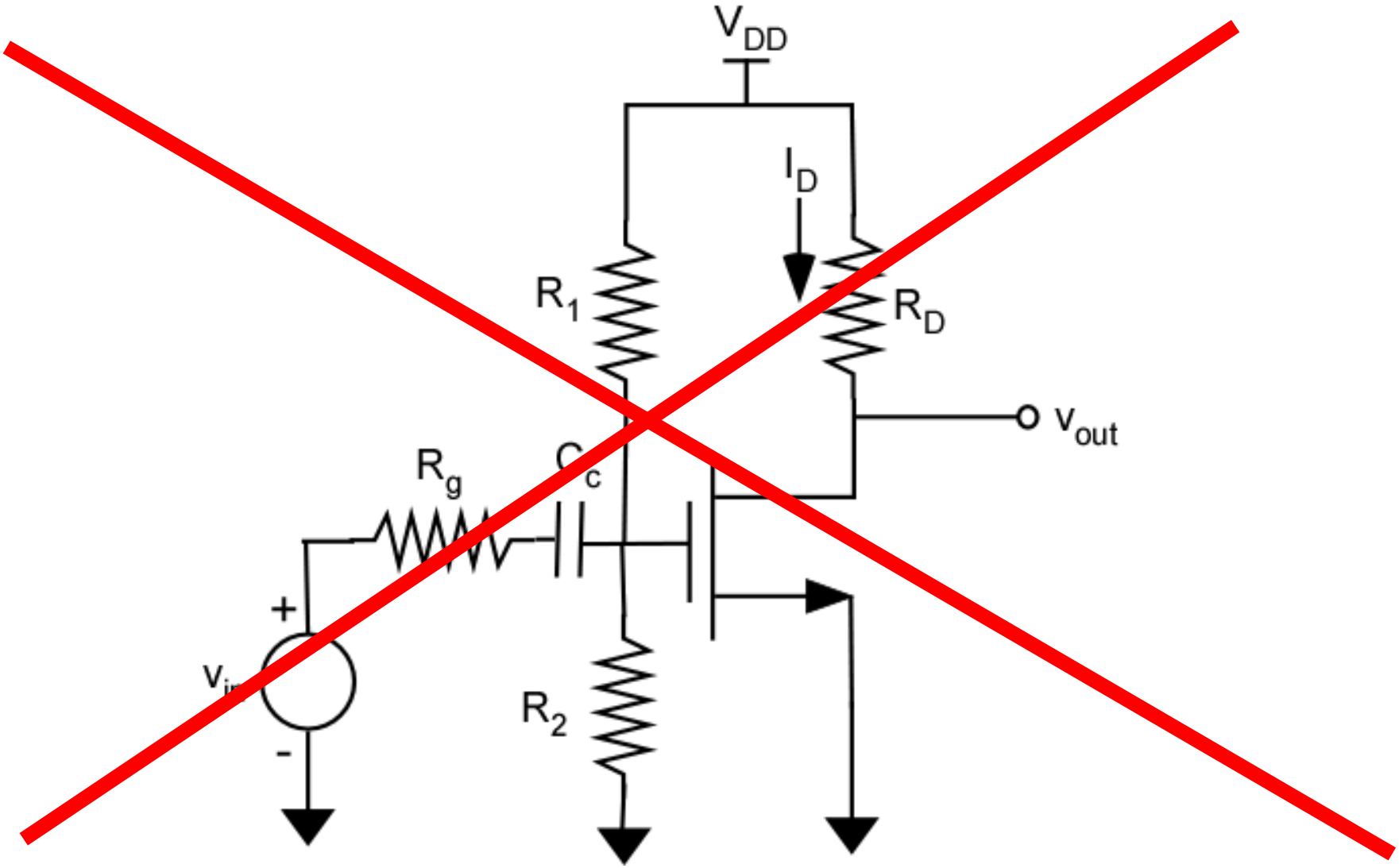
# Integrated Circuits

- **Analog Design Requirements**
  - Analog ICs may need resistors and capacitors for the design of amplifiers
  - Resistors and capacitors occupy the space of tens or hundreds of MOS devices
  - It is important to minimize their use

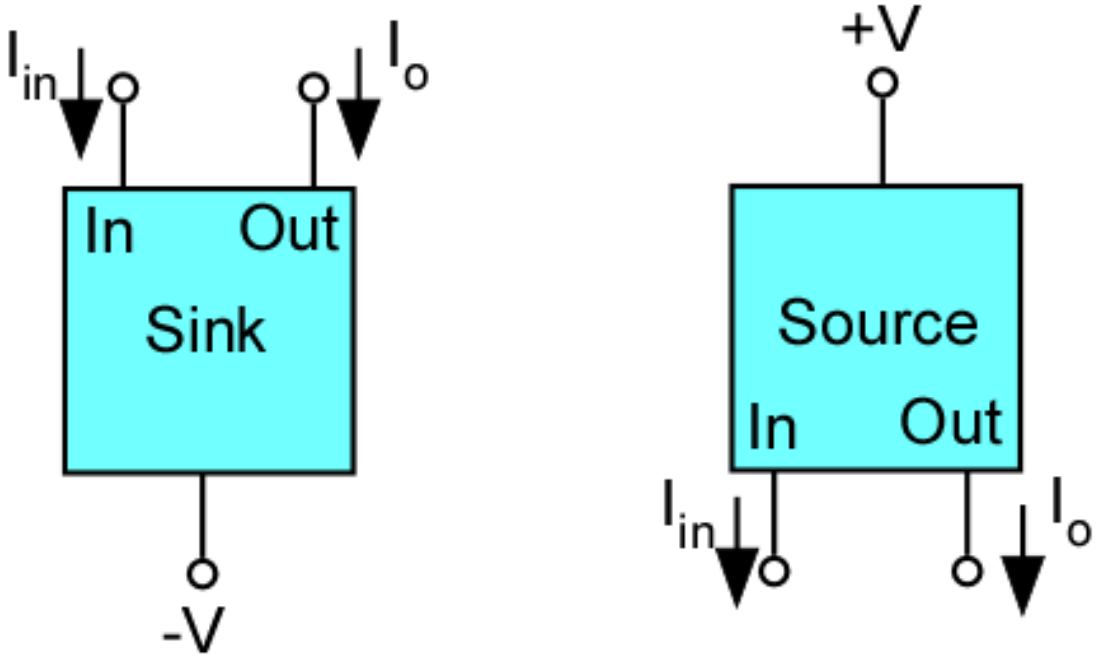
# Transistor Biasing



# Transistor Biasing

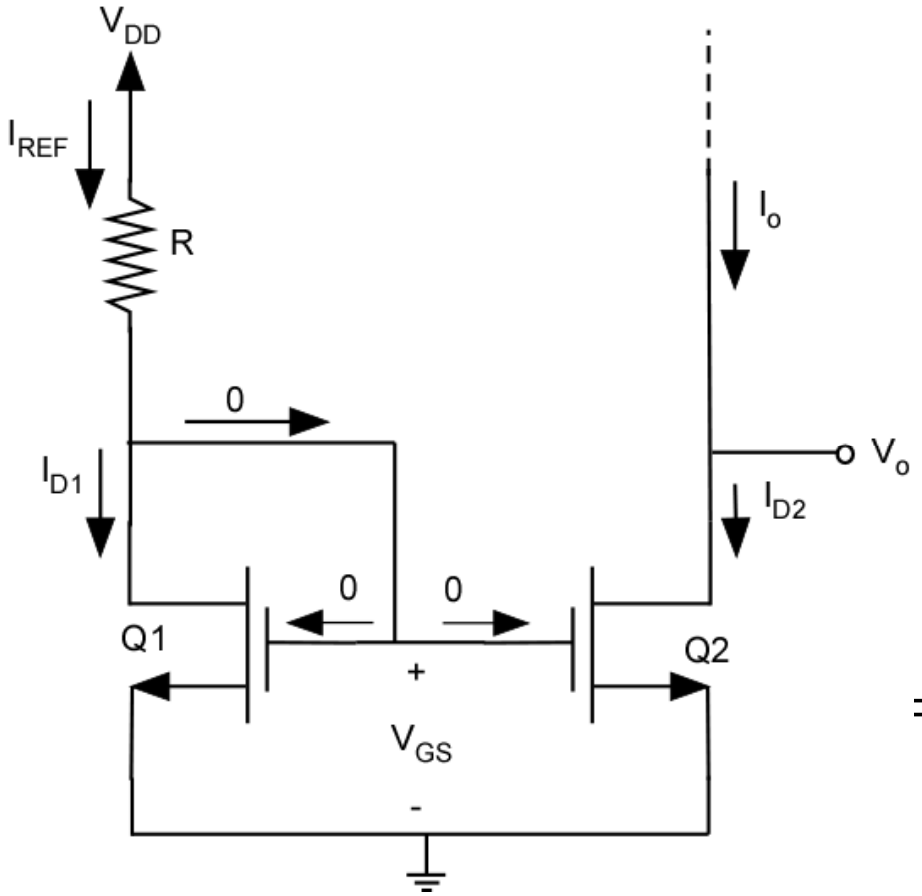


# Current Mirrors




A current mirror will reproduce a reference current to the output while allowing the output voltage to assume any value within a specified range. $I_o=KI_{in}$ where $K$ is a factor that can be less than or equal or greater than 1

# MOS Current Mirror




$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 \left(V_{GS} - V_{Tn}\right)^2$$

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

$$= I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 \left(V_{GS} - V_{Tn}\right)^2$$

**R is usually external to IC**

# MOS Current Mirror

**Assuming that the transistors are using the same process**

$$\frac{I_o}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} = \frac{W_2 L_1}{W_1 L_2}$$

- **Can be limited by**
  - Channel length modulation (λ)
  - Threshold voltage mismatch
  - Imperfect geometrical matching

# MOS Current Mirror

$$\frac{I_o}{I_{REF}} = \frac{W_2 L_1}{W_1 L_2}\left[\frac{1+\lambda\left(V_{DS2}-V_{DSP2}\right)}{1+\lambda\left(V_{DS1}-V_{DSP1}\right)}\right]$$

- **Some Properties**
  1. MOS current mirrors draw zero control current➔better than BJT's
  2. Matching of threshold voltages harder than in BJT's

# Example

A matched pair of MOSFETs are used in a current mirror witl $\lambda$ = 0.032 $V^{-1}$, $\mu C_{ox}$=70 μA/$V^2$, $W/2L$ =10, and $V_T$ = 0.9 V. Find the value of $R$ to create an input current of 100 μA. Calculate the output current when $V_o$ = 3 V.

Use drain current equation in active region to calculate

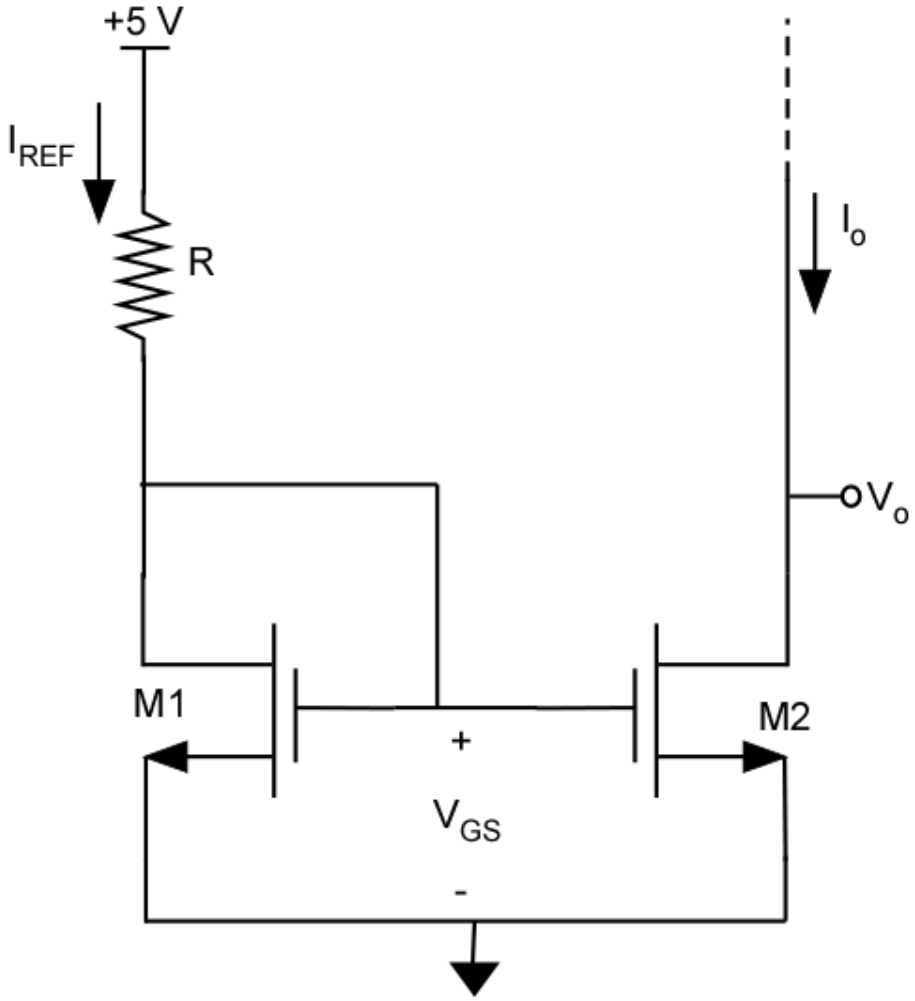
$$I_{D1} = \frac{\mu C_{ox} W}{2L}\left[V_{GS} - V_T\right]^2\left(1 + \lambda V_{DS1}\right)$$

$$I_{D1} = 100 = 700\left[V_{GS} - 0.9\right]^2\left(1 + 0.032 * V_{GS}\right)$$

We can now solve for the value of $V_{GS}$

# Example

## *MOS Current Mirror*



# Example

$$V_{GS} = 1.272 \text{ V}$$

The resistance needed is:

$$R = \frac{5 - V_{DS1}}{I_{D1}} = \frac{5 - 1.272}{0.1} = 37.2\ k\Omega$$

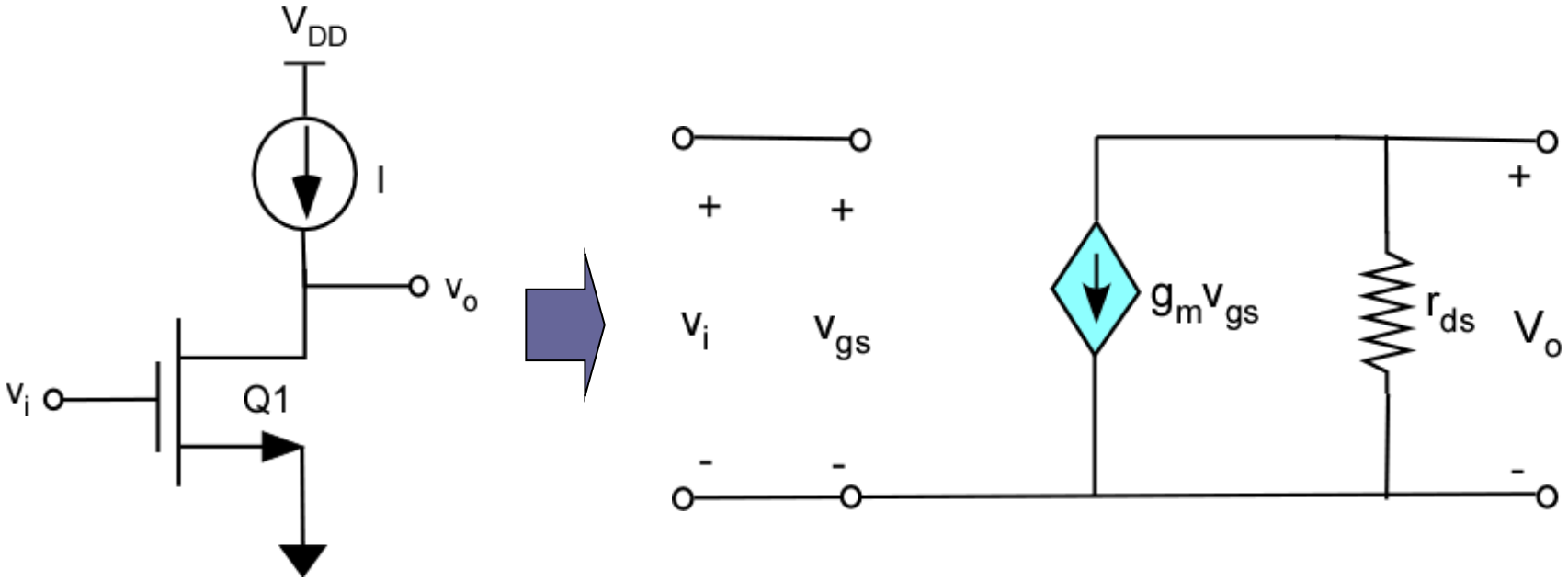
The output current is calculated from:

$$I_{D2} = \frac{\mu C_{ox} W}{2L}\left[V_{GS} - V_T\right]^2 \left(1 + \lambda V_{DS1}\right)$$

$$I_{D2} = 700\left[1.272 - 0.9\right]^2 \left(1 + 0.032 \times 3\right) = 106\ \mu A$$

$$I_{D2} = 106\ \mu A$$

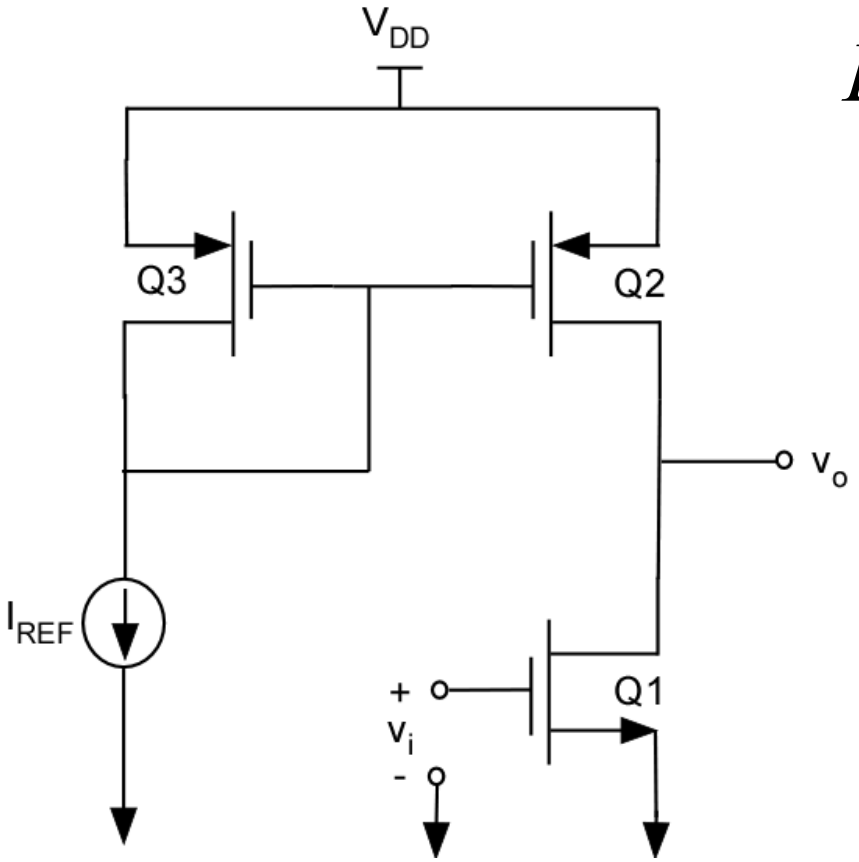
# Ideal MOS Common Source CKT




$$R_i = \infty, \quad A_{vo} = -g_m r_{ds}, \quad R_o = r_{ds}$$

*Intrinsic gain is* $g_m r_{ds}$

# PMOS Implementation of Active Load




$$Let\ r_{ds1} = r_{o1}\ for\ Q_1$$

$$r_{ds2} = r_{o2}\ for\ Q_2$$

$$then,\ R_{out} = r_{o1} \| r_{o2}$$

$$A_{MB} = -g_{m1} R_{out}$$

$$Let\ g_{o1} = \frac{1}{r_{o1}} = g_{ds1}$$

$$g_{o2} = \frac{1}{r_{o2}} = g_{ds2}$$

# PMOS Implementation of Active Load

Can show that the 3dB point is given:

$$f_{2o} = \frac{\left(g_{01} + g_{02}\right)}{2\pi\left(C_{db1} + C_{db2} + C_{gd1} + C_{gd2}\right)}$$

**Large incremental load leads to high gain while maintaining acceptable DC current (resistor would not work)**