ECE 546
Lecture -18
IBIS

Spring 2024

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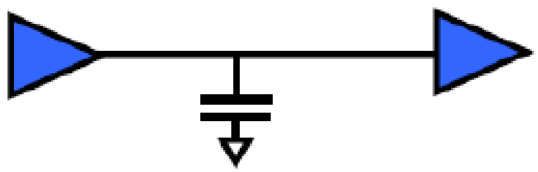
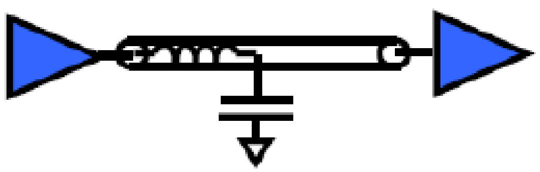
Inter-IC Communication Trends

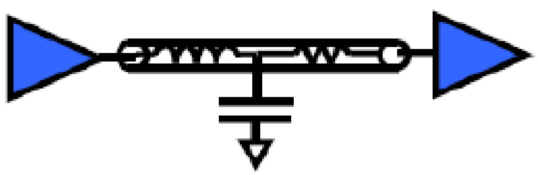
Lumped capacitance

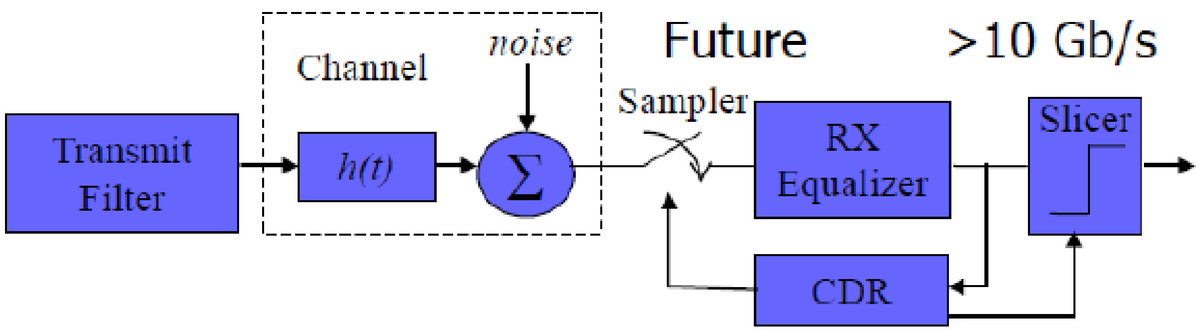


Transmission line



Lossy transmission line



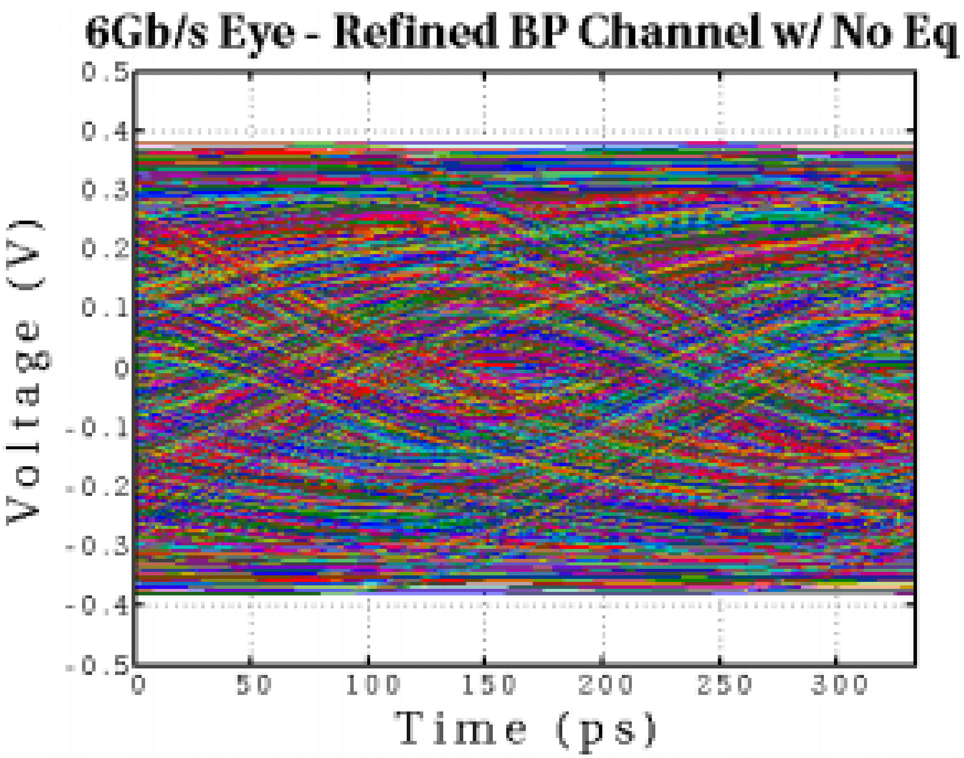


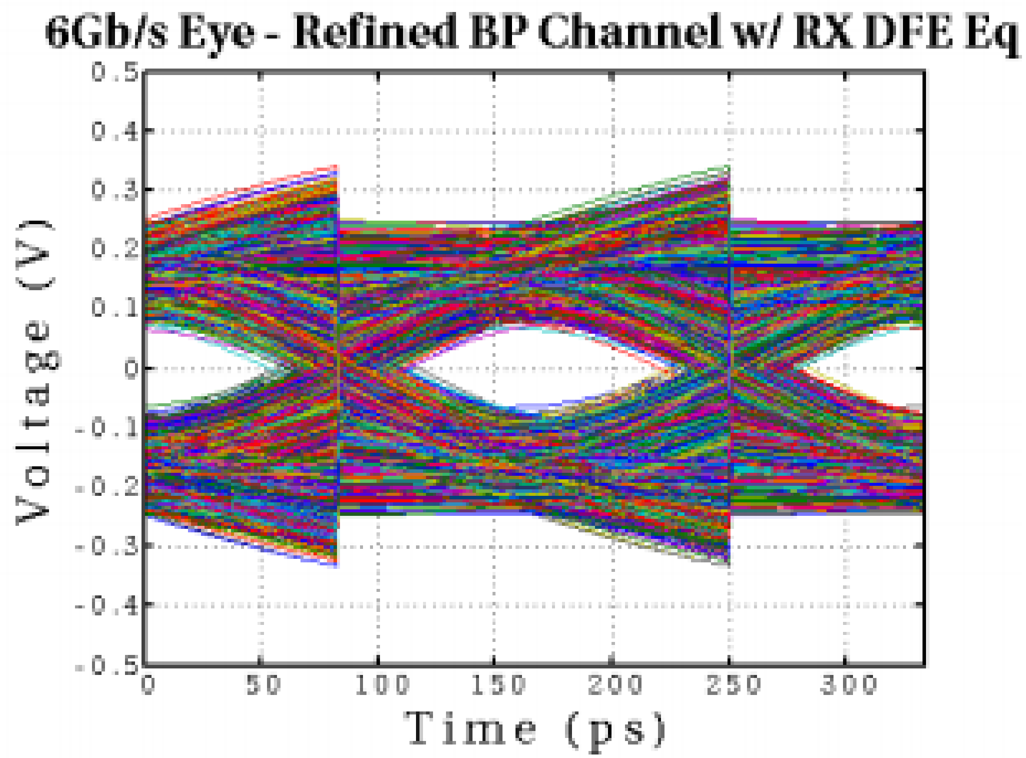
Decade	Speeds	Transceiver Features
1980's	>10Mb/s	Inverter out, inverter in
1990's	>100Mb/s	Termination Source-synchronous clk.
2000's	>1 Gb/s	Pt-to-pt serial streams Pre-emphasis equalization
Future	>10 Gb/s	Adaptive Equalization, Advanced low power clk. Alternate channel materials

Slide Courtesy of Frank O'Mahony & Brian Casper, Intel

DFE Challenge

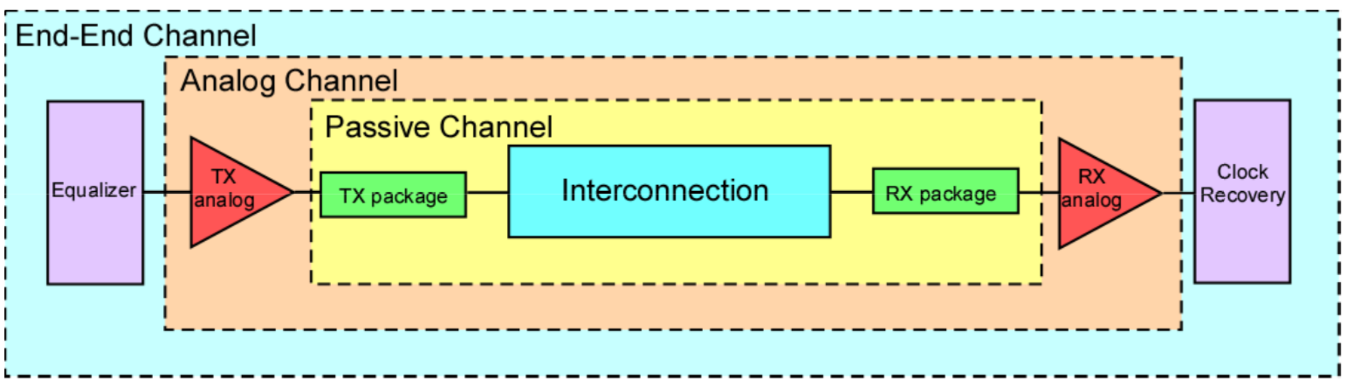
- DDR5 will introduce DFE
- DDR5 memory systems will operate near closed eye at input of DRAM
- Designers need to have control over equalization on both DRAM and memory controller





Serial Channel Characterization

- Serial channels can be characterized using S Parameter data and/or other passive interconnect models
- Millions of bits of behavior are needed to adequately characterize serial links➔ long simulation times
- SERDES transmitters / receivers can be modeled as a combination of analog & algorithmic elements
- DDR5 is upsetting status quo for simulation



IBIS

- I/O Buffer Information Specification is a Behavioral method of modeling I/O buffers based on IV curve data obtained from measurements or circuit simulation.

- The IBIS format is standardized and can be parsed to create the equivalent circuit information needed to represent the behavior of an IC.

- Can be integrated within a circuit simulator using an IBIS translator.

Industry Standard: IBIS

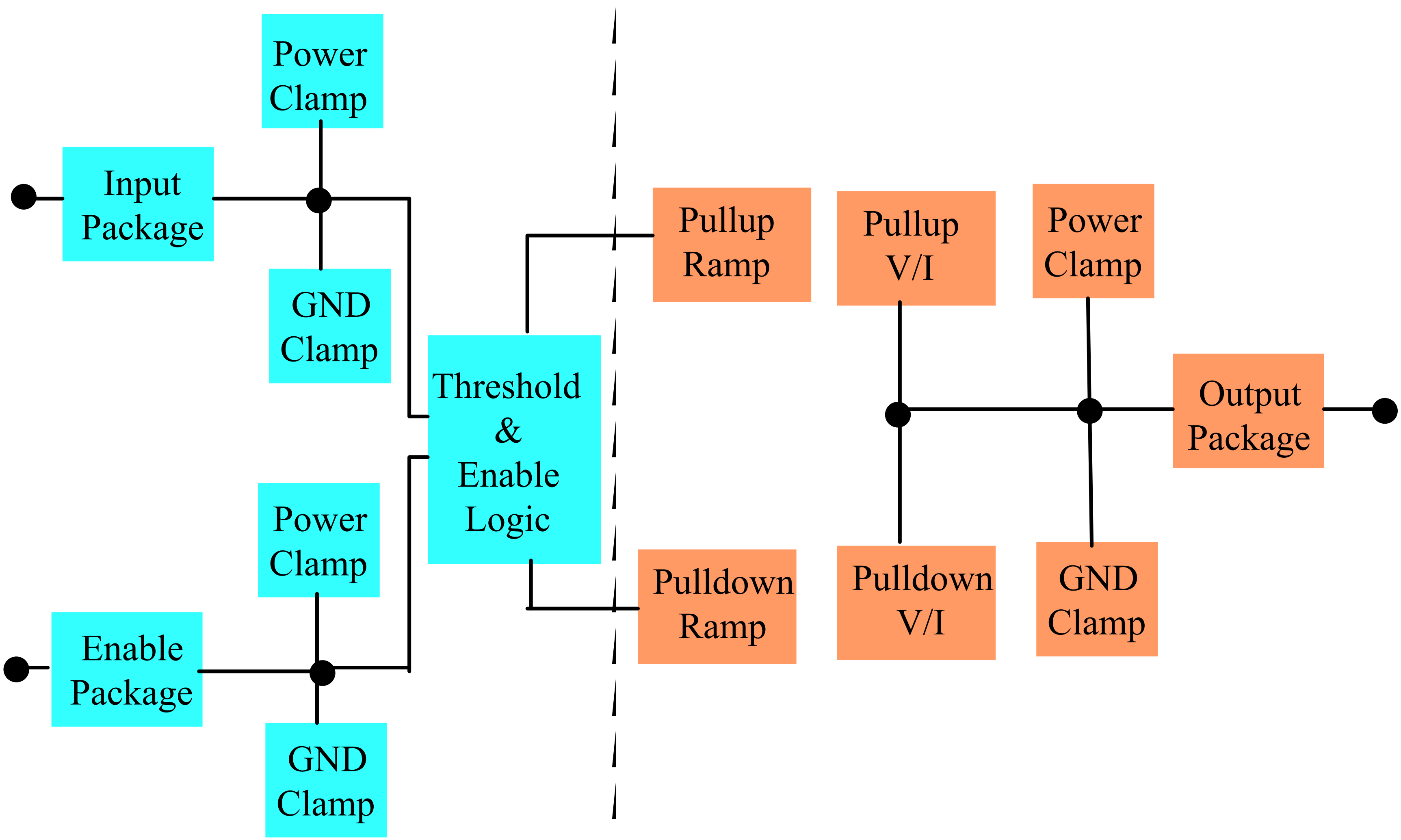
- Provided as binary code
- Fast, efficient execution
- Protects vendor IP
- Extensible modeling capability
- Allows models to be developed in multiple languages
- Standardized execution interface
- Standardized control (.AMI) file

IBIS homepage: **http://www.eigroup.org/ibis/**

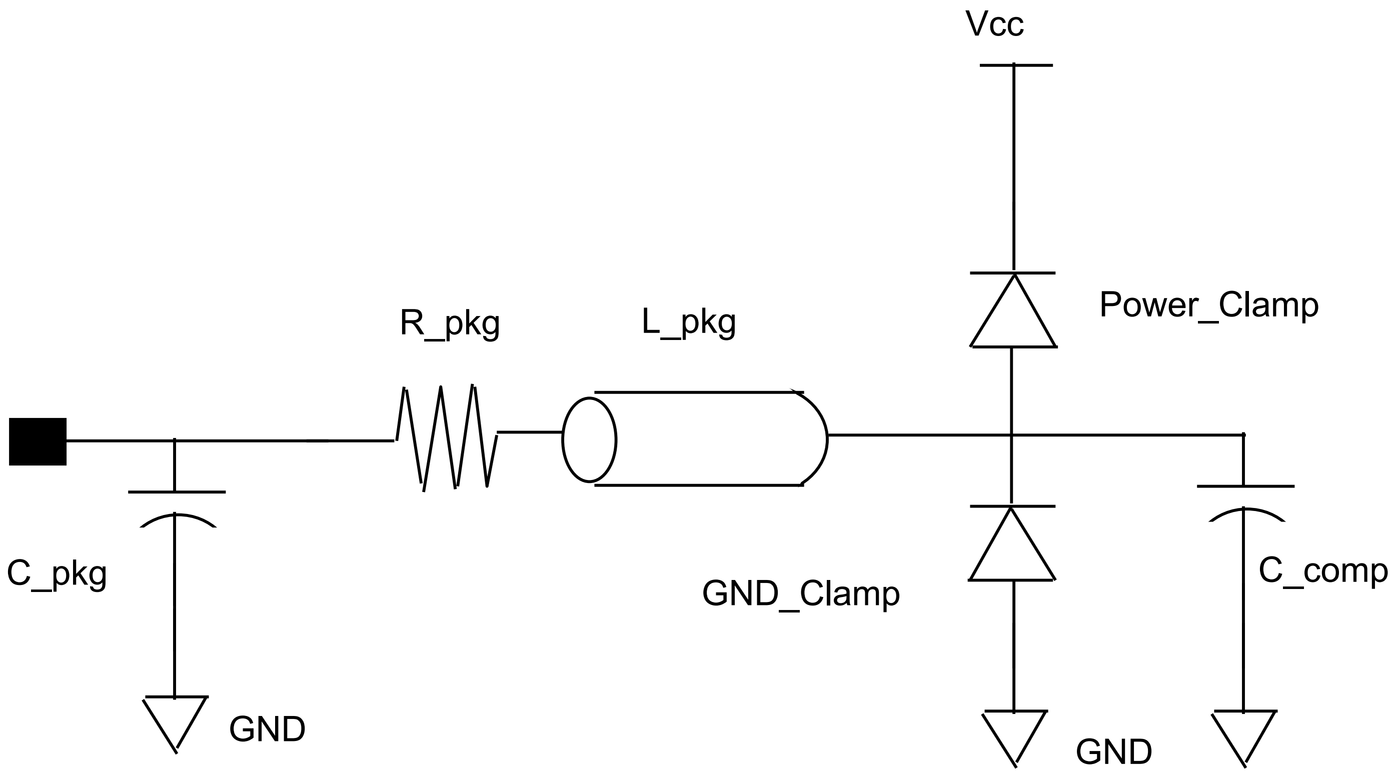
Advantage of IBIS

- Protection of proprietary information
- Adequate for signal integrity simulation
- Models are free from vendors
- Faster simulations (with acceptable accuracy)
- Standardized topology

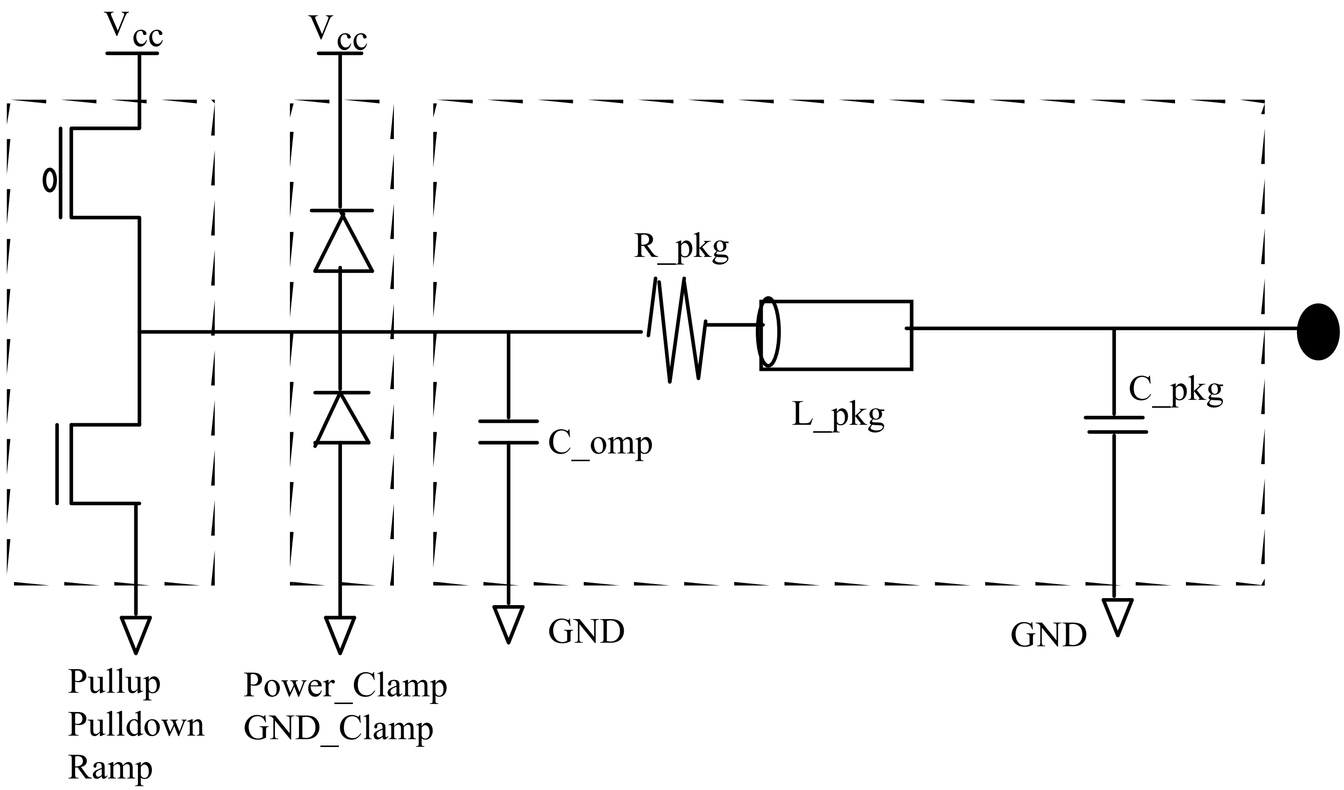
IBIS Diagram



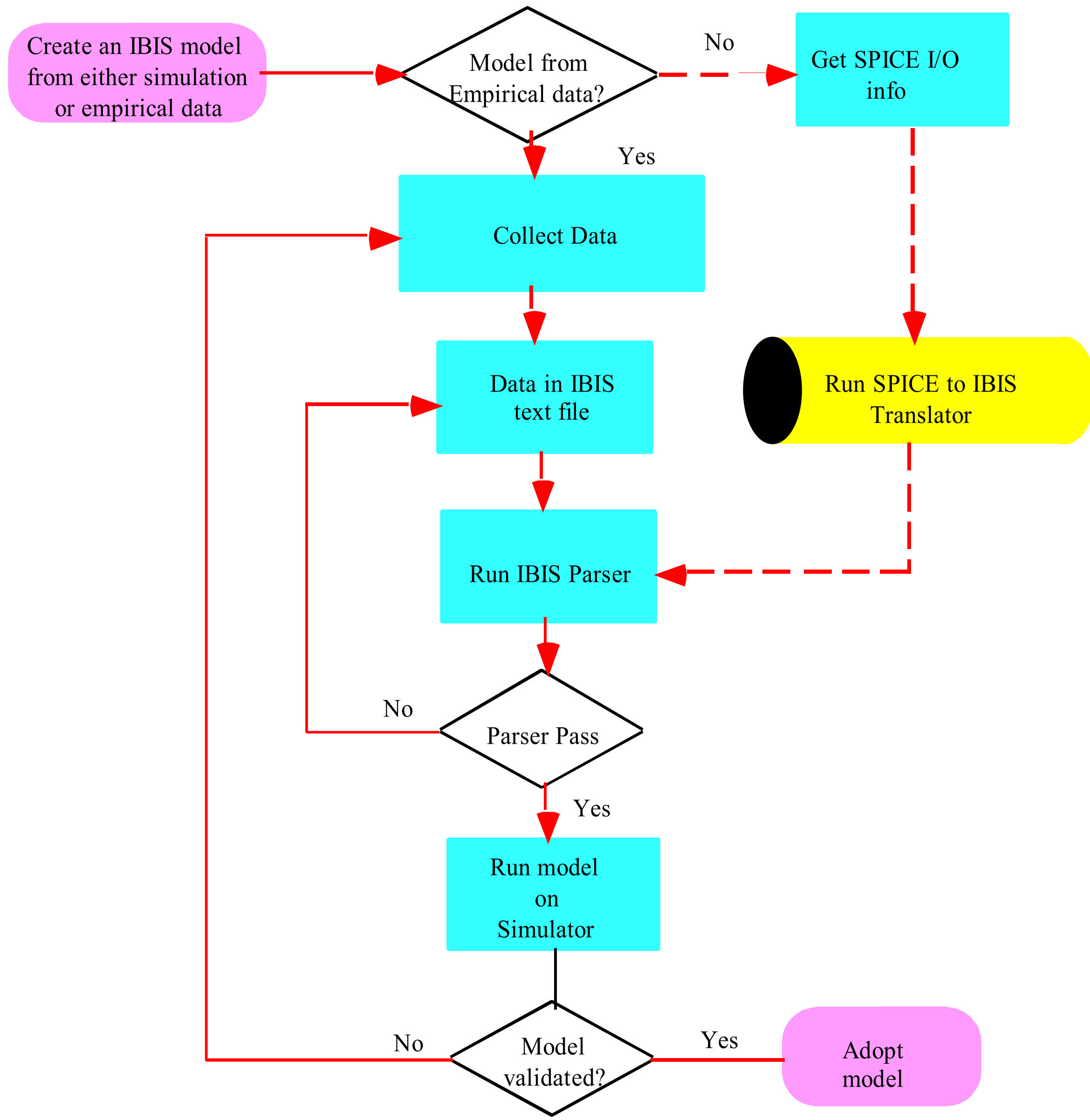
IBIS Input Topology



IBIS Input Topology

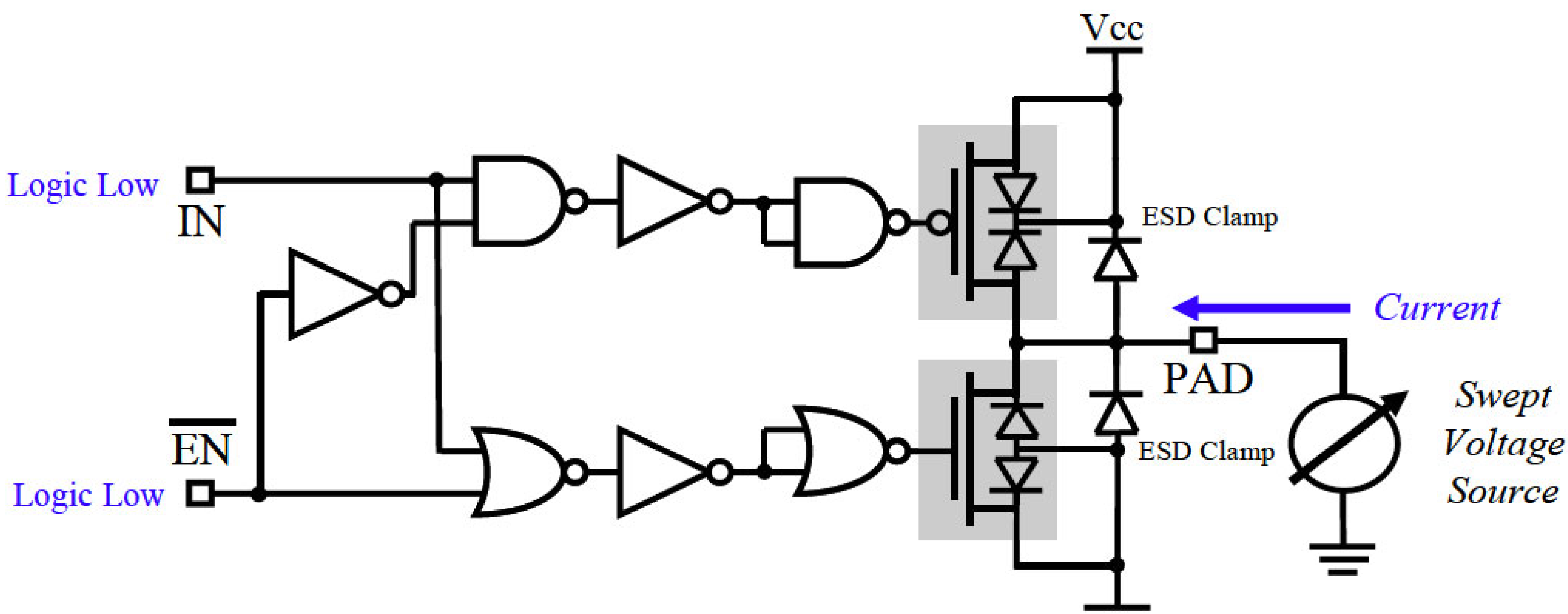


IBIS Model Generation



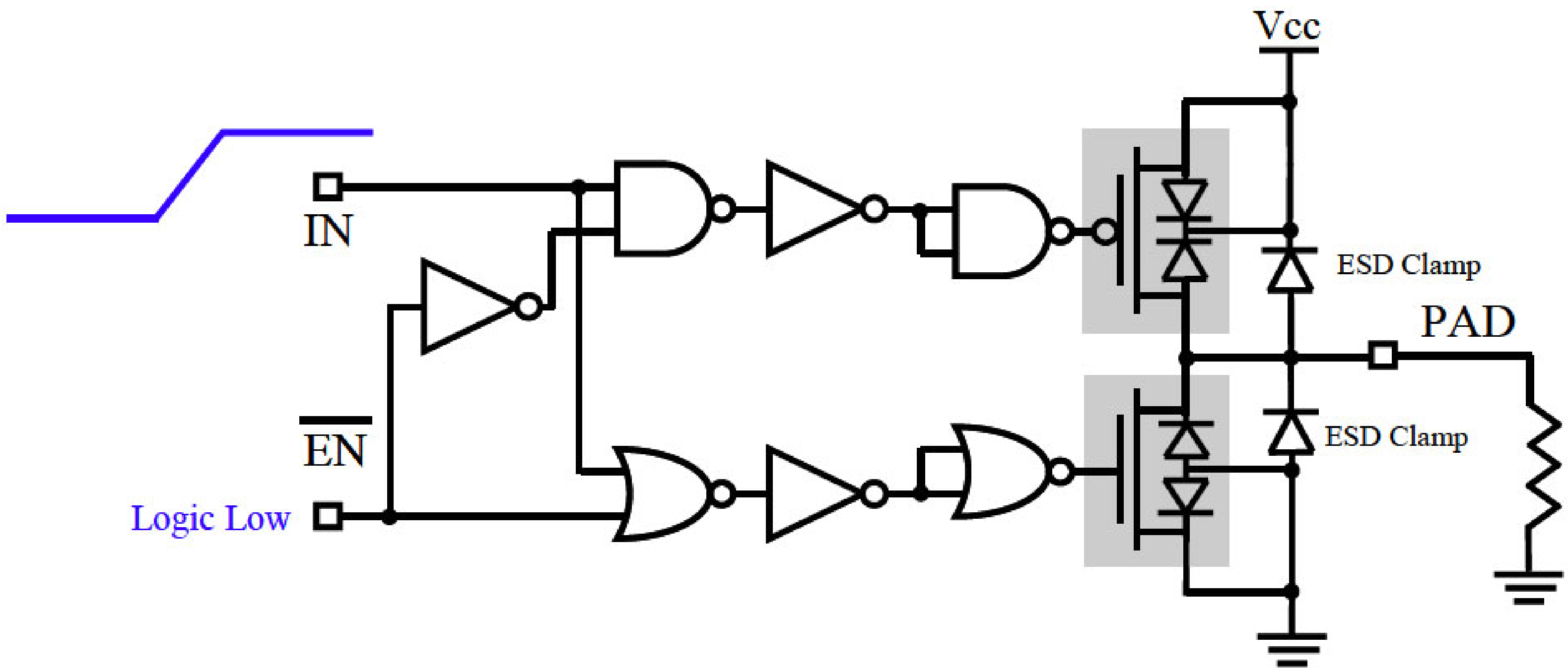
IBIS Model

Static data



IBIS Model

Dynamic data



IBIS VT Waveforms

Technology	# of Waveforms	Load Circuit and Waveform	Notes
Standard Push/Pull – CMOS	4	1R + 1F driving 50 Ω to Vcc 1R + 1F driving 50 Ω to GND	1
Open-drain/collector– CMOS, TTL and GTL	2	1R + 1F into manufacturer's suggested pullup resistor termination and voltage	1, 2
Open-source/emitter – CMOS and TTL	2	1R + 1F into manufacturer's suggested pulldown resistor termination and voltage	1, 2
ECL	2	1R + 1F into manufacturer's suggested pulldown resistor termination and voltage	3

IBIS File

```
|**************************************************************************
|                              Model lvpclpf5_ew
|**************************************************************************
|
[Model]          lvpclpf5_ew
Model_type       I/O
Polarity         Non-Inverting
Enable           Active-High
Vinl =   1.4500V
Vinh =   1.7500V
Vmeas =   1.6000V
|
C_comp          1.737pF          1.396pF          2.077pF
|
|
[Temperature Range]       25.0000            70.0000            0.000
[Voltage Range]           3.3000V            3.0000V            3.6000V
[Pulldown]
| voltage     I(typ)              I(min)              I(max)
|
-3.3000         -62.3070mA         -48.2070mA         -75.0990mA
-3.1000         -62.3070mA         -48.2070mA         -75.0990mA
-2.9000         -62.3070mA         -48.2070mA         -75.0990mA
```

IBIS File

```
|
[Pullup]
| voltage      I(typ)              I(min)              I(max)
|
-3.3000          50.6898mA          38.3720mA          61.1590mA
-3.1000          50.6898mA          38.3720mA          61.1590mA
-2.9000          50.6898mA          38.3720mA          61.1590mA
:
|
[GND_clamp]
| voltage      I(typ)              I(min)              I(max)
|
-3.3000          -7.7650A          -6.8810A          -8.3930A
-3.2000          -7.4070A          -6.5660A          -8.0040A
-3.1000          -7.0490A          -6.2520A          -7.6150A
:
|
[POWER_clamp]
| voltage      I(typ)              I(min)              I(max)
|
-3.3000          1.1410A          1.1150A          1.1710A
-3.2000          1.0910A          1.0670A          1.1200A
-3.1000          1.0420A          1.0190A          1.0690A
:
```

IBIS File

```
[Ramp]
| variable       typ                  min                  max
dV/dt_r 1.7344/9.6534e-11     1.4944/1.4735e-10     1.9469/7.9570e-11
dV/dt_f 1.7528/1.4479e-10     1.5200/2.2995e-10     1.9609/1.2362e-10
R_load = 50.0000
|
[Rising Waveform]
R_fixture = 50.000
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
|
|  time          V(typ)         V(min)         V(max)
|
0.000S        3.587e-04        4.167e-04        3.253e-04
132.000pS        7.977e-05        1.311e-04        2.383e-04
:
[Rising Waveform]
R_fixture = 50.000
V_fixture = 3.300
V_fixture_min = 3.000
V_fixture_max = 3.600
|
|  time          V(typ)         V(min)         V(max)
|
0.000S        4.774e-01        5.704e-01        4.246e-01
43.200pS        4.772e-01        5.701e-01        4.244e-01
```

IBIS File

```
|
[Falling Waveform]
R_fixture = 50.000
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
|
|  time           V(typ)        V(min)        V(max)
|
0.000S        2.808e+00        2.415e+00        3.156e+00
63.000pS        2.809e+00        2.416e+00        3.156e+00
126.000pS        2.808e+00        2.416e+00        3.156e+00
:
|
[Falling Waveform]
R_fixture = 50.000
V_fixture = 3.300
V_fixture_min = 3.000
V_fixture_max = 3.600
|
|  time           V(typ)        V(min)        V(max)
|
0.000S        3.299e+00        2.999e+00        3.599e+00
52.200pS        3.300e+00        2.999e+00        3.600e+00
121.800pS        3.299e+00        2.999e+00        3.599e+00
:
|
| End
```

IBIS Processing

1. Arrange static IV data

2. Pulldown data (current vs voltage) → I_{pd}, m_{pd} points

3. Pullup data (current vs voltage) → I_{pu}, m_{pu} points

4. Ground clamp data (current vs voltage) → I_{gc} , m_{gc} points

5. Power clamp data (current vs voltage) → I_{pc} , m_{pc} points

IBIS Processing

- Next Get VT data. VT data is presented as: Rising waveform:

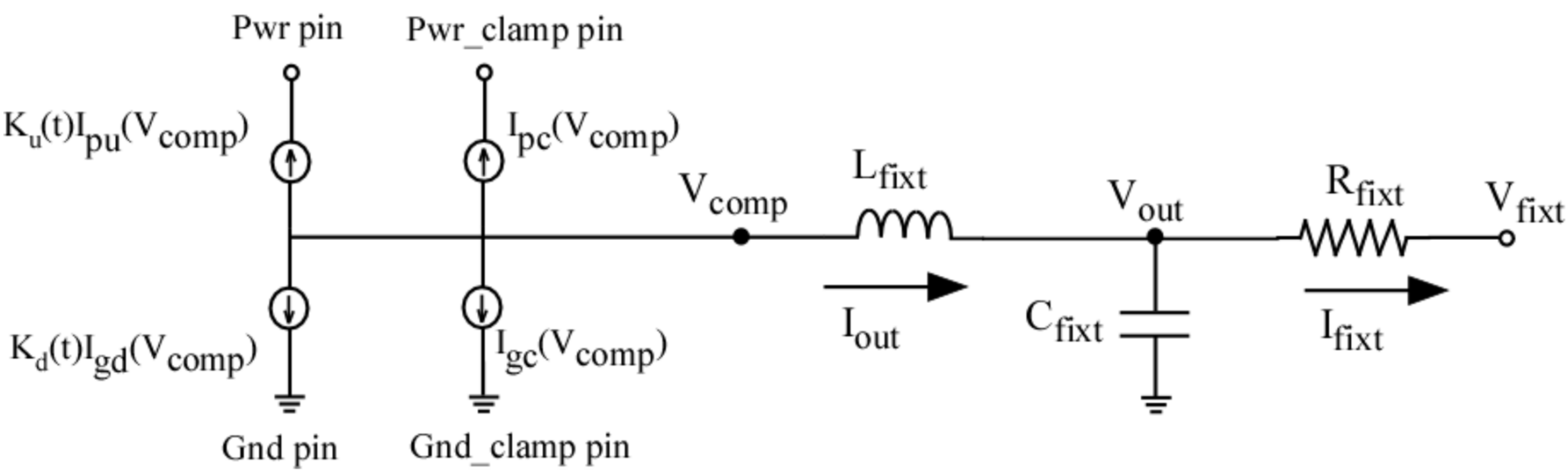
- Voltage versus time for V_{fix} low → V_{R1}, m_{r1} points

- Voltage versus time for V_{fix} high → V_{R2}, m_{r2} points: Falling waveform:

- Voltage versus time for V_{fix} low → V_{F1}, m_{f1} points

- Voltage versus time for V_{fix} high → V_{F2}, m_{f2} points

IBIS Circuit Analysis



$$I_{fixt} = \frac{V_{out} - V_{fixt}}{R_{fixt}}$$

$$I_{cap} = C_{fixt} \frac{V_{out}(t) - V_{out}(t - \Delta t)}{\Delta t}$$

$$V_{comp} = L_{fixt} \frac{\Delta I_{out}}{\Delta t} + V_{out}$$

$$I_{out} = I_{cap} + I_{fixt}$$

IBIS Circuit Analysis

We need to extract K_u and K_d

- Pick value V_{comp1}
- Find closest corresponding currents in static IV data
- Set them as I_{pd1}, I_{pu1}, I_{gc1} and I_{pc1}
- Pick value V_{comp2}
- Find closest corresponding currents in static IV data
- Set them as I_{pd2}, I_{pu2}, I_{gc2} and I_{pc2}

IBIS Circuit Analysis

2 equations, two unknown system

$$-I_{out1} = K_u I_{pu1} + K_d I_{pd1} + I_{pc1} + I_{gc1}$$

$$-I_{out2} = K_u I_{pu2} + K_d I_{pd2} + I_{pc2} + I_{gc2}$$

Rearrange as:

$$K_u I_{pu1} + K_d I_{pd1} = -I_{out1} - I_{pc1} - I_{gc1} = I_{RHS1}$$

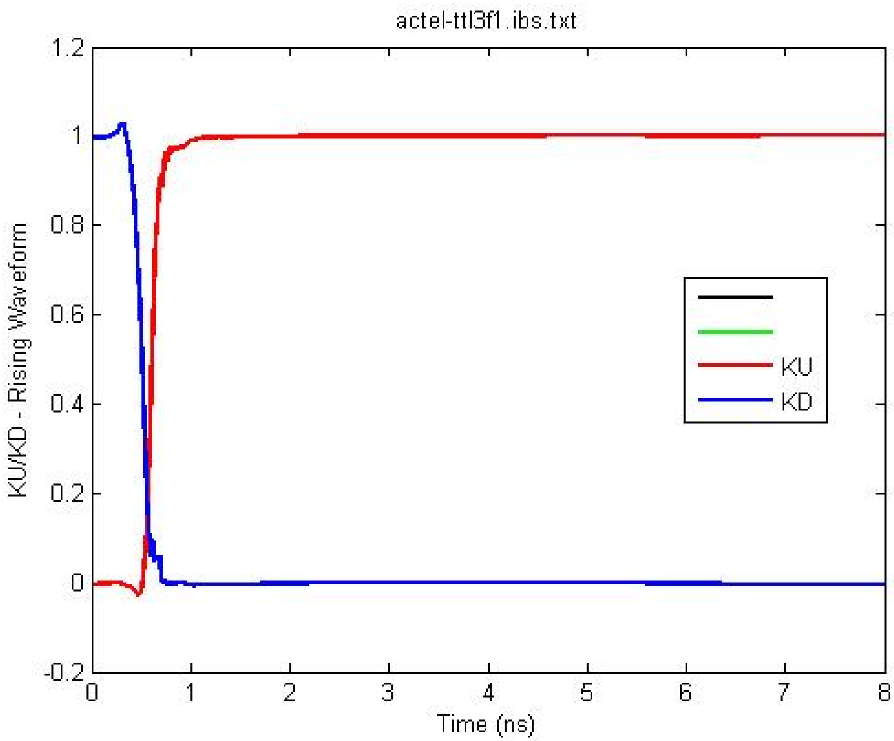
$$K_u I_{pu2} + K_d I_{pd2} = -I_{out2} - I_{pc2} - I_{gc2} = I_{RHS2}$$

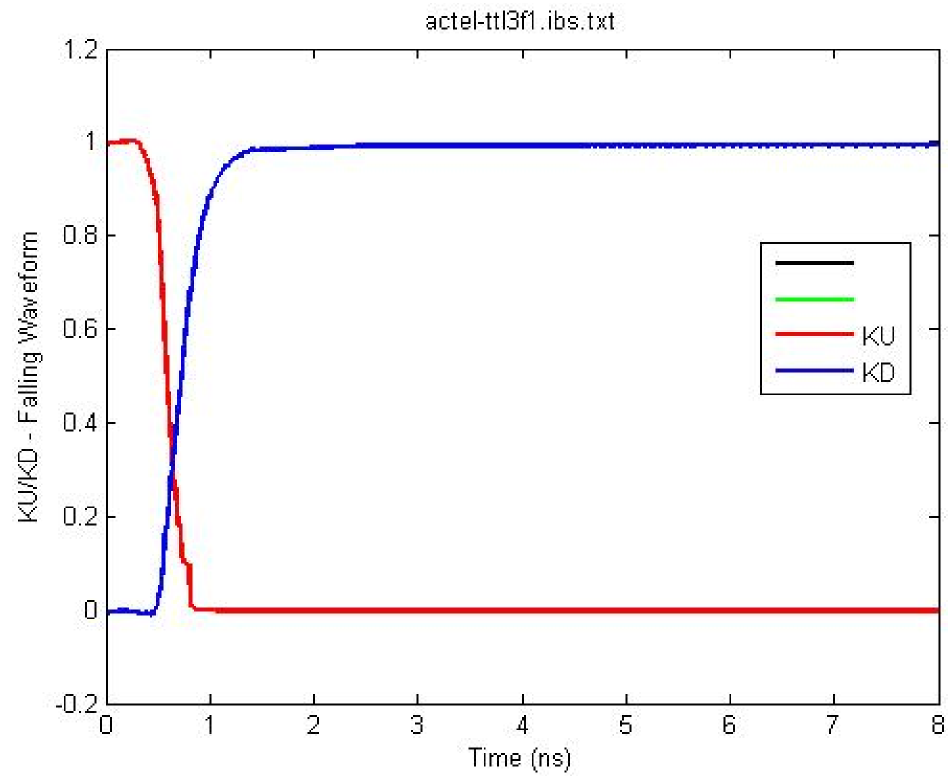
or

$$\begin{bmatrix} I_{pu1} & I_{pd1} \\ I_{pu2} & I_{pd2} \end{bmatrix} \begin{bmatrix} K_u \\ K_d \end{bmatrix} = \begin{bmatrix} I_{RHS1} \\ I_{RHS2} \end{bmatrix}$$

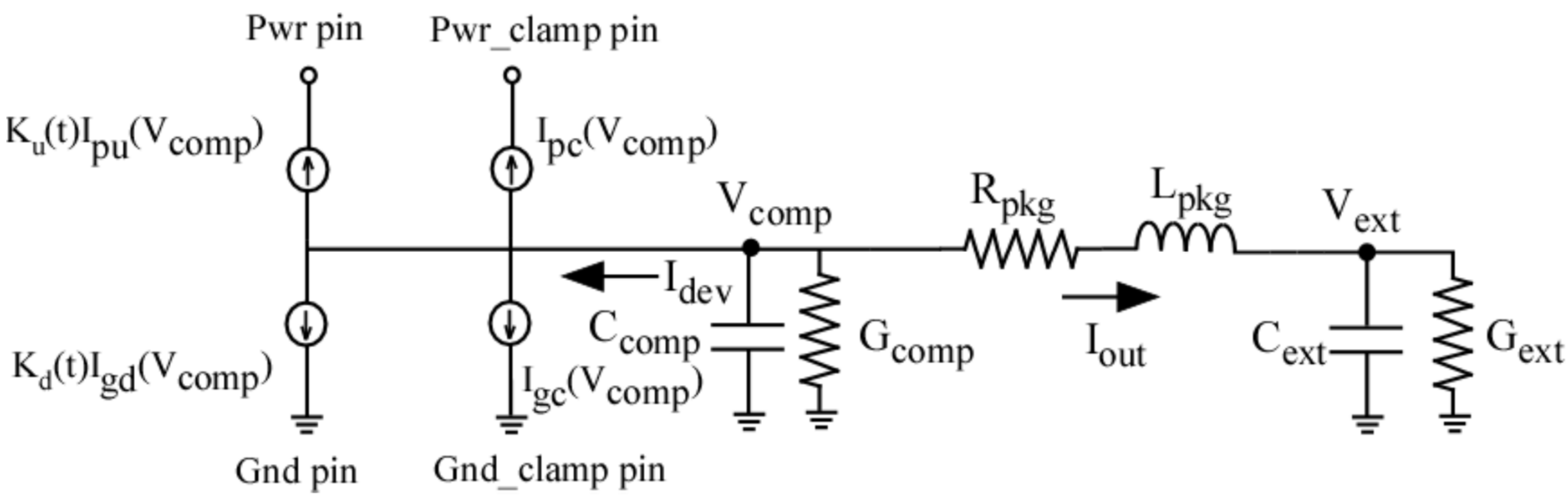
Solve for K_u and K_d

Example of Ku and Kd





IBIS Simulations

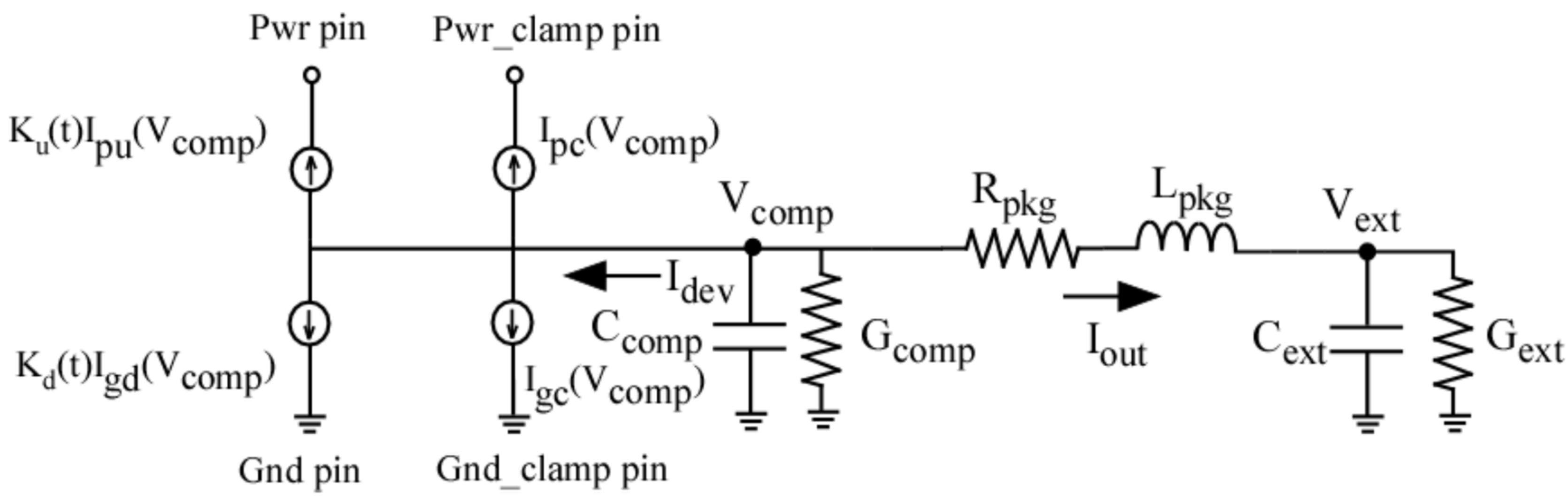


$$K_u I_{pu}\left(V_{comp}\right)+K_d I_{pd}\left(V_{comp}\right)+I_{pc}\left(V_{comp}\right)+I_{gc}\left(V_{comp}\right)$$

$$+I_{out}\left(V_{comp}\right)+I_{C_{comp}}\left(V_{comp}\right)+I_{G_{comp}}\left(V_{comp}\right)=0$$

Nonlinear system ➔ use Newton-Raphson

...or Better: Use a LIM Formulation



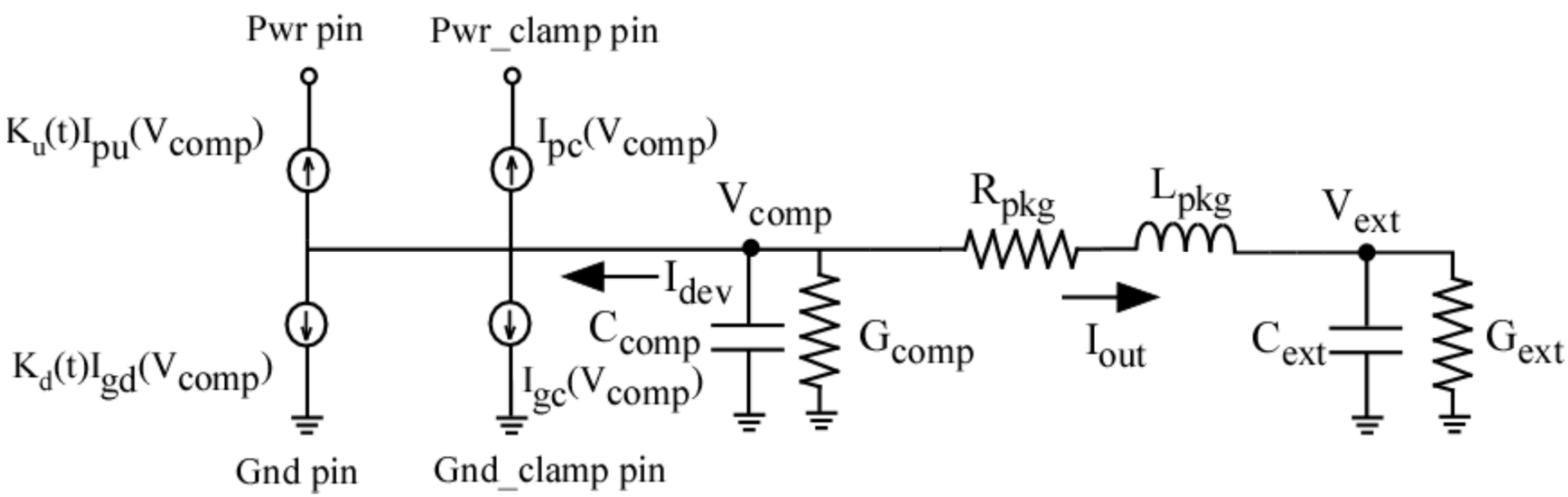
$$C_{ext}\frac{\left(V_{ext}^{n+1/2}-V_{ext}^{n-1/2}\right)}{\Delta t}+\frac{G_{ext}}{2}\left(V_{ext}^{n+1/2}+V_{ext}^{n-1/2}\right)=I_{out}^{n}$$

$$V_{ext}^{n+1/2}=\frac{I_{out}^{n}+\left(\frac{C_{ext}}{\Delta t}-\frac{G_{ext}}{2}\right)V_{ext}^{n-1/2}}{\left(\frac{C_{ext}}{\Delta t}+\frac{G_{ext}}{2}\right)}$$

$$V_{comp}^{n+1/2}-V_{ext}^{n+1/2}=L_{pkg}\frac{\left(I_{out}^{n+1}-I_{out}^{n}\right)}{\Delta t}+\frac{R_{pkg}}{2}\left(I_{out}^{n+1}+I_{out}^{n}\right)$$

$$I_{out}^{n+1}=\frac{\left(V_{comp}^{n+1/2}-V_{ext}^{n+1/2}\right)+I_{out}^{n}\left(\frac{L_{pkg}}{\Delta t}-\frac{R_{pkg}}{2}\right)}{\left(\frac{L_{pkg}}{\Delta t}+\frac{R_{pkg}}{2}\right)}$$

IBIS-LIM Solution



$$C_{comp}\frac{\left(V_{comp}^{n+1/2}-V_{comp}^{n-1/2}\right)}{\Delta t}+\frac{G_{comp}}{2}\left(V_{comp}^{n+1/2}+V_{comp}^{n-1/2}\right)=-I_{out}^{n}-I_{dev}^{n}$$

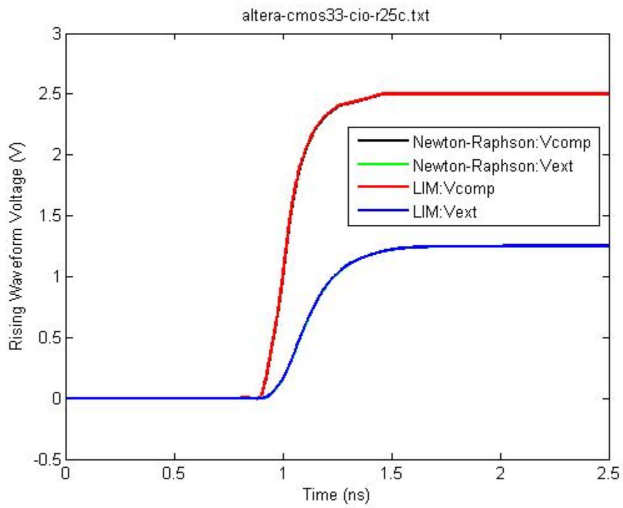
Explicit equations

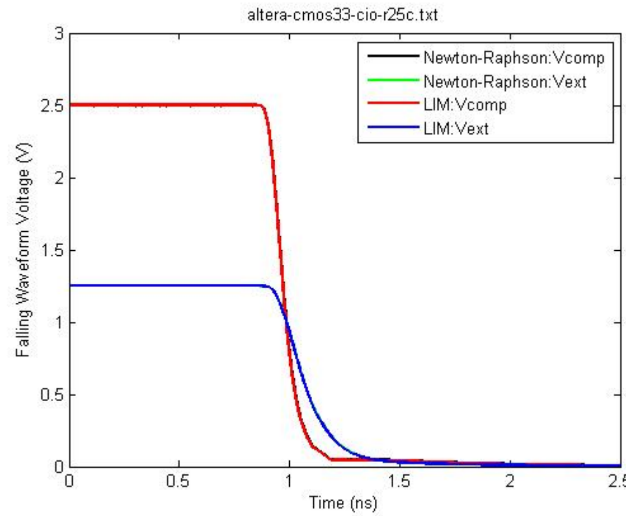
$$V_{comp}^{n+1/2}=\frac{-I_{out}^{n}-I_{dev}^{n}+\left(\frac{C_{comp}}{\Delta t}-\frac{G_{comp}}{2}\right)V_{comp}^{n-1/2}}{\left(\frac{C_{comp}}{\Delta t}+\frac{G_{comp}}{2}\right)}$$

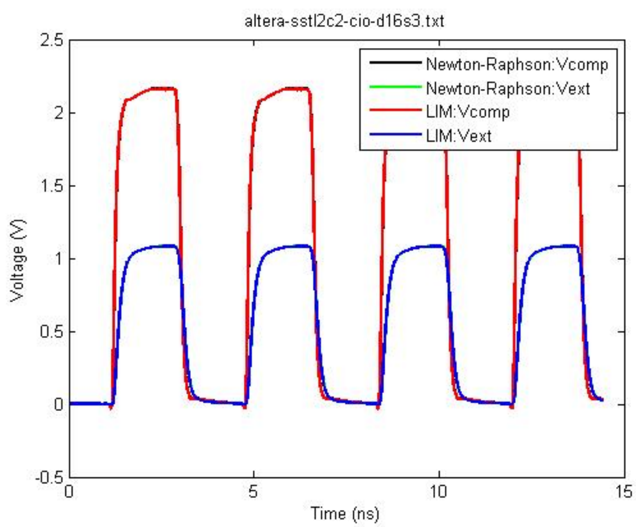
$$I_{dev}^{n}=K_u I_{pu}\left(V_{comp}\right)+K_d I_{pd}\left(V_{comp}\right)+I_{pc}\left(V_{comp}\right)+I_{gc}\left(V_{comp}\right)$$

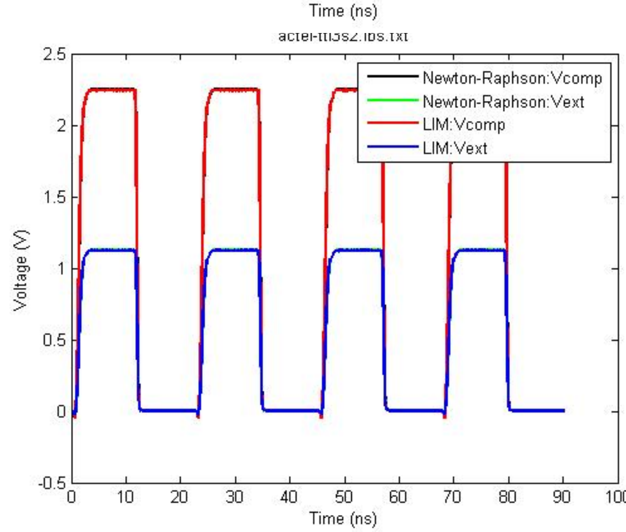
Transient Simulation Examples

NR and LIM give same results…



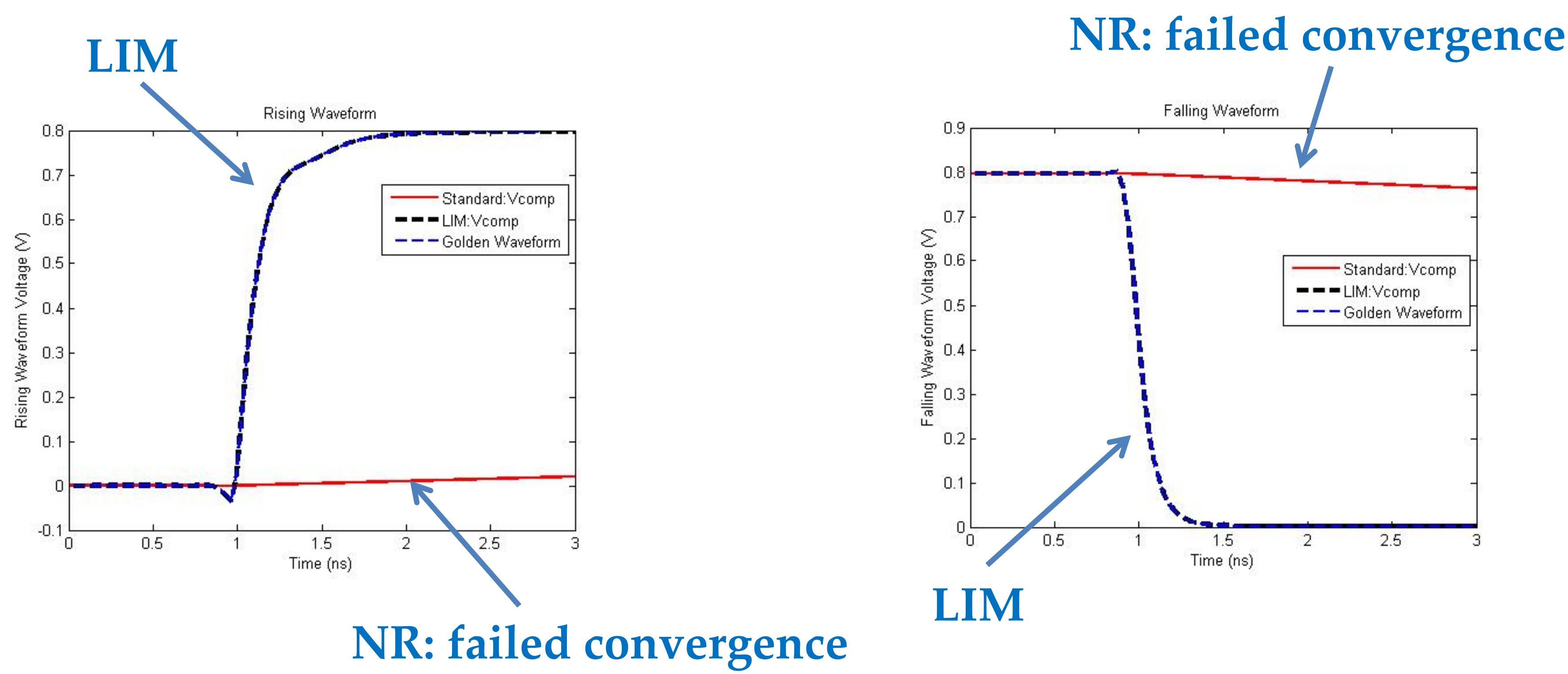






Transient Simulation Examples

… in some cases Newton-Raphson fails to converge…



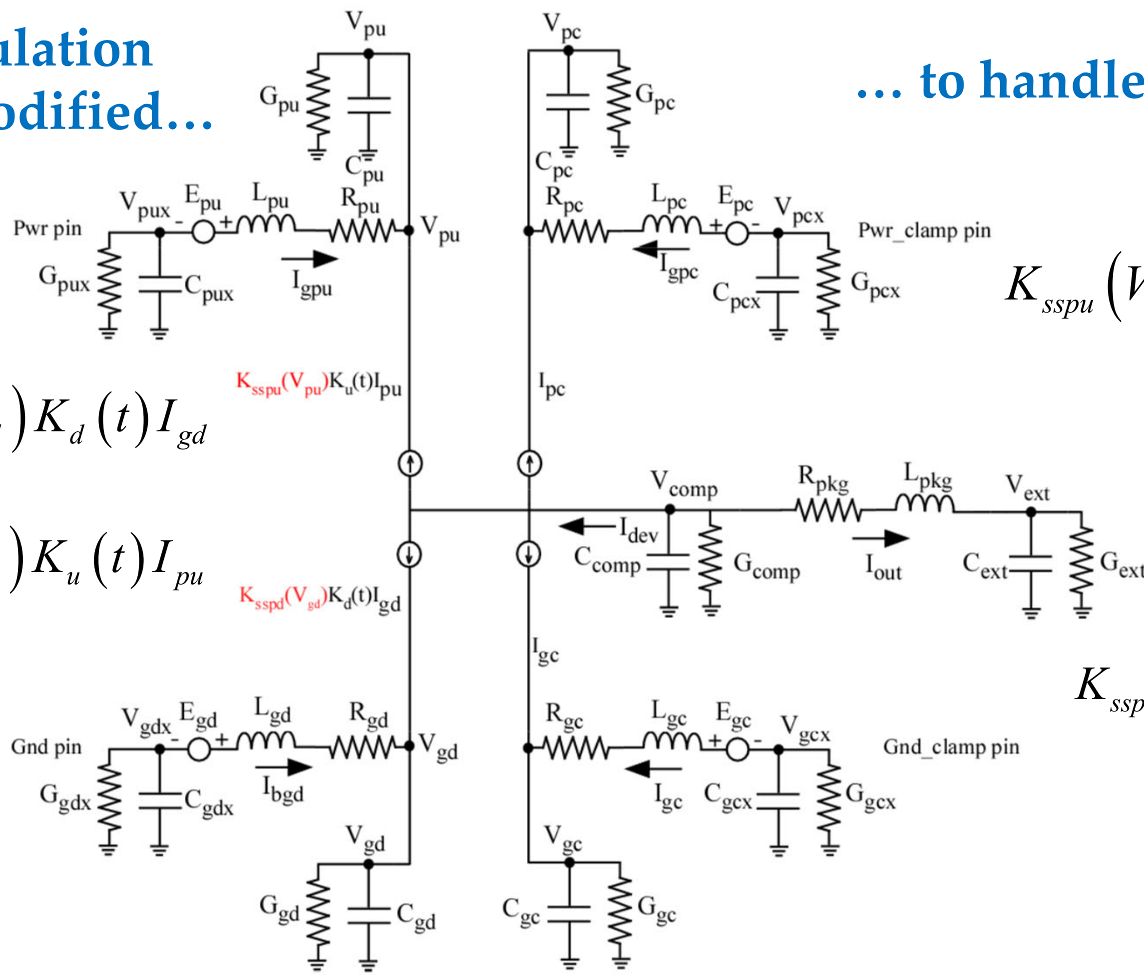
Handling Gate Modulation Effects (BIRD 98.3)

LIM-IBIS formulation can easily be modified…

… to handle SSN

$$K_d(t)I_{gd} \rightarrow K_{sspd}(V_{gd})K_d(t)I_{gd}$$

$$K_u(t)I_{pu} \rightarrow K_{sspu}(V_{pu})K_u(t)I_{pu}$$



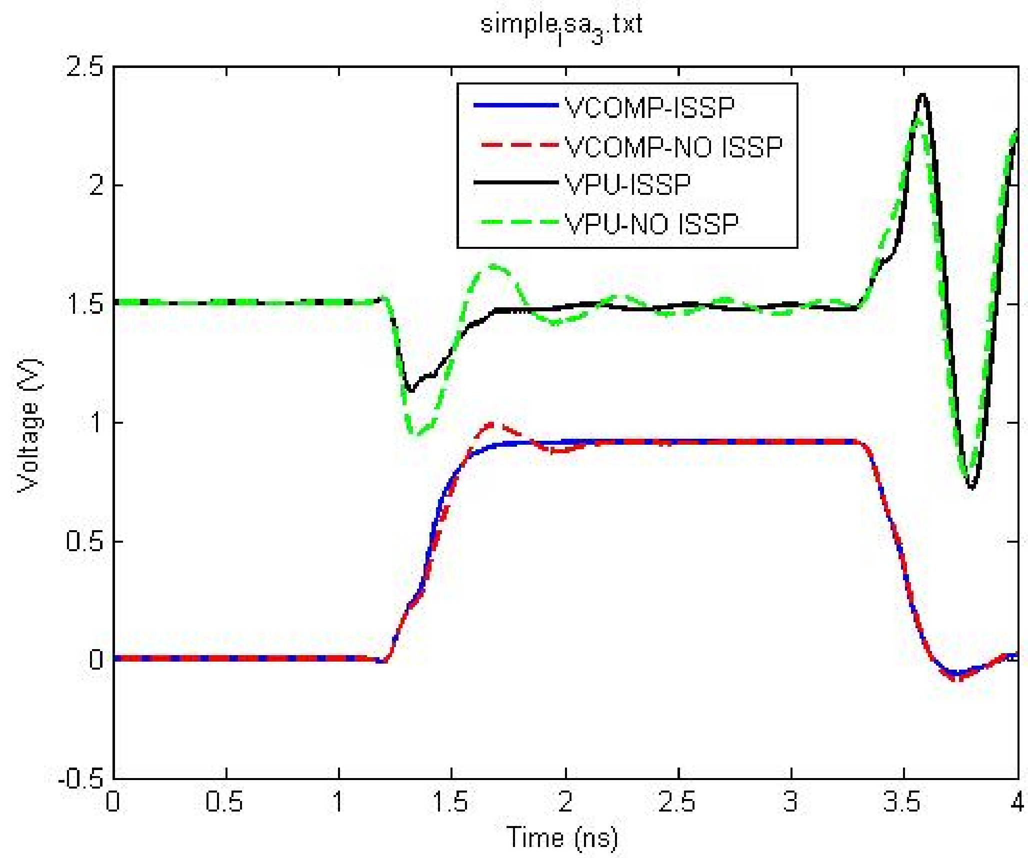
$$K_{sspu}(V_{pu}) = \frac{I_{sspu}(V_{pu})}{I_{sspu}(0)}$$

$$K_{sspd}(V_{gd}) = \frac{I_{sspd}(V_{gd})}{I_{sspd}(0)}$$

Gate Modulation Effects (BIRD 98.3)

Large power supply inductance
Small decoupling capacitance

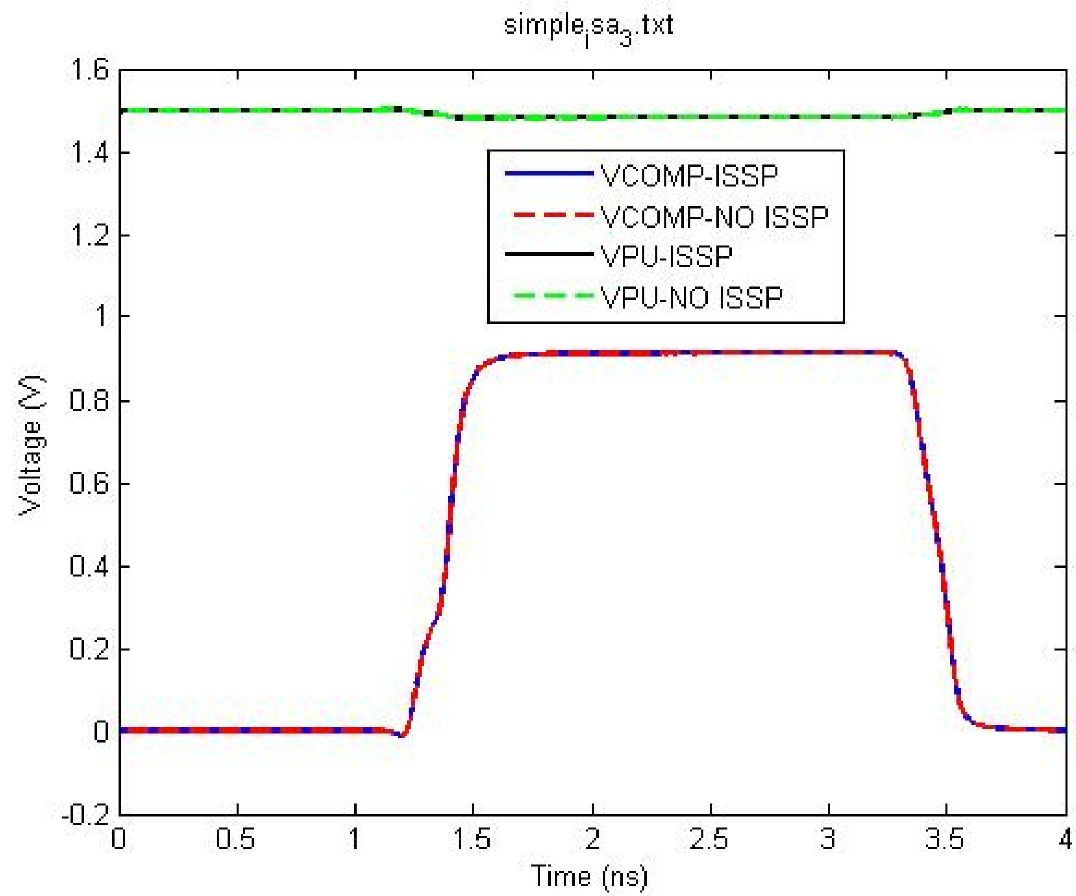
L_{pu} = 5 nH
C_{pu} = 0.001 nF



Gate Modulation Effects (BIRD 98.3)

Small power supply inductance
Large decoupling capacitance

L_{pu} = 0.005 nH
C_{pu} = 0.1 nF



IBIS for Signal Integrity

- Crosstalk
- Ringing, Overshoot, undershoot
- Distortion, Nonlinear effects
- Reflections issues
- Line termination analysis
- Topology scheme analysis

Visit http://www.eigroup.org/ibis/ibis.htm

Algorithmic Modeling Interface (AMI)

- faster signal processing algorithms
- intellectual property protection
- used in convolution transient engines
- designed to be used with fixed time step data
- introduced in IBIS 5.0 specs
- in these specs the library is specified inside the IBIS wrapper

IBIS stands for "I/O Buffer Information Specification"; high-level buffer specification for circuit modeling
http://eda.org/pub/ibis/ver5.0/ver5_0.txt

Simulation Methods

Analysis Method	Advantages	Drawbacks
IBIS	Fast	Not accurate
Device Level	Accurate Nonlinear	Very slow IP liability
Fast convolution	Very fast Handles EQ Include bit patterns	Not Silicon Specific Assumes LTI
Statistical	Very Fast Handles EQ	Not silicon specific No bit patterns Assumes LTI
IBIS-AMI	Fast Handles Vendor EQ Includes Bit Patterns Not limited to LTI	Implementations vary