ECE 546
Lecture -20
Power Distribution Networks

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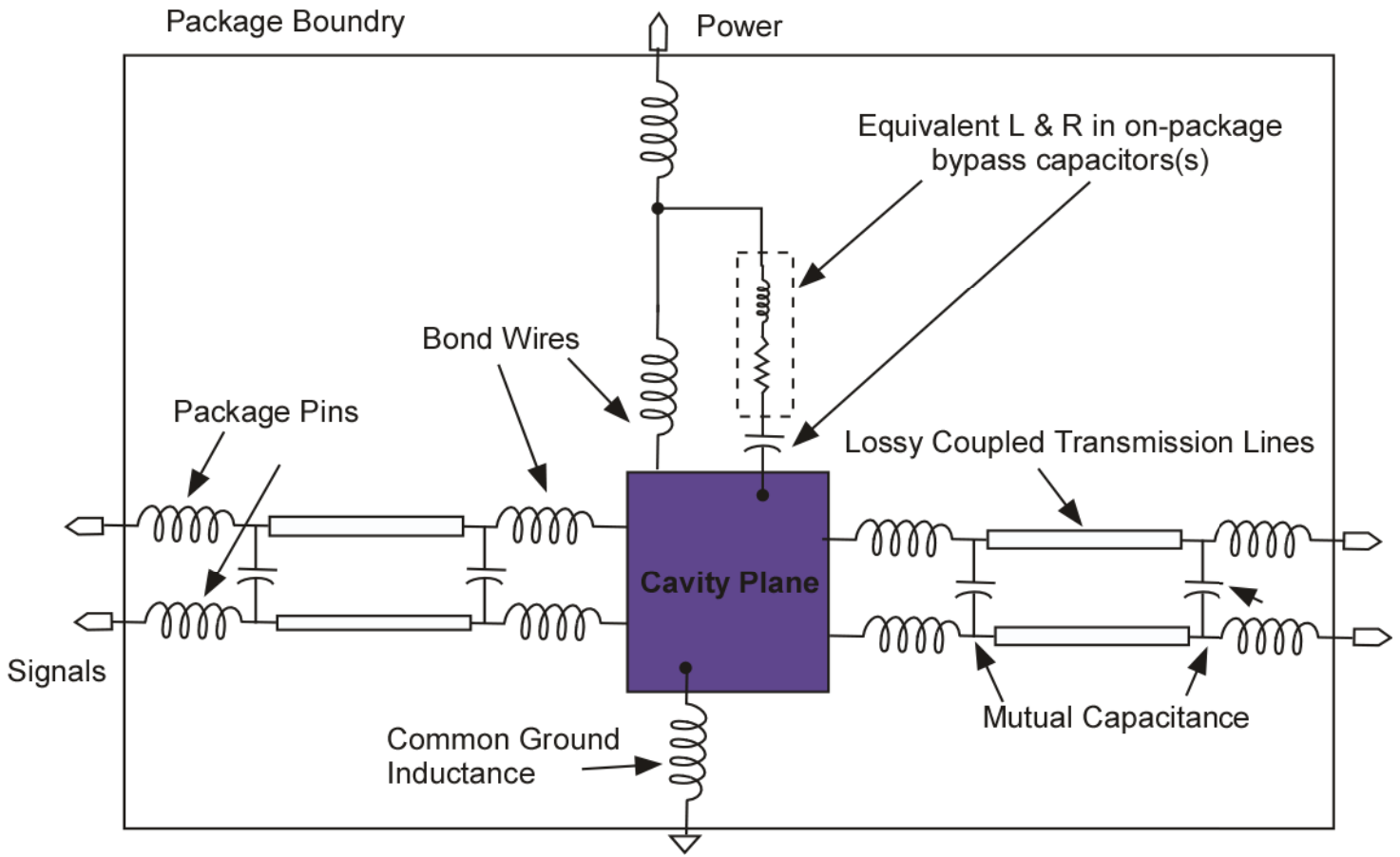
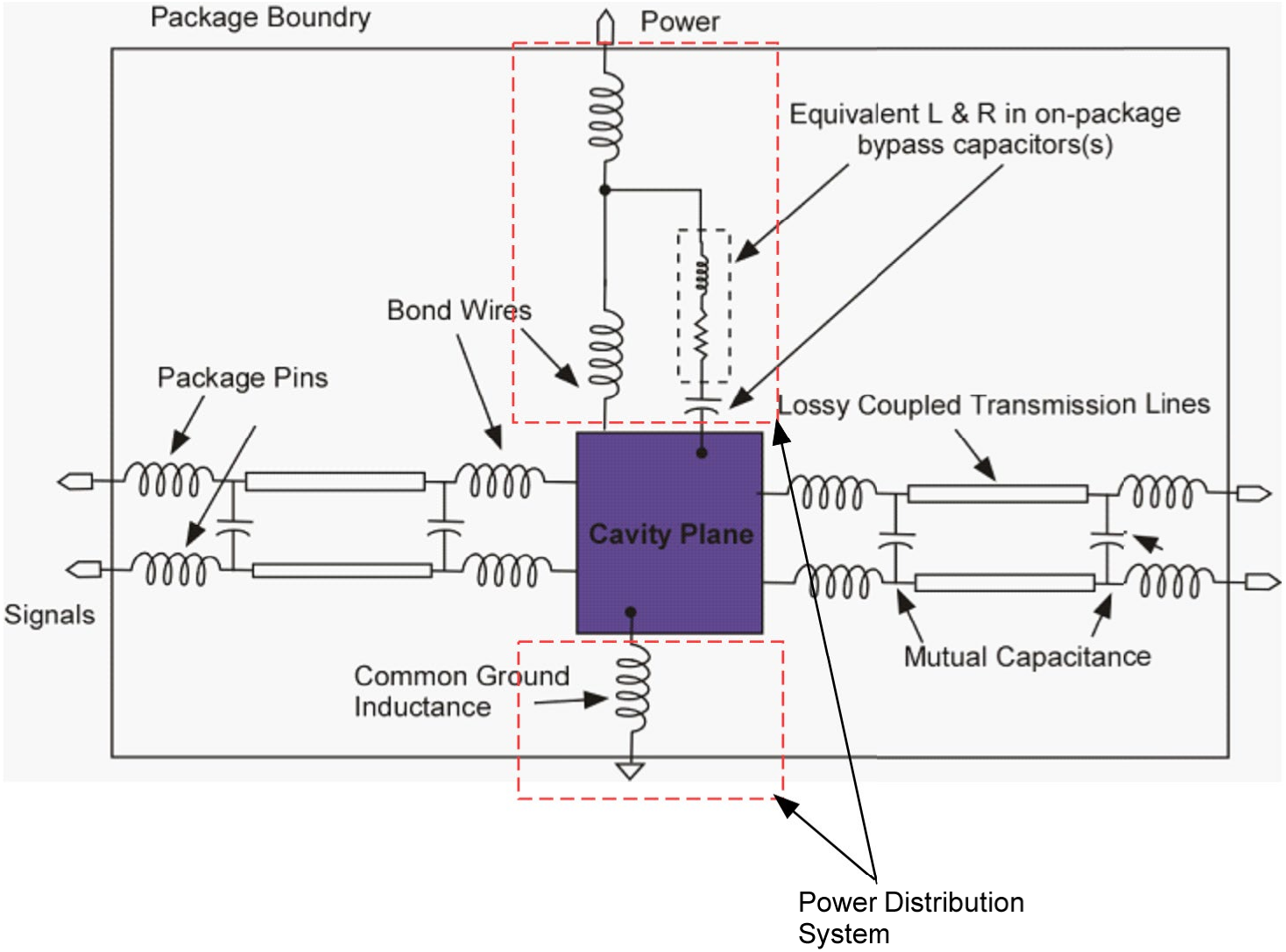
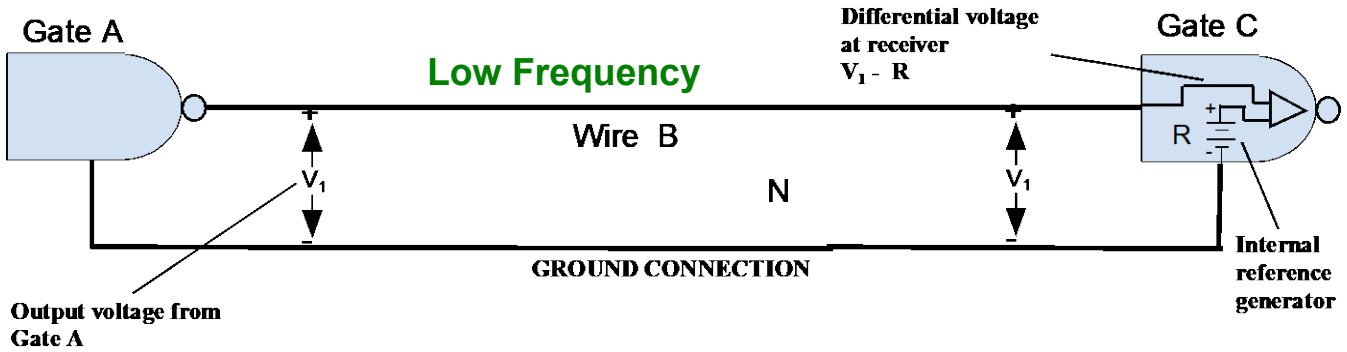
IC on Package

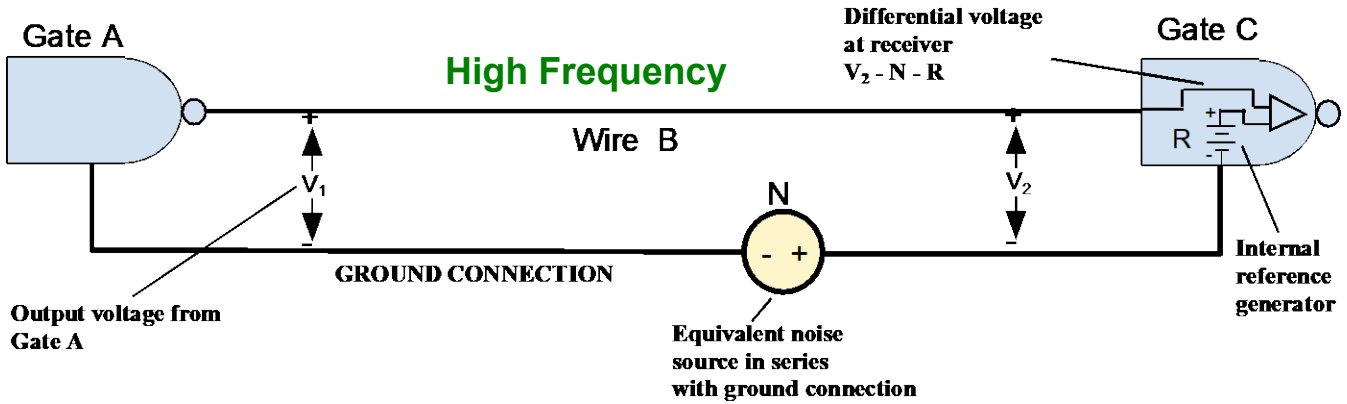


IC on Package



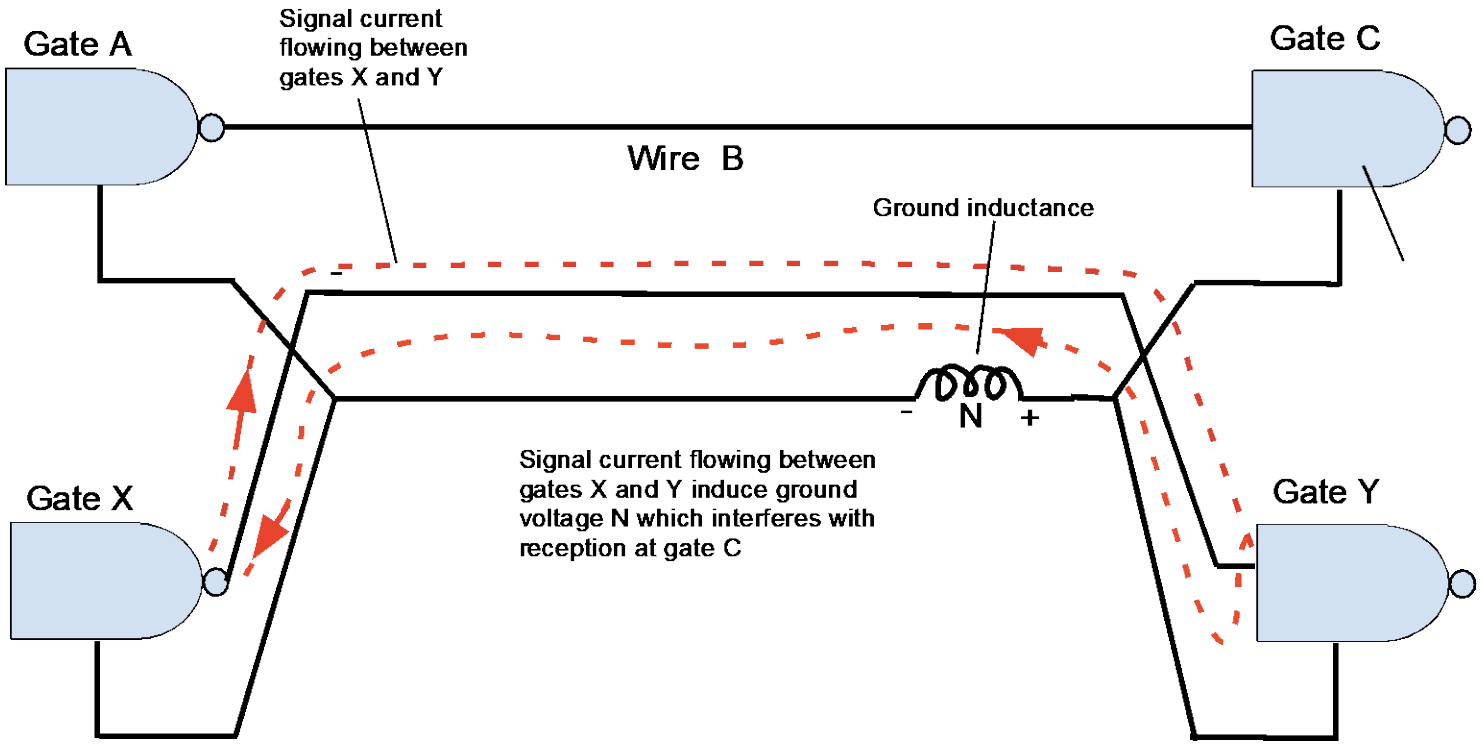
Interconnects and PDN





At high frequencies, Wire B is a transmission line and ground connection is no longer the reference voltage

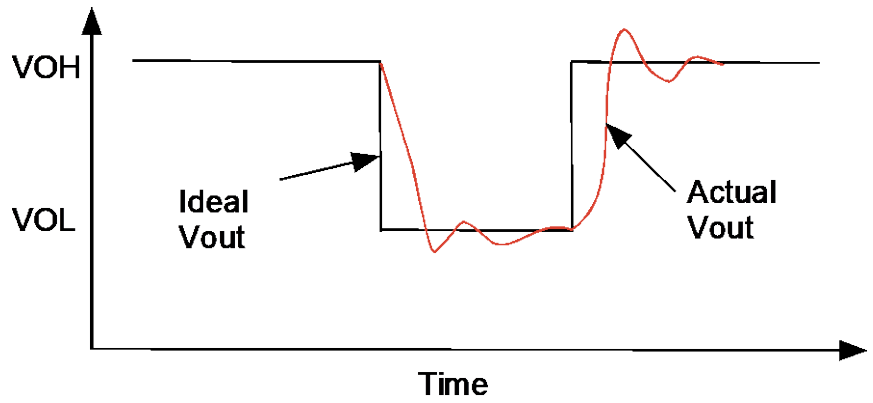
Rules for Power Distribution



- Use low-impedance ground connections between gates
- Provide low-impedance path between power and ground
- Minimize voltage differences between power lines

Power Integrity Issues

- Power-supply-level fluctuations
- Delta-I noise
- Simultaneous switching noise (SSN)
- Resonance
- Ground bounce
- IR Drop



Voltage Fluctuations

- Voltage fluctuations can cause the following
  - Reduction in voltage across power supply terminals. May prevent devices from switching
  - Increase in voltage across power supply terminals➔reliability problems
  - Leakage of the voltage fluctuation into transistors
  - Timing errors, power supply noise, delta-I noise, simultaneous switching noise (SSN)

Power-Supply-Level Fluctuations

- Total capacitive load associated with an IC increases as minimum feature size shrinks
- Average current needed to charge capacitance increases
- Rate of change of current (dI/dt) also increases

- Total chip current may change by large amounts within short periods of time
- Fluctuation at the power supply level due to self inductance in distribution lines

Reducing Power-Supply-Level Fluctuations

Minimize dI/dt noise

- Decoupling capacitors
- Multiple power & ground pins
- Taylored driver turn-on characteristics

Decoupling capacitors

- Large capacitor charges up during steady state
- Assumes role of power supply during current switching
- Leads should be small to minimize parasitic inductance
- Must be placed as close as possible to the chip

Motivation and Objectives

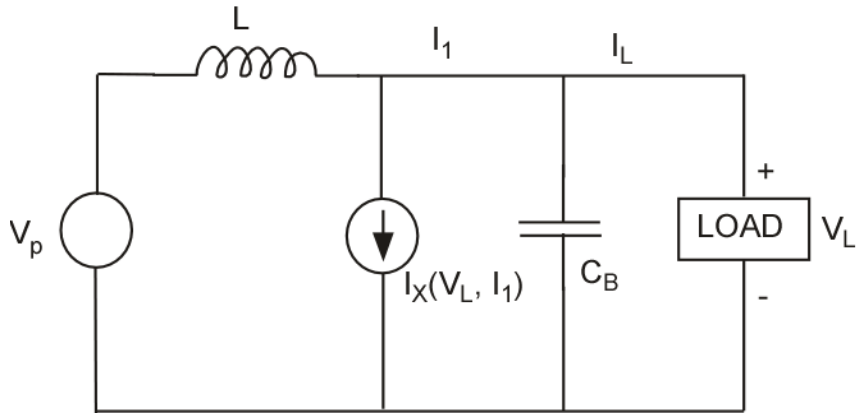
- Provide stable, quiet DC supply voltage
- Compensate for large AC current draws
- Compensate for fast transients

- Current draws of 200A
- Rate of change of 200 GA/s
- Voltage supply needs to be maintained within 10%

Local Regulation

- Used to prevent overshoot so voltage cannot exceed nominal value by more than a small amount.
- Supply overshoot can be reduced via clamping
- Supply voltage droops can be reduced using shunt regulators
- Clamps draw little power and are inexpensive
- Shunt regulators dissipate considerable average power and are expensive

Local Regulation Using Clamps



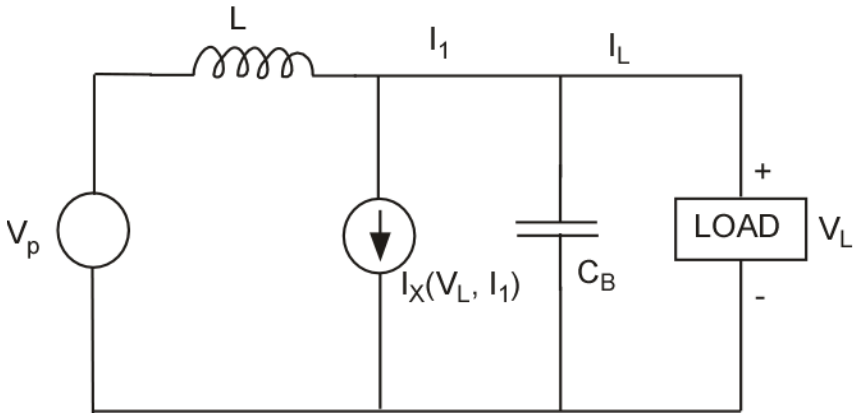
$$I_X = \begin{cases} 0 \text{ if } V_L < V_n \\ k_s(V_L - V_n) \text{ if } V_L > V_n \end{cases}$$

k_s: transconductance of clamp

- Clips off top half cycle by directing inductor current into clamp rather than capacitor➔prevents overshoot.

- Cannot prevent supply voltage drooping.

Shunt Regulators



$$I_X = \max\left[0, I_{\max} - I_1 + k_s(V_L - V_n)\right]$$

k_s: transconductance

Keeps current constant

Regulates voltage

- **Not used on chip**
- **Power hungry and expensive**
- **Last resort to prevent supply voltage droops**

Effects of SSN

SSN can affect circuits in 3 ways

1) SSN may increase chip-to-chip delays
2) Affects the operation of the receiving chips
3) May affect gates on the sending chip

Current driven off-chip has only one return path: power and ground pins of the chip carrier➔ to minimize effective inductance of the return path and noise, many power/ground pins must be supplied for off-chip drivers

On-chip circuitry can close the loop by small inductance on chip lines

Design Criteria for SSN

Inductive time constant must be much smaller than its capacitive time constant

$$\frac{L}{R} \ll RC$$

Valid for external power distribution lines that carry the current to the chip and for internal lines that distribute it on the chip

- Presently satisfied by on-chip lines
- Board and package power lines are too high to satisfy criteria

Design Criteria for SSN

- Cannot distribute power on the board simply by using the printed circuit wires and connecting them to the power/ground pins of the chip directly.

- Off chip power distribution must employ methods that reduce the effects of line and pin inductance.

To insure reliable circuit operation:

$$L\frac{dI}{dt} \ll V_{DD}$$

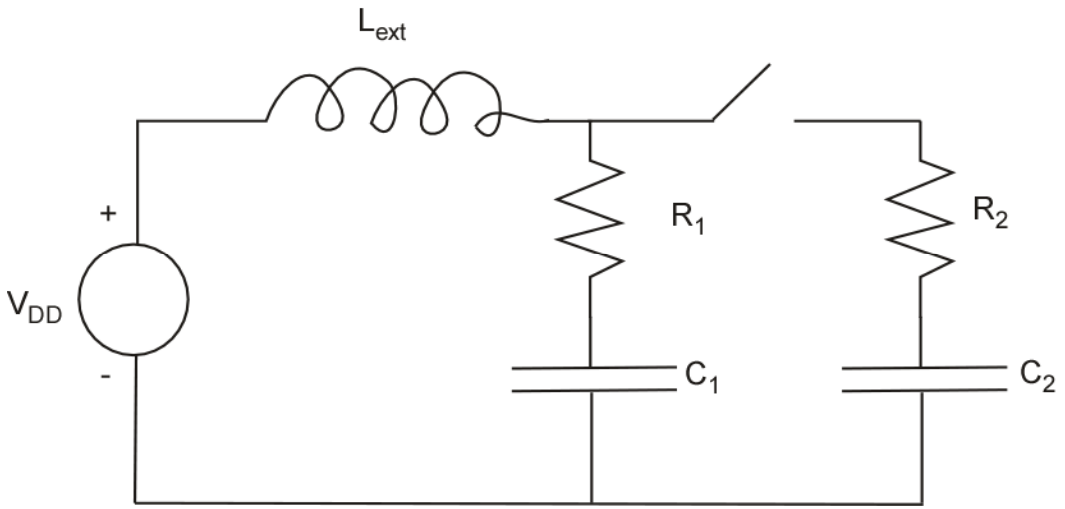
Equivalence of 2 conditions is obtained by setting:

$$dI = V_{DD} / R$$

$$dt = RC$$

Delta-I Noise in CMOS Circuits

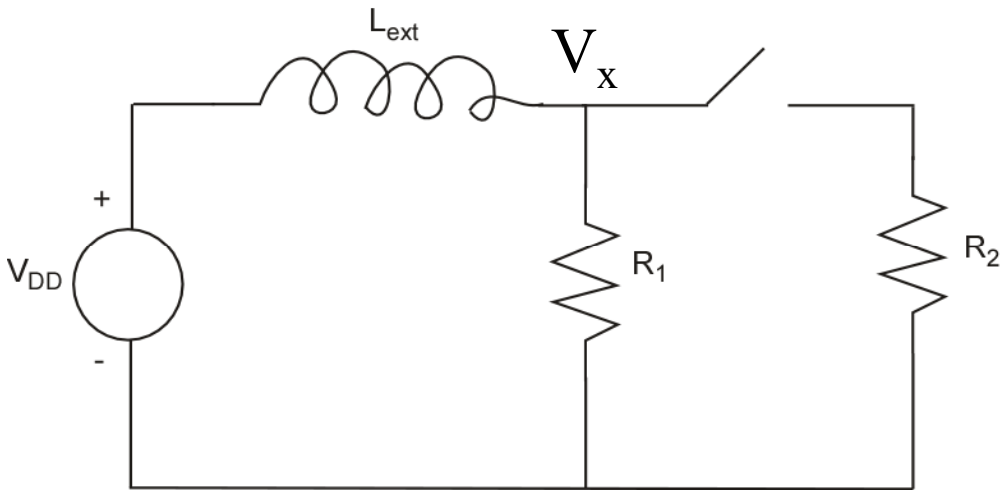
In a CMOS chip the portion of the circuit that is not switching (R_1, C_1) at a given system cycle helps the switching portion of the chip (R_2, C_2).



$$V_{DD} + \Delta V = \frac{C_1}{C_1 + C_2} V_{DD}$$

Delta-I Noise in ECL Bipolar Circuits

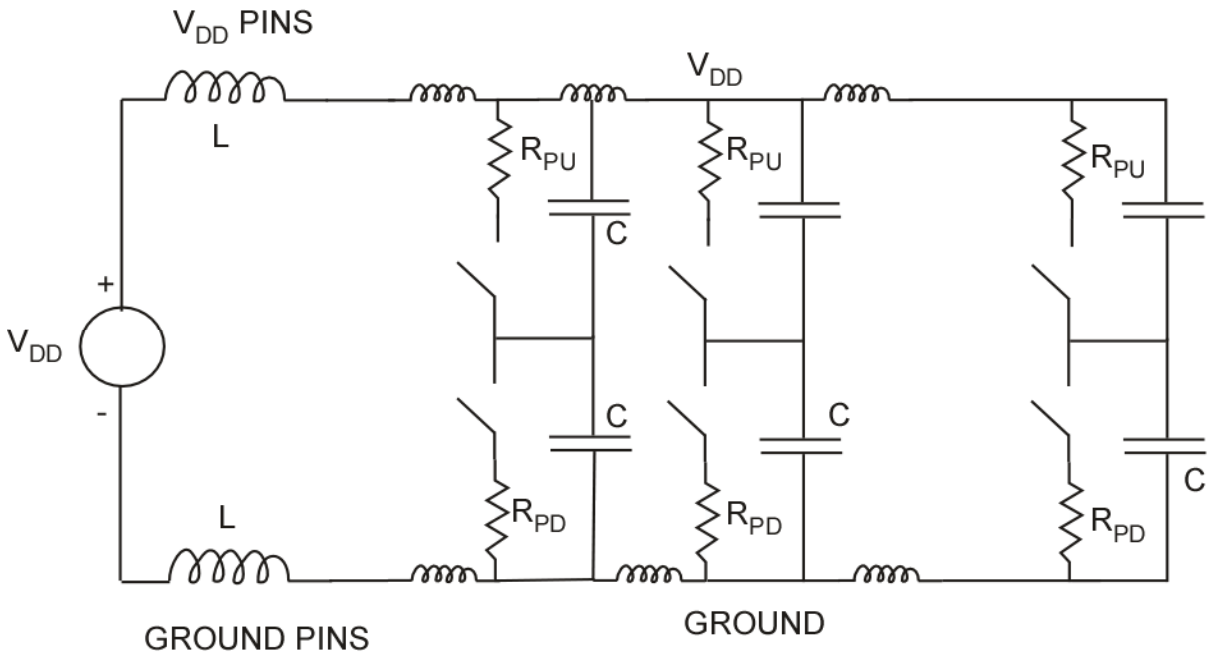
Because of diode structure of BJTs, current can only flow in one direction



DC current of gates (proportional to V_x) help reduce power-supply-level fluctuations

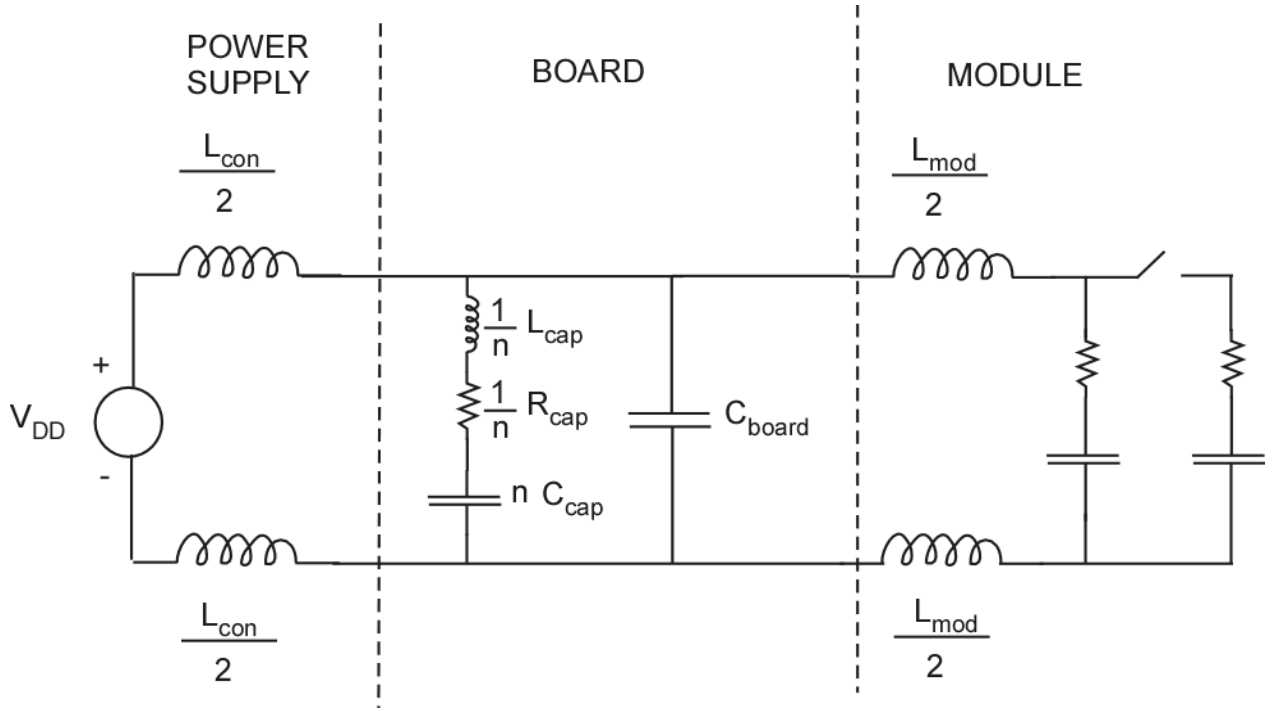
$$\Delta V = -\frac{R_1}{R_1 + R_2} V_{DD}$$ For turn on $$\Delta V = \frac{R_1}{R_2} V_{DD}$$ for turn off

Model for On-Chip Power Distribution



1) Portion of circuits switch
2) V_{dd}-V_{SS} is reduced
3) Non-switching devices come to rescue (through low inductance)
4) Share charge with switching capacitors
5) Power-level collapse is prevented

Model for CMOS Power Distribution Network



- n decoupling capacitors
- L_{con} is due to power connectors at edge of board
- C_{board} is intrinsic power and ground capacitance

Off-Chip Driver SSN Calculations

- Worst case on-chip delta-I noise generated at beginning of clock cycle
- Main problem for on-chip drivers is lack of low-inductance return path
- Off-chip drivers are the major source of SSN

Problem:

32 low-impedance CMOS buffers ($R_S << Z_o$) are switched simultaneously. In addition, the line impedance is 50 Ω, rise time is 2 nsec, output swing is 5 V, and the allowed power-supply-level fluctuation is 0.25V. Find the effective inductance.

Solution:

First, calculate the rate of change of the output voltage from the voltage swing and rise time

$$\frac{dV}{dt} = \frac{80\% \times V_{swing}}{t_r} = \frac{80\% \times 5V}{2n\,\text{sec}} = 2V / n\,\text{sec}$$

Off-Chip Driver SSN Calculations

The current driven into the transmission line is $I=V/Z_o$ and its rate of change is:

$$\frac{dI}{dt}=\frac{1}{Z_o}\frac{dV}{dt}=\frac{2V/n\sec}{50\Omega}=0.04A/n\sec$$

Total current transient for 32 drivers:

$$\frac{dI_{TOT}}{dt}=N_{drv}\frac{dI}{dt}=1.28A/n\sec$$

Through a 1nH inductance the voltage drop is $\Delta V=L\frac{dI}{dt}=1.28V$

To guarantee a maximum of 0.25V voltage fluctuation, the effective inductance is

$$L=\frac{\Delta V}{dI/dt}=0.2nH$$

PDN Network

- A PDN in a system provides the interconnection framework in which gates are allowed to switch states
- Power supplies are bulky and cannot be connected directly to IC, therefore interconnections (with resistance and inductance) are used
- Current through wires create DC drop and voltage fluctuations
- PDN must be created to regulate voltage for required current to be supplied over time
- The speed at which a circuit operates determines the speed at which charge can be supplied or removed from capacitors

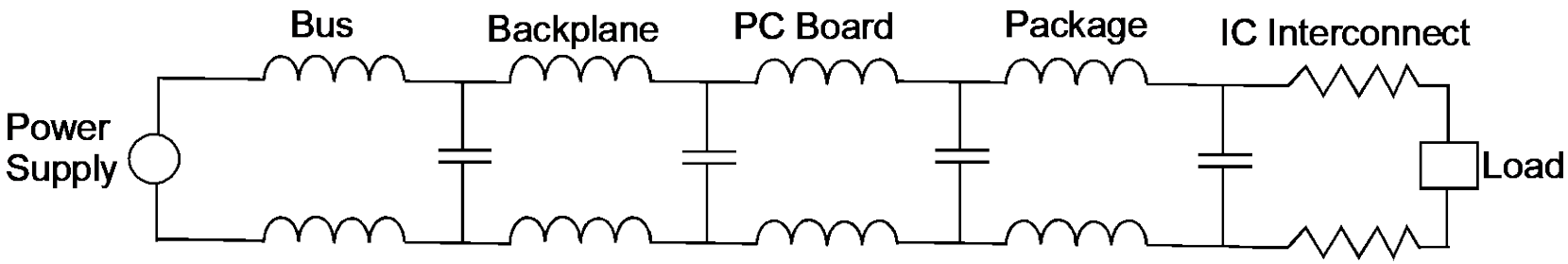
PDN Network

- A PDN consists of a power supply, DC-DC converters, lots of decoupling capacitors and interconnections
- Power supply provides high voltage and current to motherboard
- Voltage is reduced through a DC-DC converter
- Decoupling capacitors are distributed on the motherboard package and IC and act as charge reservoirs

General Topology for Power Distribution

- Hierarchy of distribution networks
- Usually a tree sometimes a loop
- Upper level inductive with distributed caps
- On-chip level resistive with distributed caps

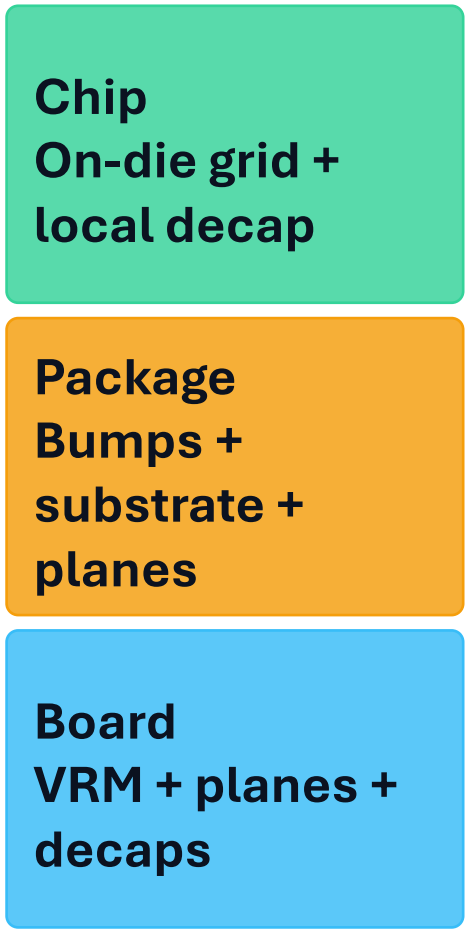
Power Supply Network



- On board inductance and on-chip resistance
- Symmetry between power and ground (return path)
- Distributed over several levels of interconnections

Hierarchical PDN

- Board level handles low-frequency energy and large current inventory.
- Package level controls loop inductance between board decaps and die bumps.
- Chip level cleans up the last distance to switching transistors and local hotspots.



Typical frequency ownership

Board / VRM	kHz → tens of MHz
Package	MHz → low GHz
Chip	100 MHz → multi-GHz

No single capacitor technology spans the entire range.

The same rail is implemented with very different geometries and bandwidth limits as we move from VRM to die.

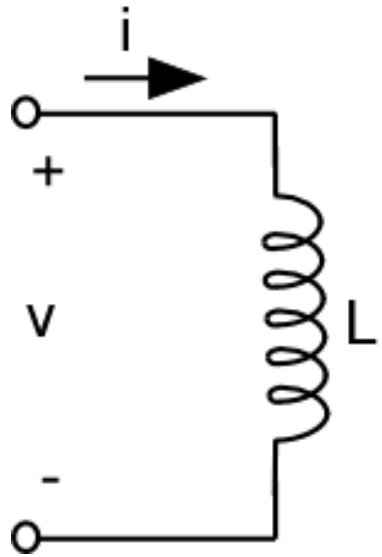
Mechanism

- For an IC, the transient current flowing through an inductor gives a voltage drop V=LdI/dt
- Positive dI/dt leads to reduction in supply voltage. Negative dI/dt results into an increase in supply voltage ➔reliability problems has several components
- Supply noise has several components
  - Ultra high frequency noise ~ 100 GHz
  - High-frequency noise 100 MHz-1GHz
  - Mid-frequency noise 1-10 MHz
  - Low frequency noise 1-100 KHz

Current Through an Inductor

$$v = L\frac{di}{dt} \Rightarrow i(t) = \frac{1}{L}\int v\,dt$$

$$i(t) = \frac{1}{L}\int_0^t v(\tau)\,d\tau$$



Current through an inductor must be continuous

Role & Function of Bypass Capacitors

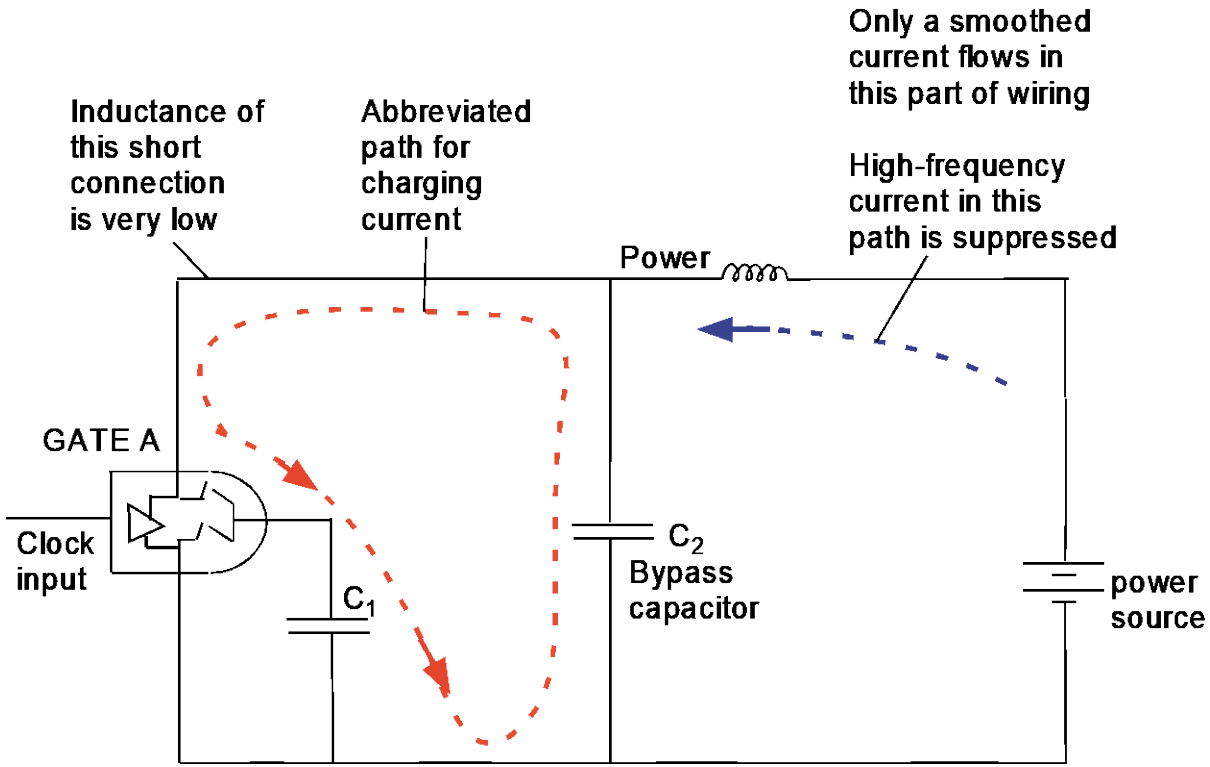
- Inserted between power and ground in path between supply and load
- Supply AC current to load faster than inductor can respond
- Can be distributed or lumped➔intermediate between a transmission line and an LC circuit
- In reality includes some resistance and inductance

IC PDN

- Core: Primarily made of transistors
- I/O: Provides communication with other ICs
- Core and I/O require separate PDN

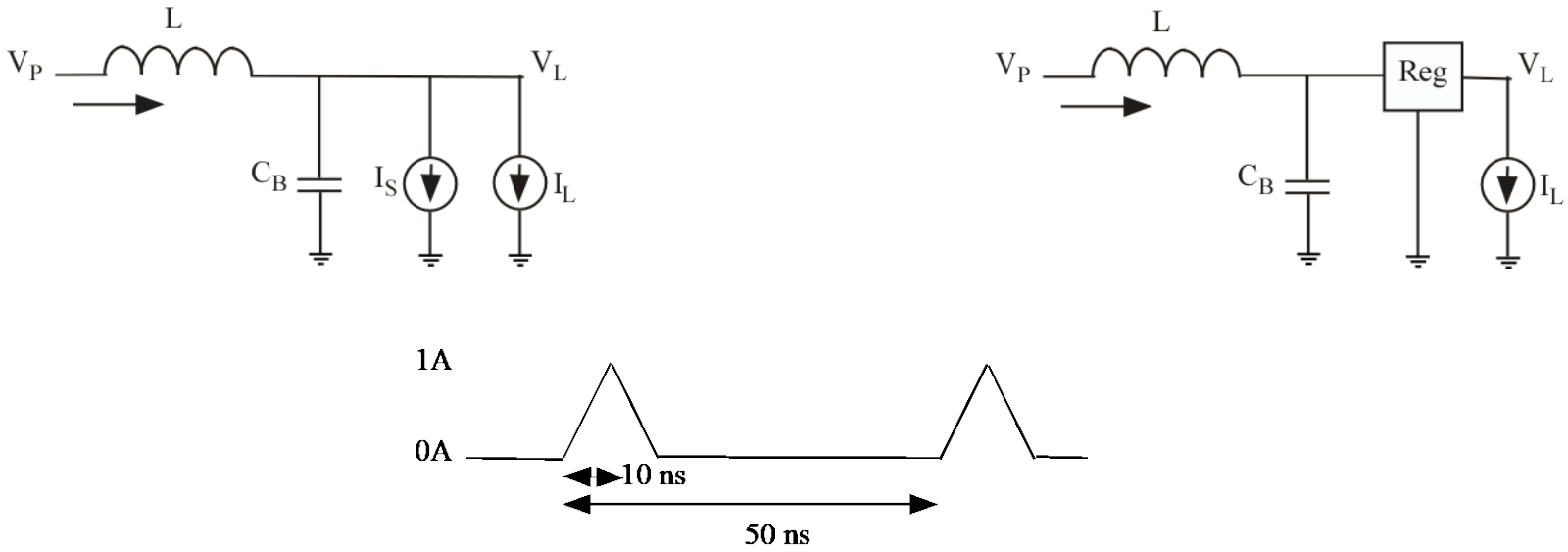
- Goal: ensure sufficient charge is supplied to switching CKT so capacitance can be charged to required voltage
- Charge has to be supplied within a short time➔minimize delay need L/R<<RC

Bypass Capacitors



- Reduce voltage drops caused by the inductance of PDN

Bypass Capacitor & series Regulator

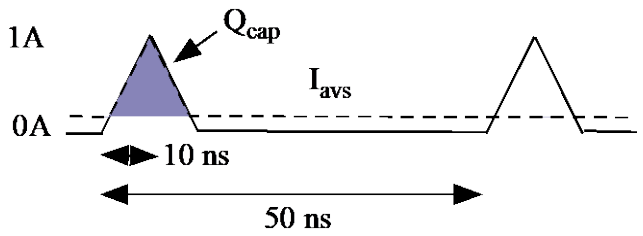


L= 10 nH

What value of C_B will keep V_L to 5% with

- No regulator
- Series regulator 3.3V to 2.5V

Bypass Capacitor & series Regulator



No regulator

ΔV=125 mV
I_{av}=200 mA
Q_{cap}=6.4 nC
$C_B > 76.8$ nF

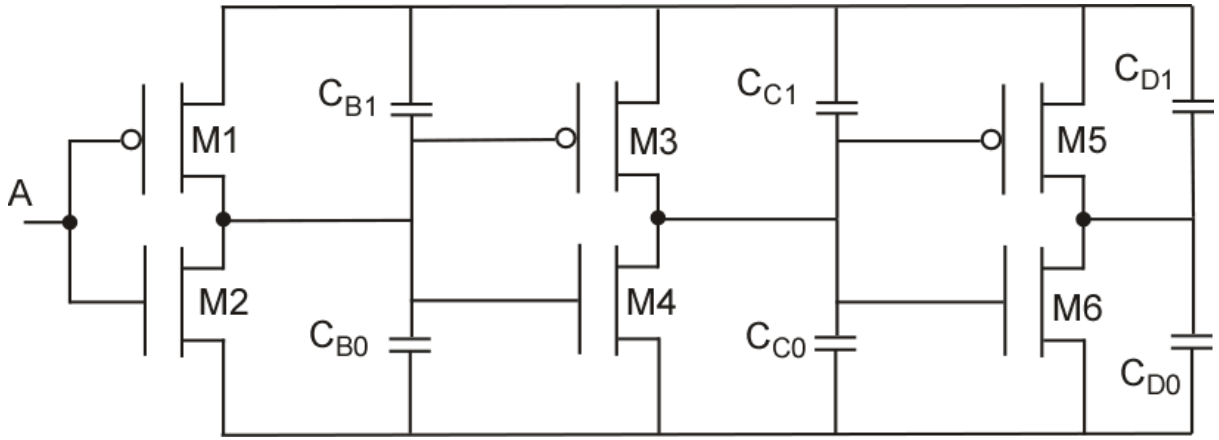
With regulator

ΔV=925 mV
I_{av}=200 mA
Q_{cap}=6.4 nC
$C_B > 7.39$ nF

P_{supply}=660W

Symbiotic Bypass Capacitors

- **On-Chip Bypass Capacitors**
  - MOS transistor with source and drain tied together
  - About half the capacitors are symbiotic



- **50K Gate Module Example**
  - Load capacitance C_{ld}=100fF
  - 4,000 gates switching simultaneously
  - 46,000 gates with output loads across power supplies ➔ 2.3 nF
  - Adequate to average supply current over a cycle

On-Chip Bypass Capacitors

- **Area Bonding**
  - Flip chip
  - More power distribution to next level of packaging
  - Reduce inductance
  - Helps metal migration problem

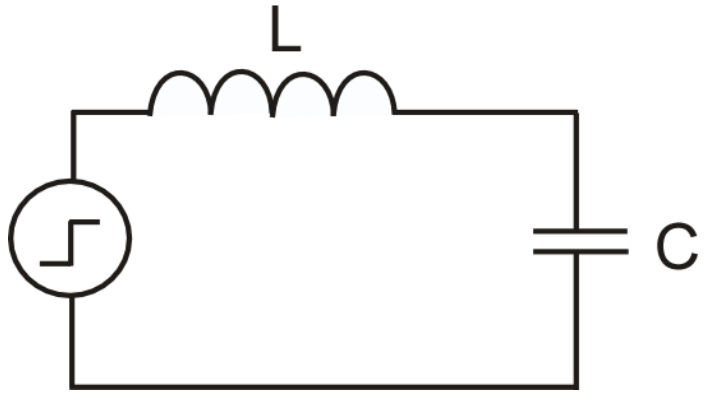
A capacitor satisfies the relation: $C_B > \frac{k_i I_{av} t_{ck}}{\Delta V}$

Reduces current load to average value

Thin oxide MOS capacitor: MOS transistor with source and drain tied together

$$C_{ox} = \frac{\varepsilon_r \varepsilon_o WL}{t_{ox}}$$

Natural Frequency



- LC tank will resonate at natural frequency

$$\Delta V = \frac{I_{avg}}{C\omega_C}\sin(\omega_C t)$$

$$= I_{avg}\sqrt{\frac{L}{C}}\sin(\omega_C t)$$

$$\Delta V_{\max} = I_{avg}\sqrt{\frac{L}{C}}$$

To keep the ripple within a prescribed ΔV, the capacitor must be sized so that

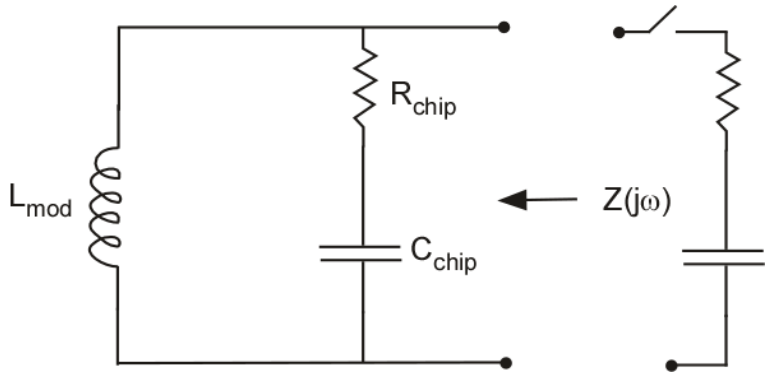
$$C_B > L\left(\frac{I_{avg}}{\Delta V}\right)^2$$

Natural Frequency of Bypass Capacitors

- Load currents at frequencies well below ω_c see an inductive impedance.
- Load currents at high frequencies see a capacitor.
- At ω_c, impedance is infinite
- At ω_c, even small currents will cause oscillations

Resonance Condition at Power-Supply Lines

- Periodic nature of digital circuits can cause resonance
- Large fluctuation can build up and cause circuit to fail



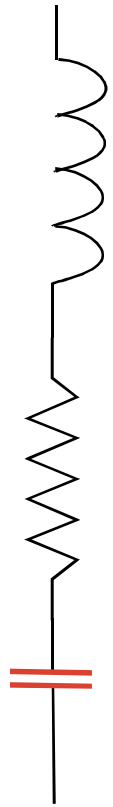
$$f_{chip} = \frac{1}{2\pi\sqrt{L_{mod}C_{chip}}}$$

$$\left|Z(j\omega_{chip})\right| \approx \frac{L_{mod}}{R_{chip}C_{chip}}$$

- f_{chip} should be much larger than the clock frequency
- Resonant impedance should be kept small

Frequency Range for Bypass Capacitors

- **Capacitors at low frequencies**
- **Actually an RLC circuit**
- **Resonance frequencies**
  - LC frequency
  - RC frequency
- **Ineffective at either of these frequencies**

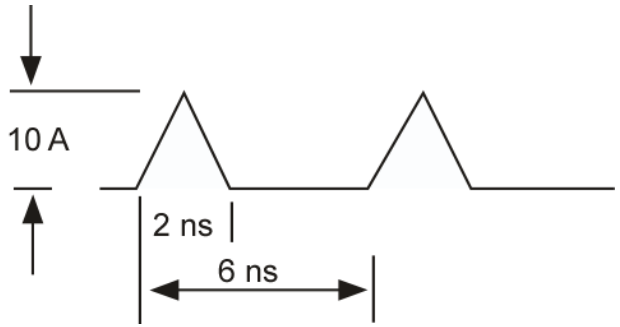


Bypass Capacitor - Table

	C	R_S	L_C	F_{RC}	F_{LC}	F_{LR}
On-chip MOS 0.35 x 114 mm)	250 fF	10 Ω	0	64 GHz		
On-chip MOS (1.4 x 115 μm)	1 pF	40 Ω	0	4 GHz		
SMT ceramic	1 nF	0.1 Ω	1 nH		160 MZ	
SMT ceramic	10 nF	0.1 Ω	1nH		50 MHz	
Ceramic disk	10 nF	0.1 Ω	5 nH		23 MHz	
Aluminum electrolytic	10 μF	1 Ω	10 nH	160 kHz		16 MHz
Aluminum electrolytic	1000μF	0.05 Ω	10 nH	3 kHz		800 kHz

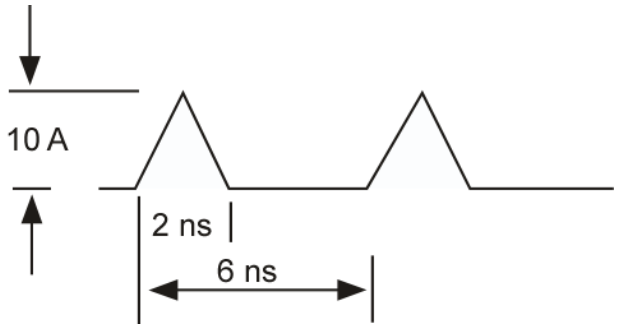
Bypass Capacitor Network Design

Using the parameters of the Table, derive a parallel combination of bypass capacitors that is able to supply the current needs of a load with the periodic triangular waveform sketched below that may start and stop abruptly. Your combined capacitor should hold voltage ripple to within 5% of the supply voltage. Assume that your capacitors are fed from a DC supply voltage of 3.3V through an inductance of 1 μH.



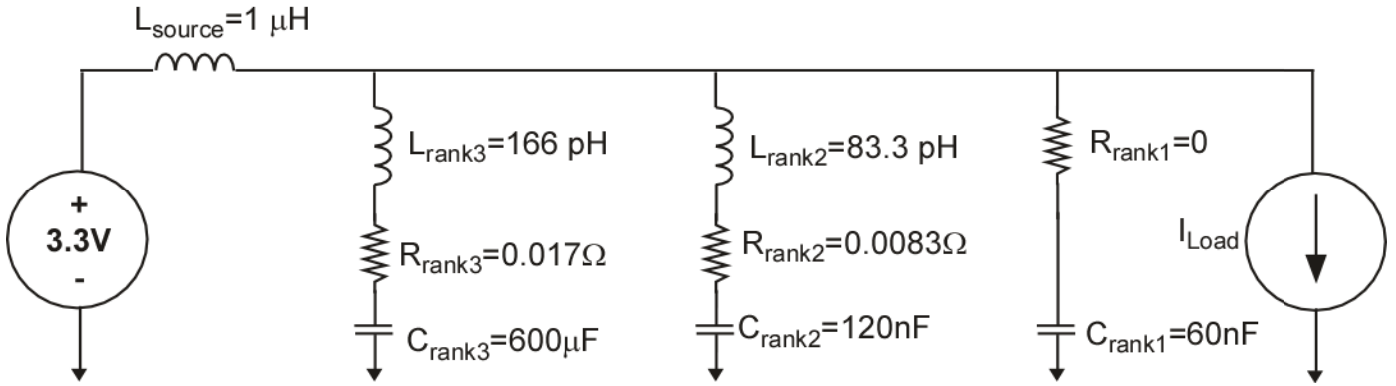
Bypass Capacitor Network Design

- Derive parallel combination of bypass capacitors
- Hold voltage ripple to within 5% of supply voltage
- DC supply of 3.3V
- Generator internal inductance 1 μH



1) ΔV in AC mode < 165mV
2) $V_{Ldrop} + V_{Cdrop} < 165$ mV
3) Capacitor must be operational above breakpoints

Solution



1st Rank

Average current and charge sourced by capacitor:

$$I_{ave} = \frac{10A \times 1ns}{6ns} = 1.67A$$

$$Q_{cap} = (1ns - 0.167ns)(10 - 1.67A) = 6.94nC$$

In AC mode the ΔV of the cap should be less than 165 mV, so:

$$C_{rank1} > \frac{Q_{cap}}{\Delta V} = \frac{6.94nC}{165mV} = 42nF$$

Drop in series L must be less than 165mV

$$L_{rank1} < \frac{\Delta V}{di/dt} = \frac{165mV}{\frac{10A}{1ns}} = 16.5pH$$

1st Rank

- Need breakpoints above 1 GHz to insure true capacitor
- From table, choose 60,000 1pF MOS on-chip cap (min:42,000)

$$C_{rank1} = 60nF, L_{rank1} = 0$$

$$R_{rank1} = \frac{40\Omega}{60,000} = 6.67 \times 10^{-4}\Omega \Rightarrow \text{resistance is negligible}$$

2nd Rank

$$L_{rank+1} < C_{rank}\left(\frac{\Delta V}{I_{ave}}\right)^2$$

Recall: To keep the ripple within a prescribed ΔV, the capacitor must be sized so that

$$C_B > L\left(\frac{I_{avg}}{\Delta V}\right)^2 \Rightarrow L < C_B\left(\frac{\Delta V}{I_{avg}}\right)^2$$

$$L_{rank\,2} < 60nF\left(\frac{165mV}{1.67A}\right)^2 = 586\,pH$$

Cannot connect the first rank up to the supply voltage since supply inductance is 1μH and does not satisfy criterion

Choose 12 SMT ceramic caps➔ satisfies inductance calculations
And doubles 1st rank cap.

$$C_{rank\,2} = 120nF, L_{rank\,2} = 83.3\,pH$$

$$R_{rank\,2} = \frac{0.1\Omega}{12} = 0.00833\Omega$$

3rd Rank

$$L_{rank3} < 120nF\left(\frac{165mV}{1.67A}\right)^2 = 1.17nH$$

Since this is less than the inductance of the supply, need to add 3rd rank of caps

Use 11 aluminum electrolytic caps

$$C_{rank3} = 110\mu F, L_{rank3} = \frac{10nH}{11} = 909pH$$

$$R_{rank3} = \frac{1\Omega}{11} = 0.091\Omega$$

This resistance looks high, need to determine the associated voltage drop…

$$0.091\Omega \times 10A = 910mV \rightarrow$$ **NO GOOD**

$$\Delta V_{\max} = 165mV$$

3rd Rank

Need to reduce resistance to: $R_{rank3} = \frac{165mV}{10A} = 0.0165\Omega$

Choose 60 aluminum electrolytic caps

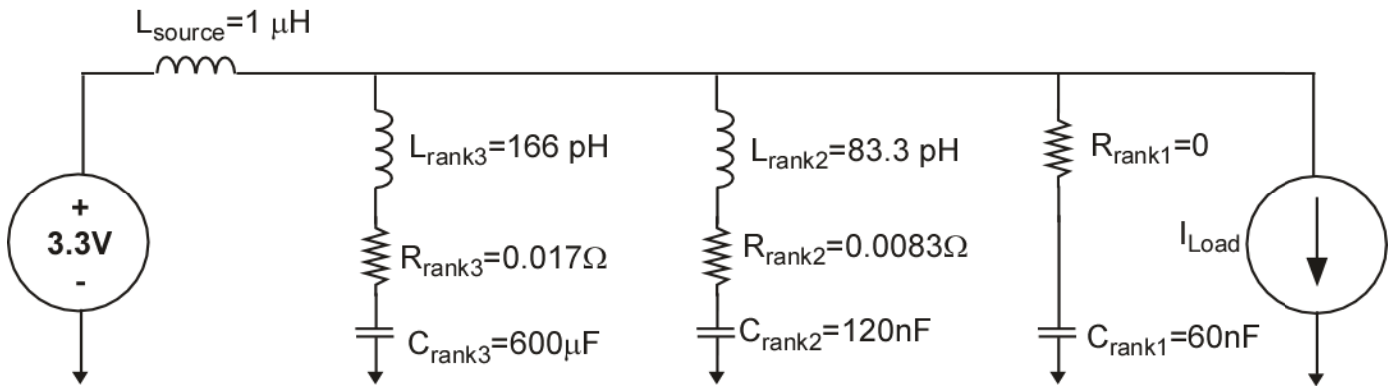
$$C_{rank3} = 600\mu F, L_{rank3} = \frac{10nH}{60} = 166pH$$

$$R_{rank3} = \frac{1\Omega}{60} = 0.0167\Omega$$

4th Rank

$$L_{rank\,4} < 600\mu F\left(\frac{165mV}{1.67A}\right)^2 = 5.86\mu H$$

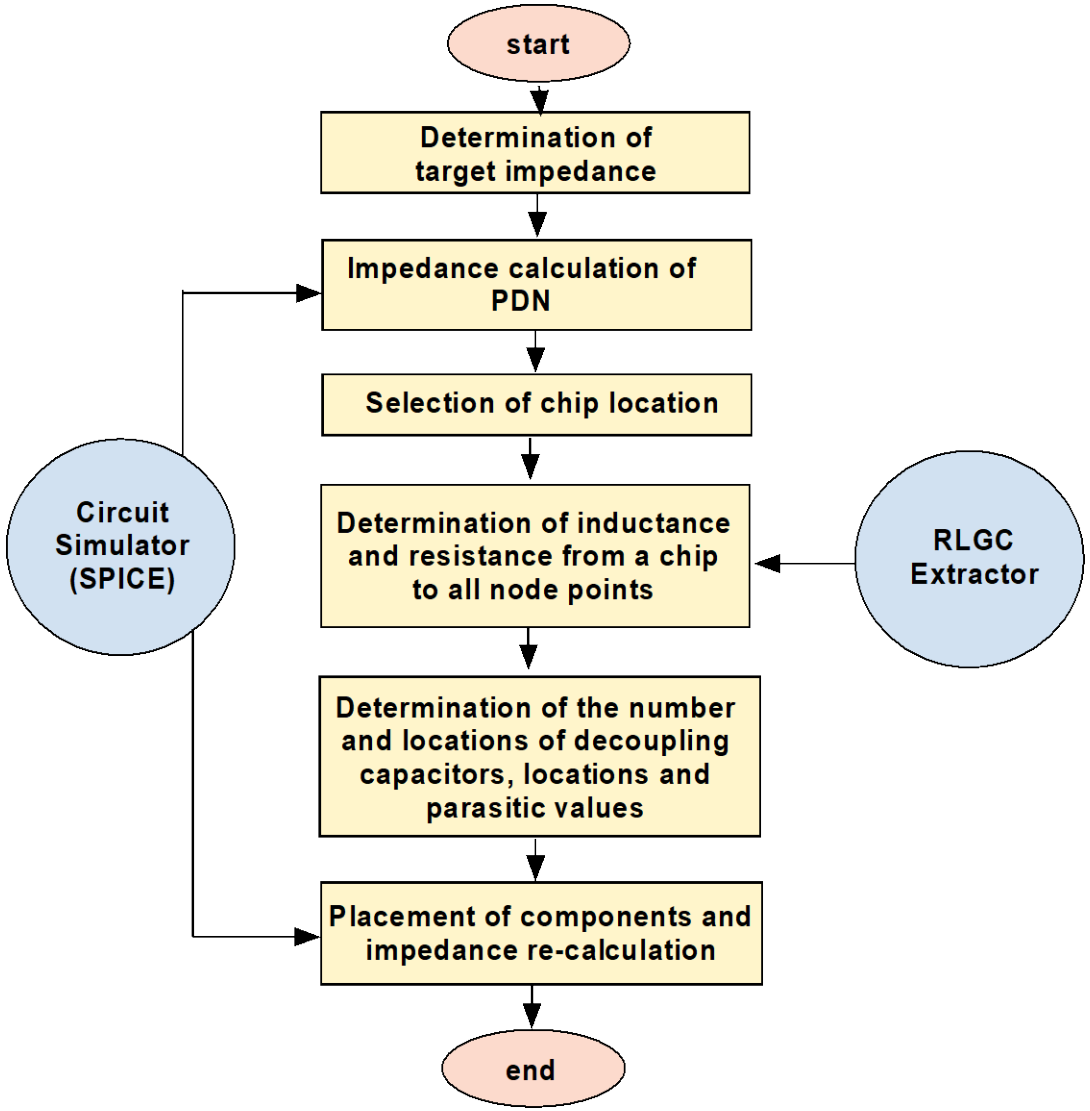
The inductance of the supply voltage satisfies this criterion
➔ no need for 4th rank.



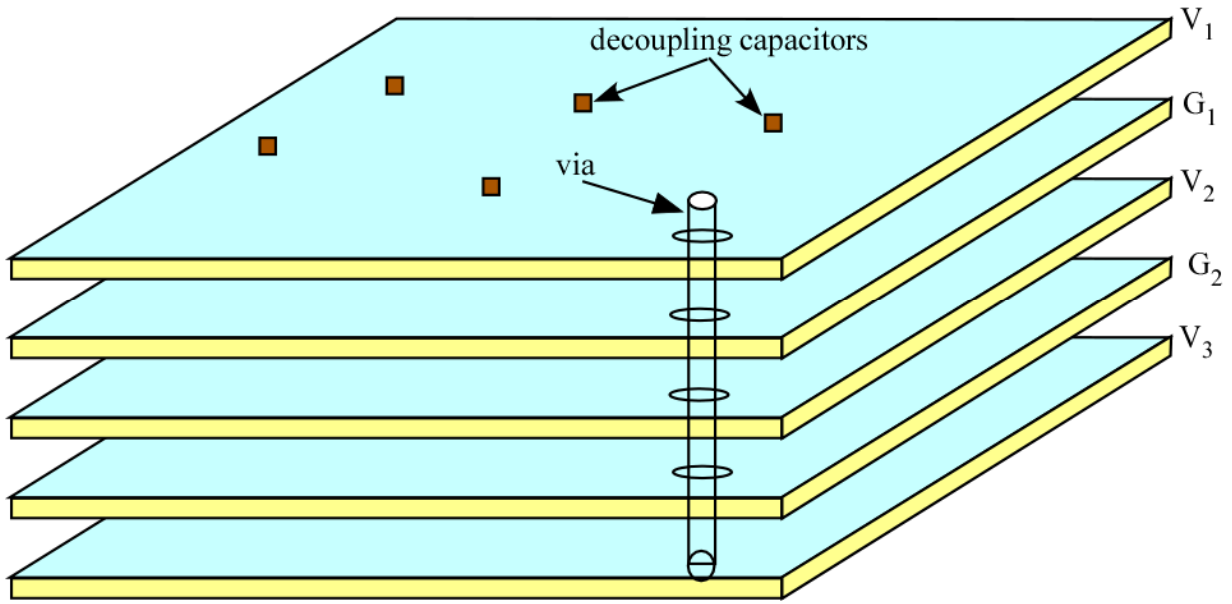
Modeling Power Distribution Networks (PDN)

- Ground planes power bus and return paths are not ideal and must be represented with parasitic inductors and resistors
- Resulting network is a two-dimensional lossy transmission line possibly non-uniform
- Bypass capacitors are needed to alleviate noise
- Simulation is computationally intensive

CAD Framework for PDN Design

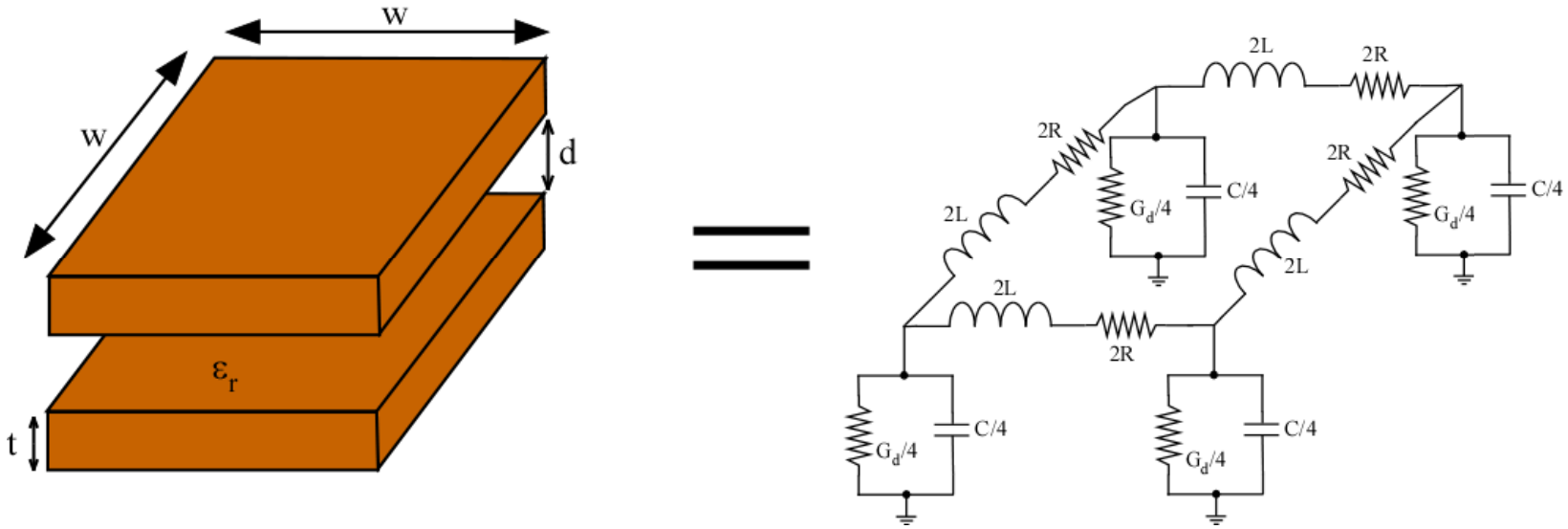


Multilayer Power/Ground Plane



- Power planes support wave propagation
- They behave as cavity resonators supporting radial waves that propagate between the plates

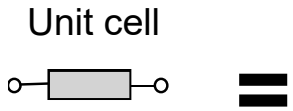
Power/Ground Plane Circuit



$$C = \varepsilon_o \varepsilon_r \frac{w^2}{d} \qquad L = \mu_o d \qquad R_{dc} = \frac{2}{\sigma_c t}$$

$$R_{ac} = 2\sqrt{\frac{\pi f \mu_o}{\sigma_c}}(1+j) \qquad G_d = \omega C \tan(\delta)$$

Example: Power Bus/Ground Plane Model

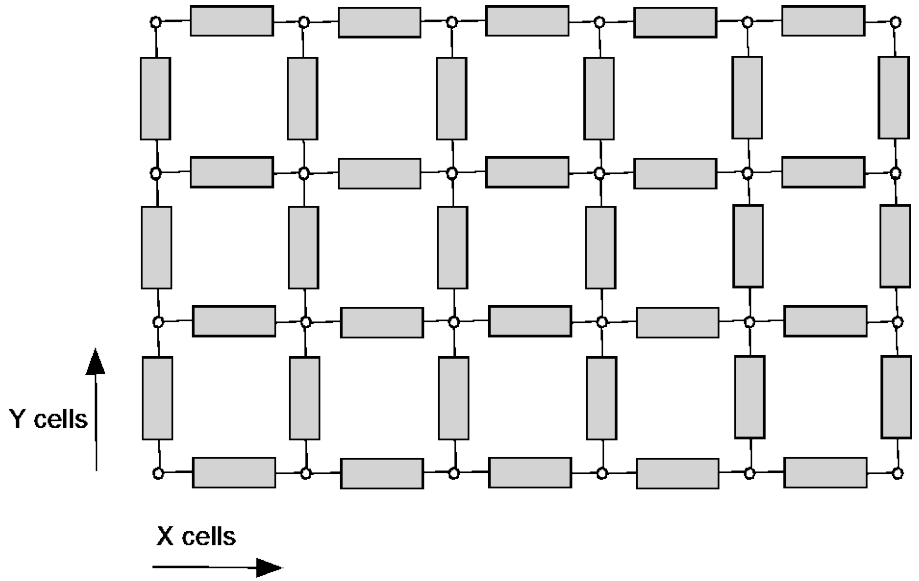


Analysis Methods

- SPICE
- Transmission matrix method
- LIM

Goal is to obtain impedance matrix between some ports of interest as a function of frequency

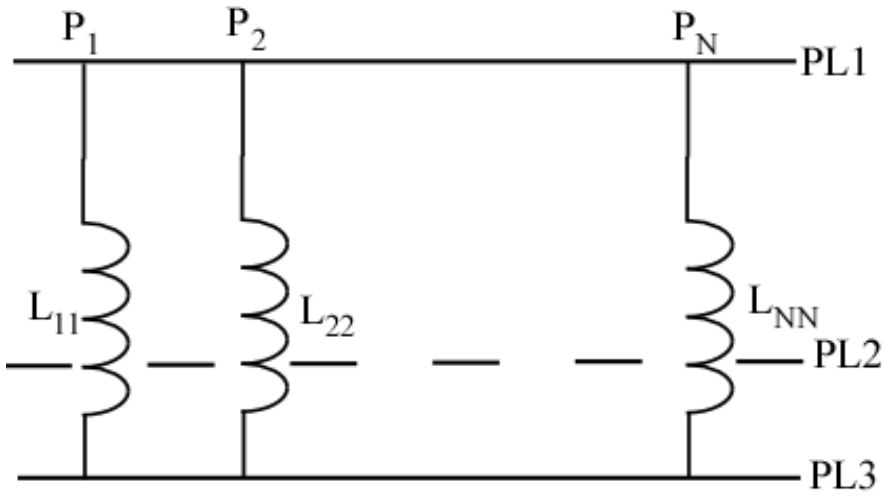
Resonance may occur



PDN design Strategy

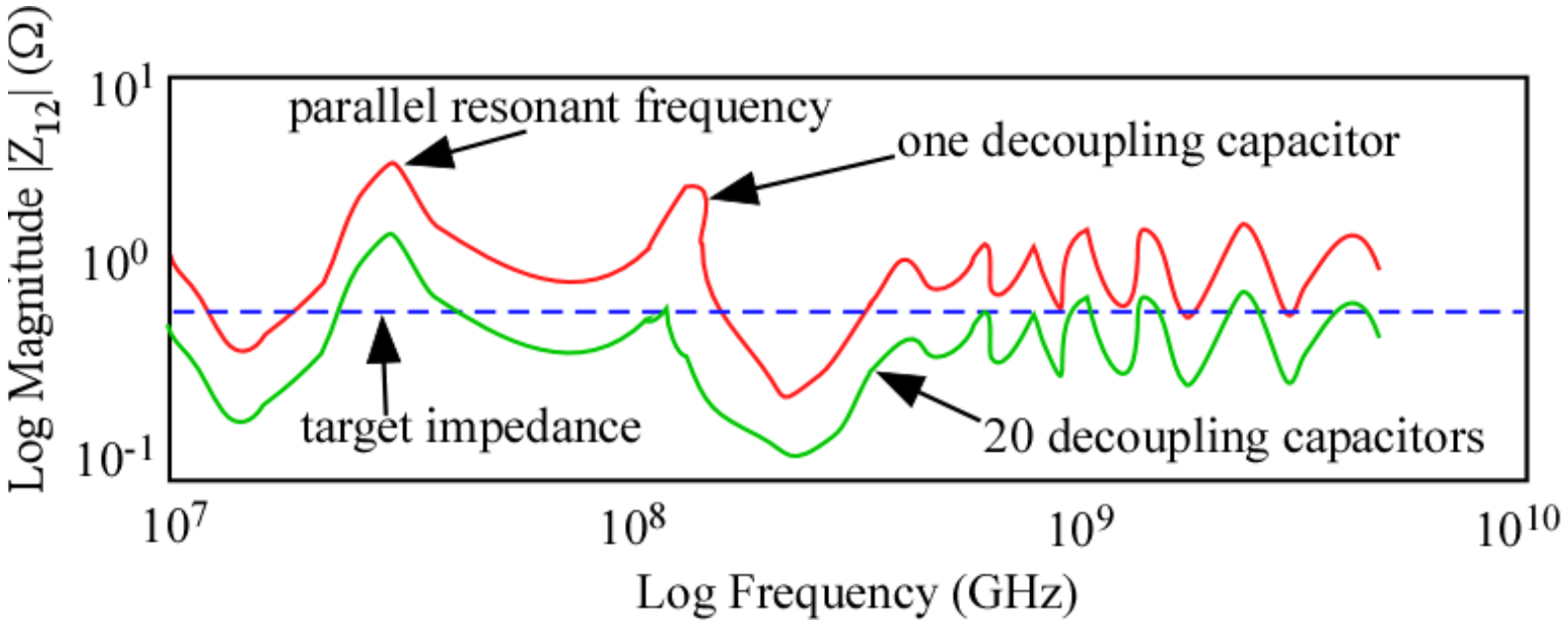
- Power/ground planes
  - Define unit cell and determine parameters
  - Synthesize complete circuit model
- Vias and via coupling
  - Incorporate vias as inductance
  - May or may not account for mutual inductance
- Decoupling Capacitors
  - Must determine optimal placement
- Impedance Calculations
  - SPICE
  - Transmission matrix
  - LIM

Vias and Via Coupling



Multiyared PDN can be represented as planes connected by vias. Many such vias are for reducing inductance and for thermal dissipation.

Decoupling Capacitors



Impedance Calculations

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} + R_1 + j\omega L_1 & Z_{12} \\ Z_{21} & Z_{22} + R_2 + j\omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

For an ideal power distribution network, the desired characteristics are zero self impedance and zero trans-impedance between ports at all frequencies

Target Impedance

The ratio of voltage to current must equal the impedance in the network

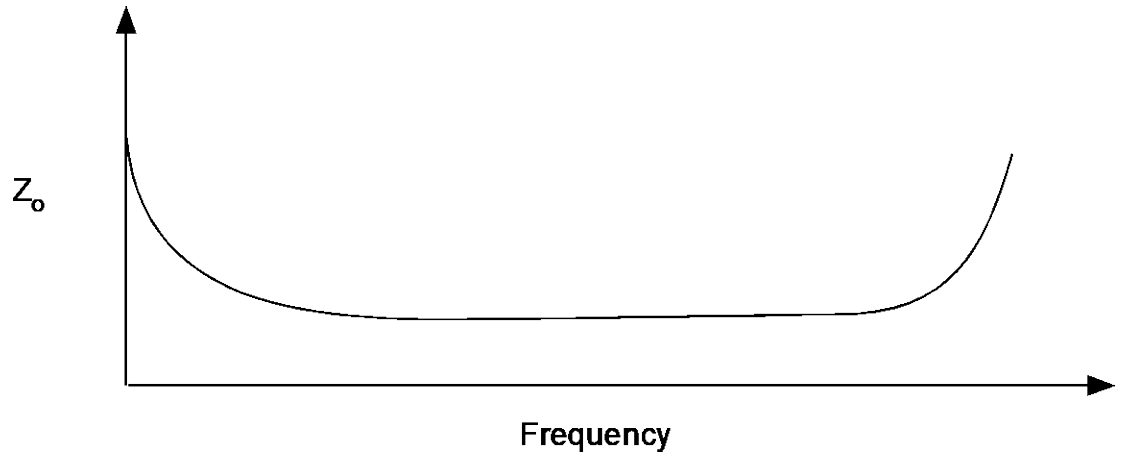
$$Z_T = \frac{V_{DD} \times ripple}{50\% \times I_{\max}}$$

V_{DD}: power supply voltage
ripple: allowed ripple on power supply
I_{max}: maximum current drawn by IC

- **The target impedance is a function of frequency. The goal is to keep it as low as possible.**

Impedance of Power Distribution Network

- **Influenced by Package and Bypass Cap**
  - Increase in low-frequency due to resonance frequency of board connector
  - Increase in the high-frequency impedance due to resonance frequency of decoupling capacitor
  - Keep both resonance frequencies away from operating frequency



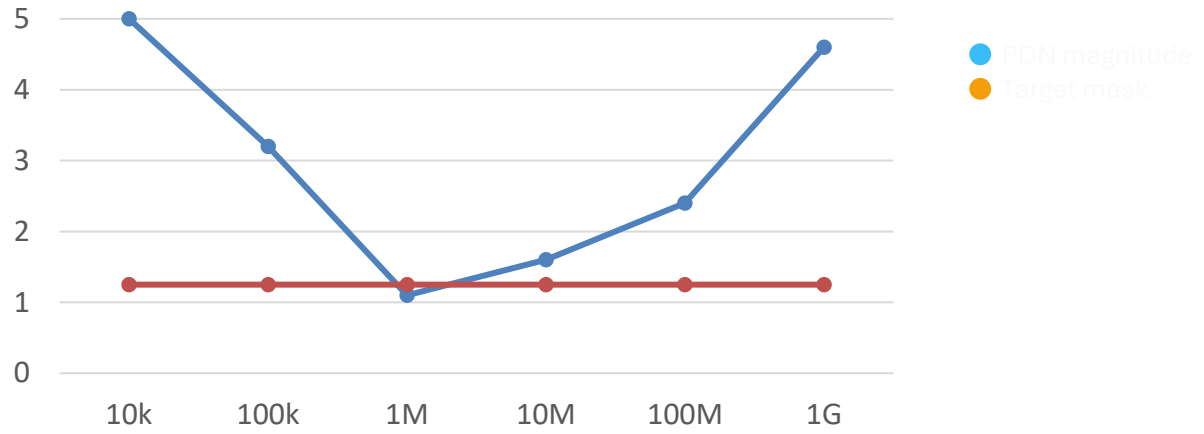
Target impedance

- For a rail with allowed ripple ΔV and transient current ΔI, the simplest requirement is Z_{target} = ΔV/ΔI.

- The design task is then to keep the die-side PDN impedance below that mask over the bandwidth that matters.

- This is a planning tool—not a substitute for spatial and time-domain analysis.

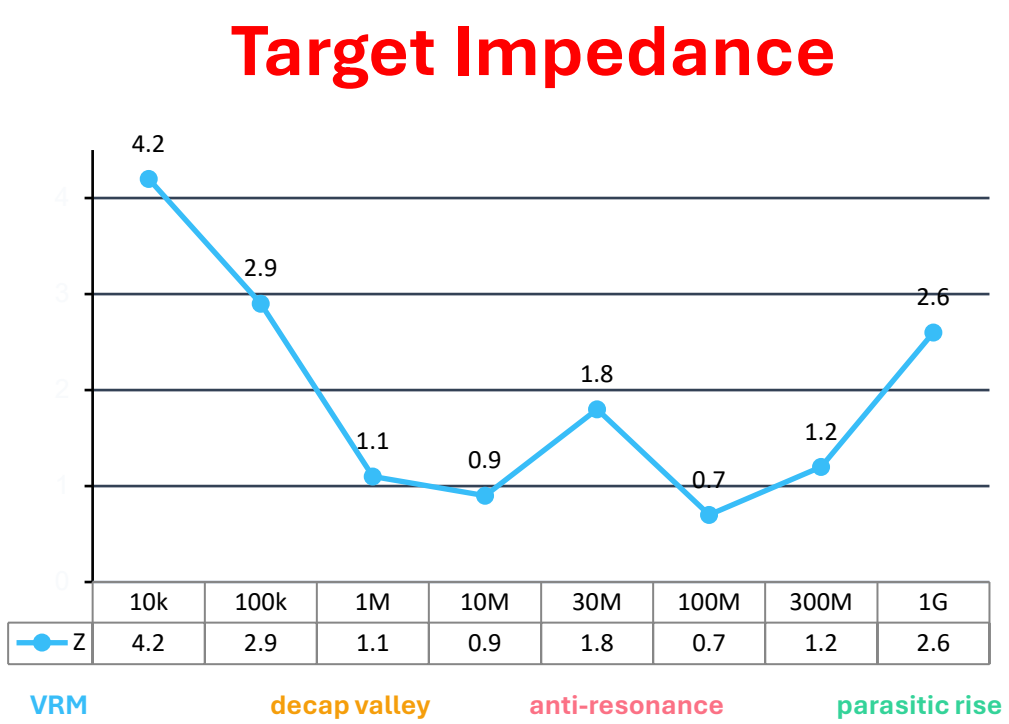
$$Z_{target} = \frac{\Delta V}{\Delta I}$$



Peak above the mask = likely droop / ringing problem

Frequency-Domain PDN Impedance Shaping

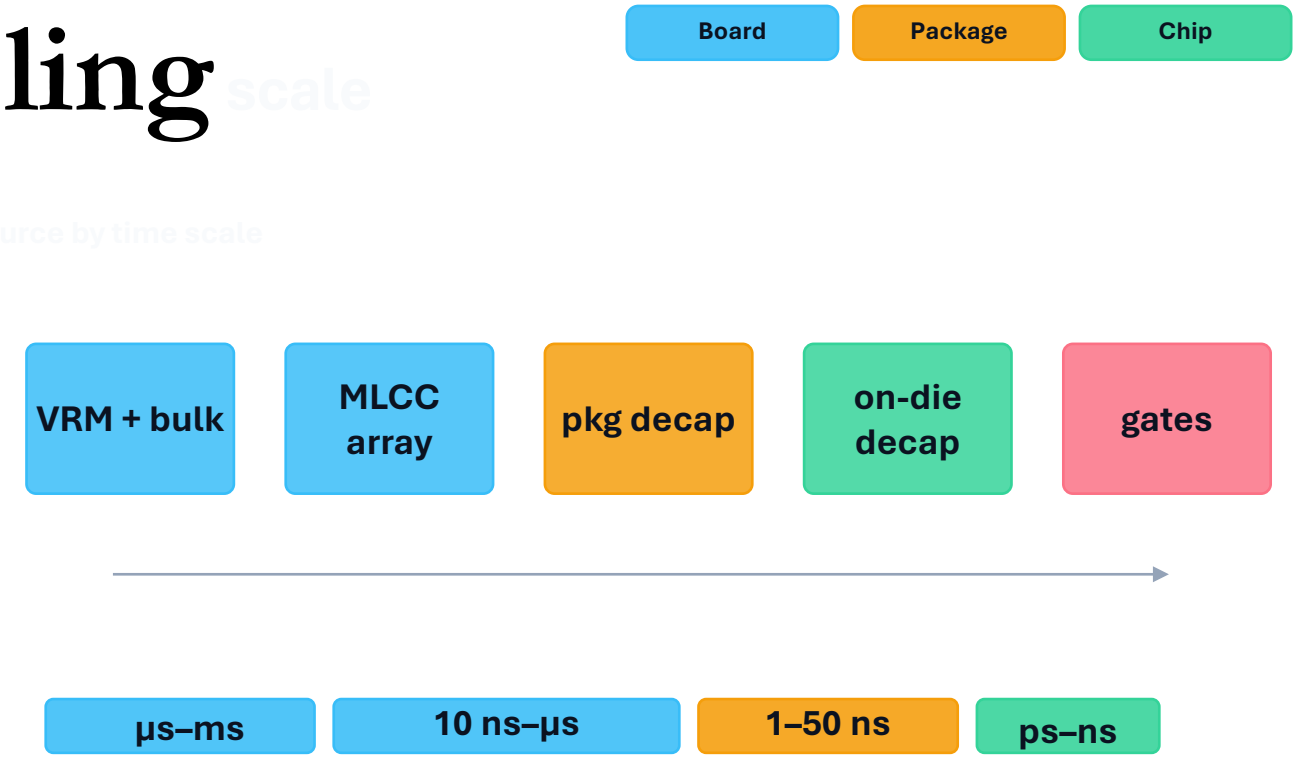
- Low frequency: VRM output impedance and load-line behavior dominate.
- Mid band: board and package decaps push impedance down—but can also create anti-resonance.
- High frequency: spreading, bumps, planes, and on-die resources dominate.



PI objective: flatten this curve at key observation points.

Hierarchical Decoupling

- Bulk capacitors and the regulator replenish energy over long windows.
- MLCCs handle the mid-band where the regulator is too slow but planes still help.
- On-package and on-die capacitance serve the shortest, highest-bandwidth demand.



The lower the inductance to the load, the later in the chain it must live.

Functions and Integration Levels

Board

- VRM bandwidth / load-line
- Plane shape and spreading
- Bulk + MLCC population
- Connector and return path

Package

- Bumps and escape routing
- Substrate/interposer inductance
- Package plane / cavity modes
- On-package decoupling

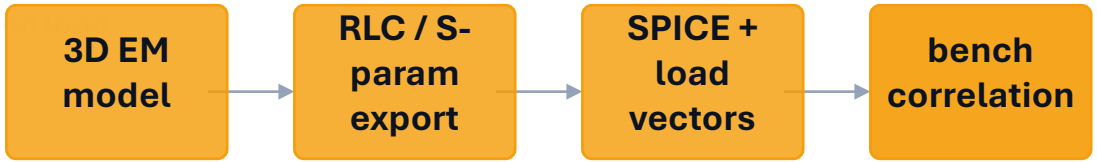
Chip

- Power grid topology
- Local decap placement
- Hotspot current density
- Static + dynamic signoff

PI closure works when each level owns a different part of the bandwidth and geometry problem.

Package modeling and measurement

- Package extraction is commonly delivered as broadband S-parameters or reduced RLC macromodels.



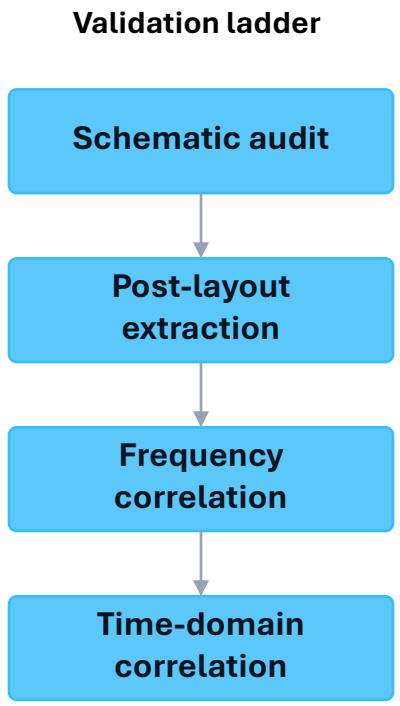
- The useful observation point is usually at the die bump / die pad side—not only at the PCB pads.

- Correlation needs both frequency-domain impedance and time-domain droop measurement.

Only after this loop is closed do capacitor and bump tradeoffs become trustworthy.

Board-level PI validation via Measurements

- Use a VNA for impedance / resonance characterization where fixtures permit.
- Use low-inductance probing and differential techniques for transient droop capture.
- Correlate measurement to the die-side observation point as closely as packaging allows.



Does the network make sense before layout?

Where are the real loop inductances?

Where are the peaks and valleys?

How deep is the actual droop?

EM + Circuit Co-Simulation Workflow

- Extract board and package geometry as broadband S-parameters or reduced RLC blocks.
- Combine S-parameters with regulator models, capacitor models, and ***chip current profiles*** in circuit simulation.
- Close the loop with VNA and transient measurements, then iterate ownership at the level that can actually fix the issue.

Use field solvers where geometry matters; use circuit simulation where design-space exploration matters.

Example: Power Delivery for Chiplets

Objectives

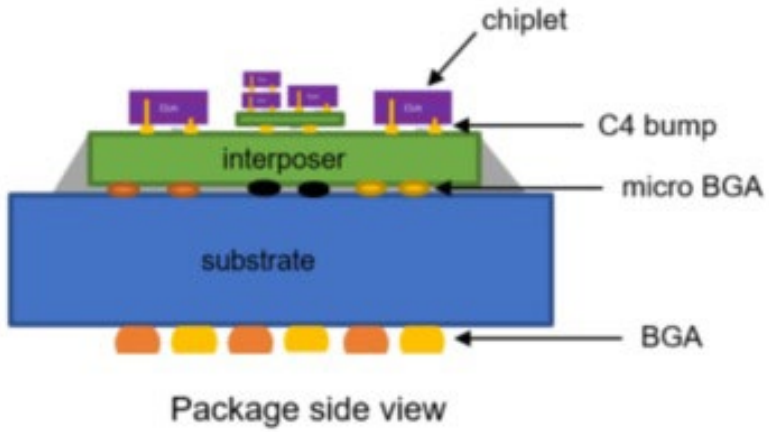
- Improve the efficiency of the power delivery to chiplets,
- Improve bandwidth and signal integrity

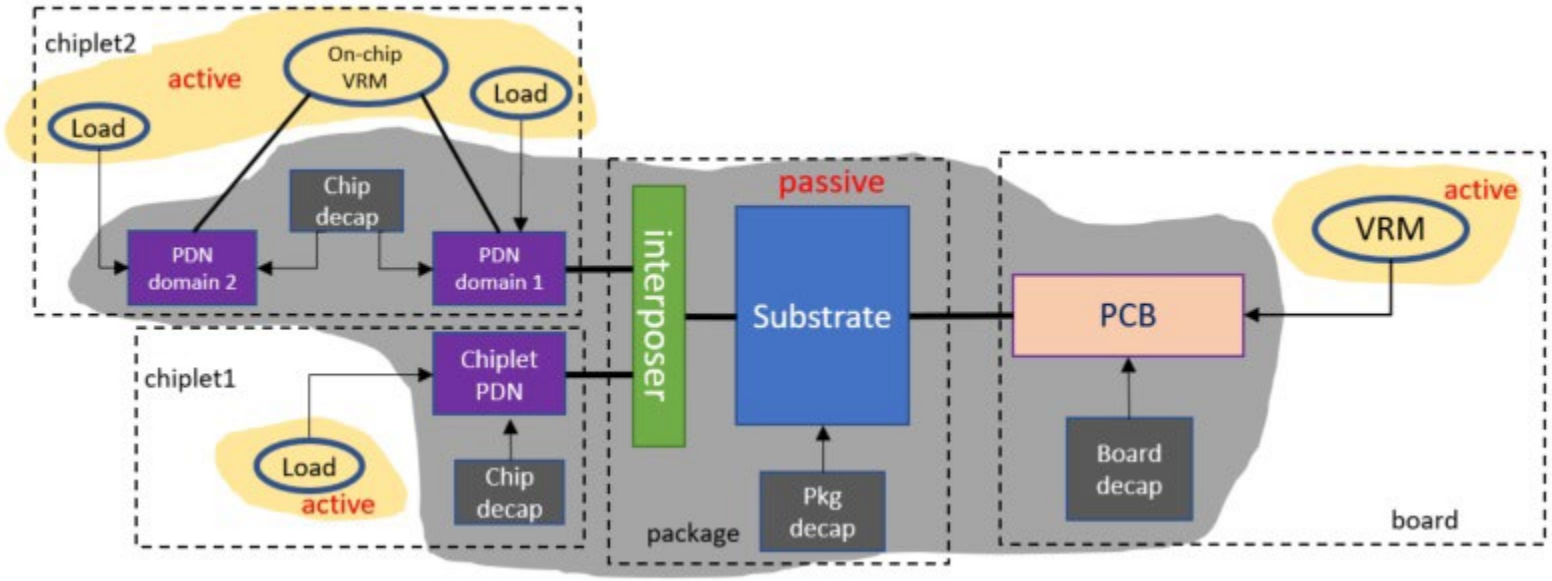
Co-Design Approach

- Modeling of Passive Power Delivery Network.
- Placement and Optimization of hierarchical decaps.
- Optimization of power/ground vias and number of planes to satisfy PDN requirements.
- Design and integration of active Power Conversion Circuits.

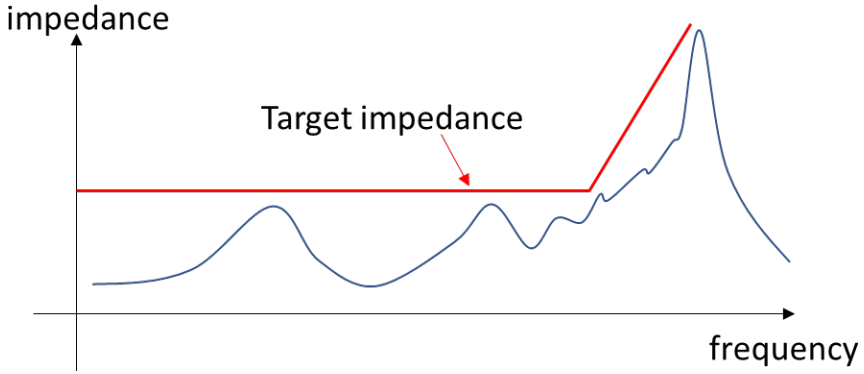
Power Delivery for Chiplet-Based SiP

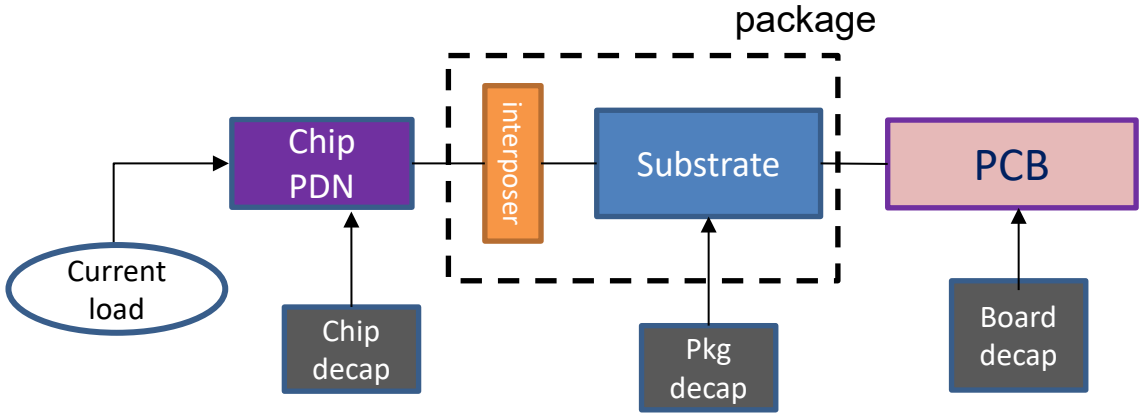
Chiplets must be positioned in their respective locations and provided with paths through the power distribution network. There can be multiple power domains. Package builder tools are used to automate the placement of vias, ball grid arrays and traces to the PDN. To mitigate supply voltage fluctuations decoupling capacitors (“decaps”) are placed on the PCB, package substrate, package interposer, and the silicon dies.

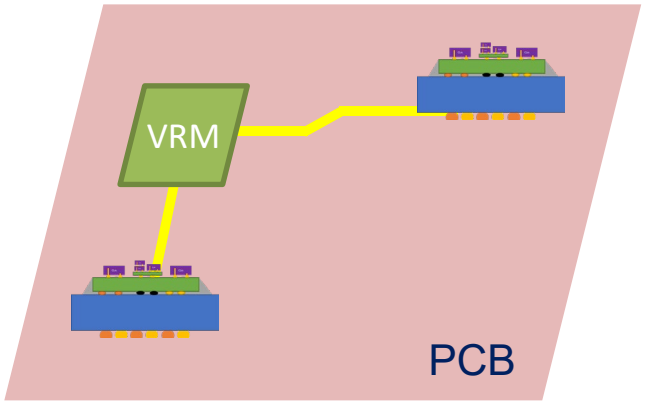


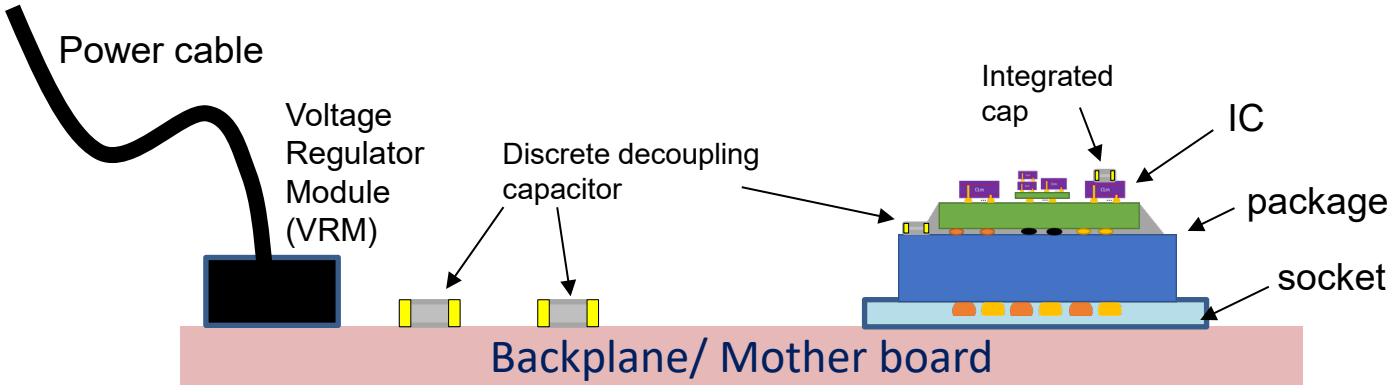


POWER DISTRIBUTION NETWORK (PDN) DESIGN





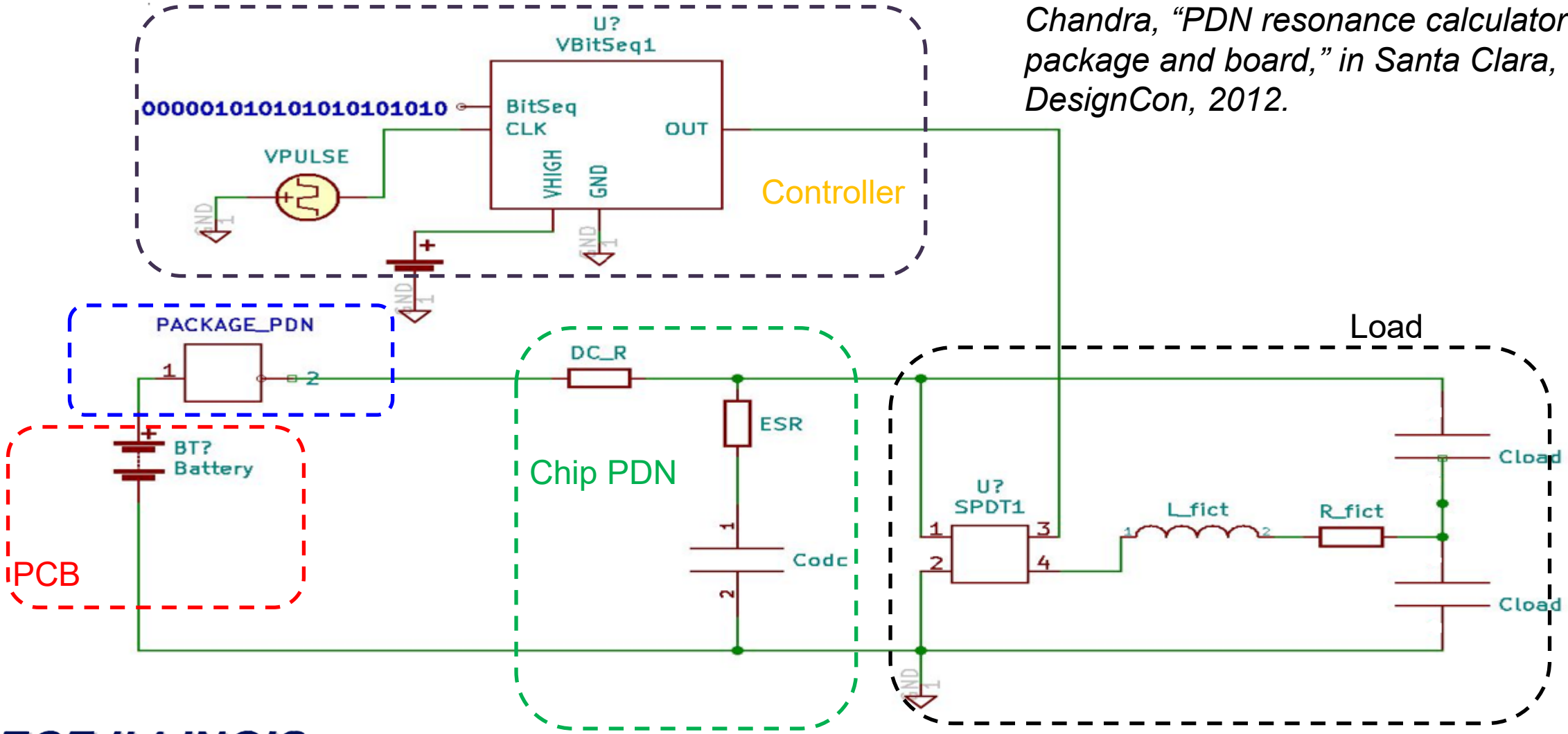




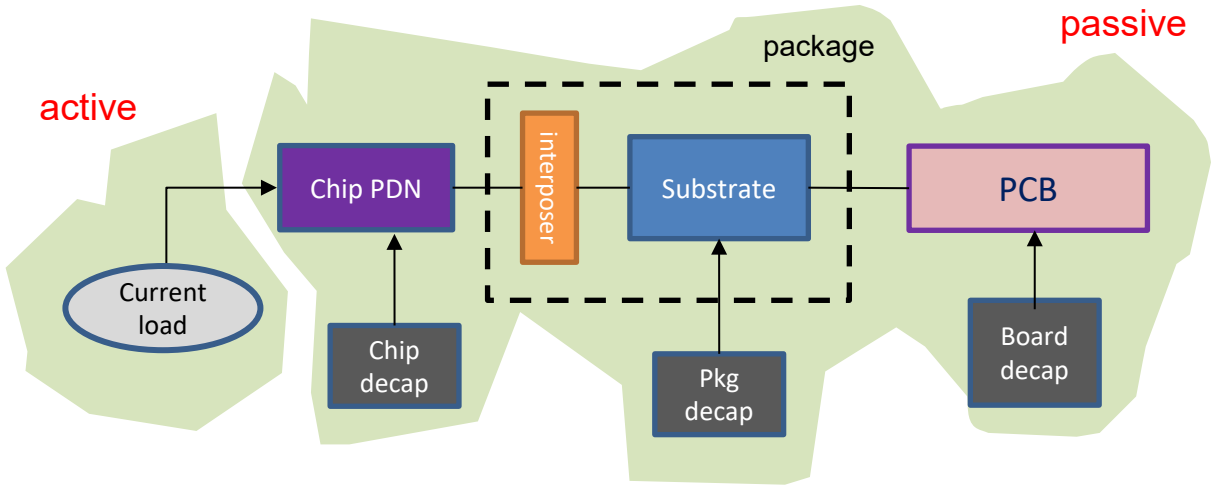
Goal: Achieve target impedance through use of decoupling capacitors at chip, package and board levels

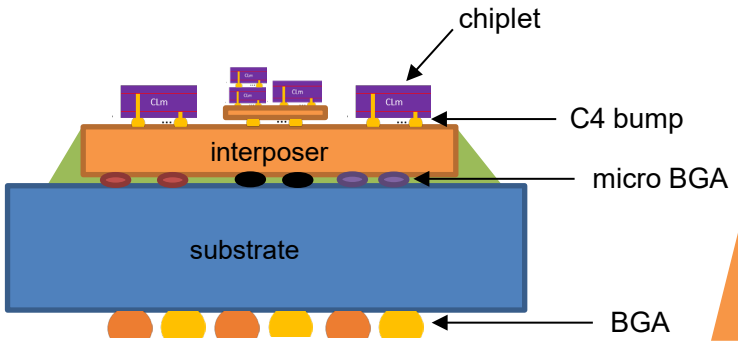
RECONFIGURABLE LOAD MODEL FOR A CHIPLET

Ref: *S. Smith, Larry Sarmiento, Mayra Tretiakov, Yuri Sun, Shishuang Li, and Zhe Chandra, "PDN resonance calculator for chip, package and board," in Santa Clara, CA, DesignCon, 2012.*

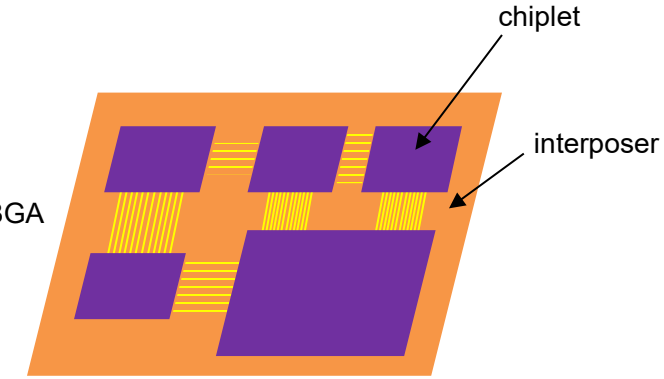


VALIDATION OF LOAD MODEL



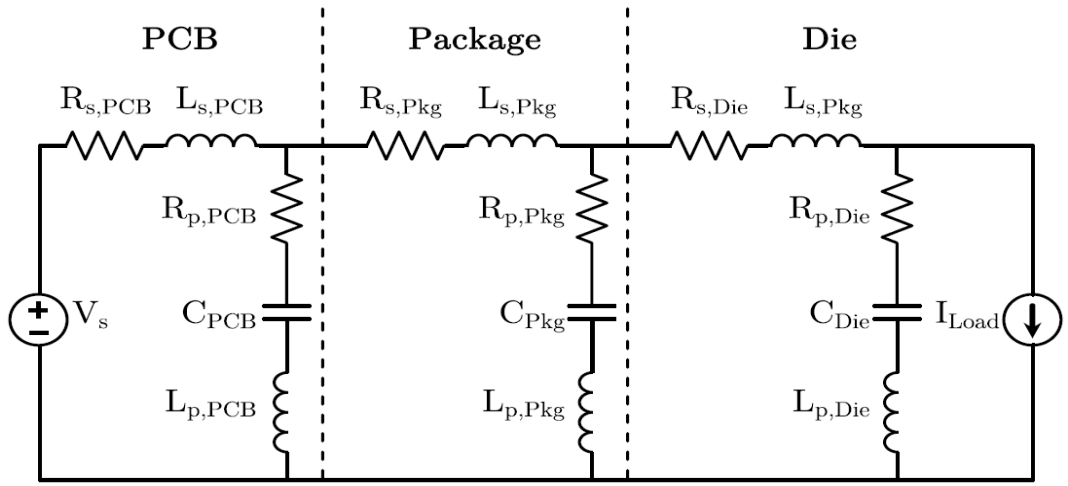


Package side view



Interposer top view

- Operation of the reconfigurable load model was validated.
- An off chip driver was laid out and driven through a clock signal.
- Generated current waveforms were generated and validated through on-chip voltages.
- Simulations were done in Cadence Virtuoso and Keysight ADS.



3 level hierarchical PDN

SYSTEM FOR PDN SIMULATION

Update configuration:
- Package design (geometry, bumps placement etc.)
- Power domain allocation
- Chiplet placements
- Decoupling
- etc.

Domain knowledge

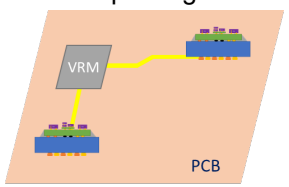
Decision making

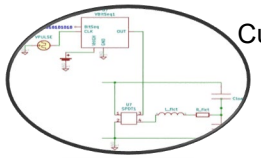
Feedback

Metric

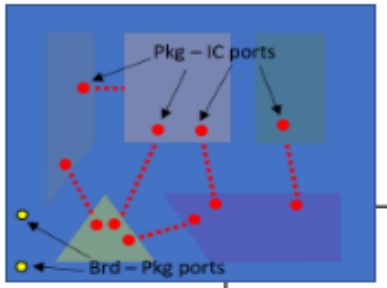
System level simulation

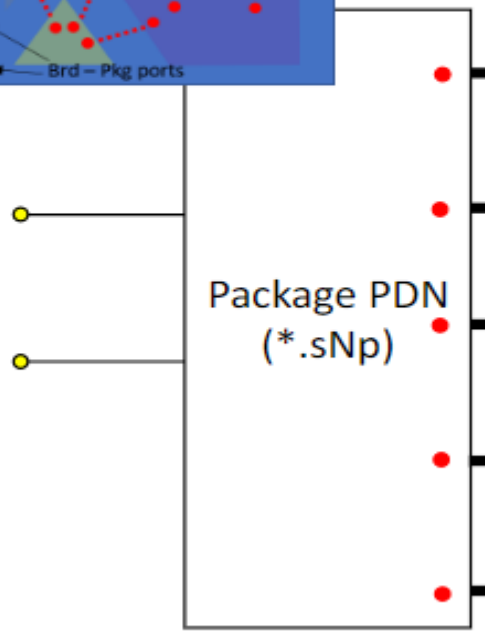
Board-package

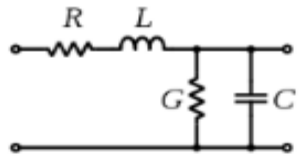




Current load



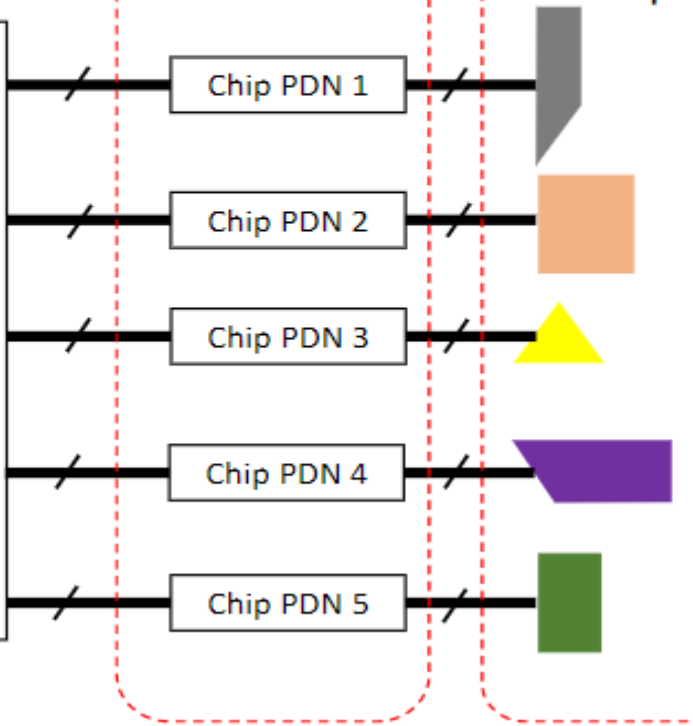




SPICE model
Load current waveform

Lumped RLGC

chiplet

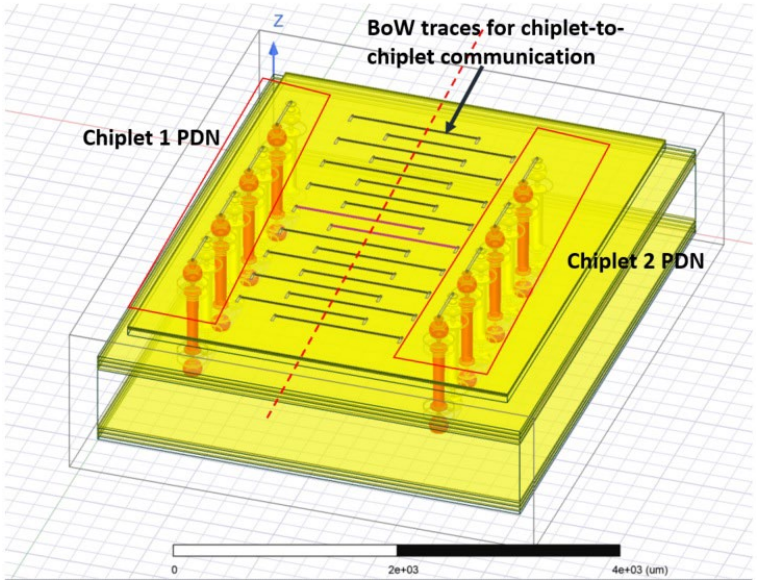


System level PDN assessment requires 2 components: a passive model for board – package – chip system PDN and an active model for chip power consumption (aka chip power model).

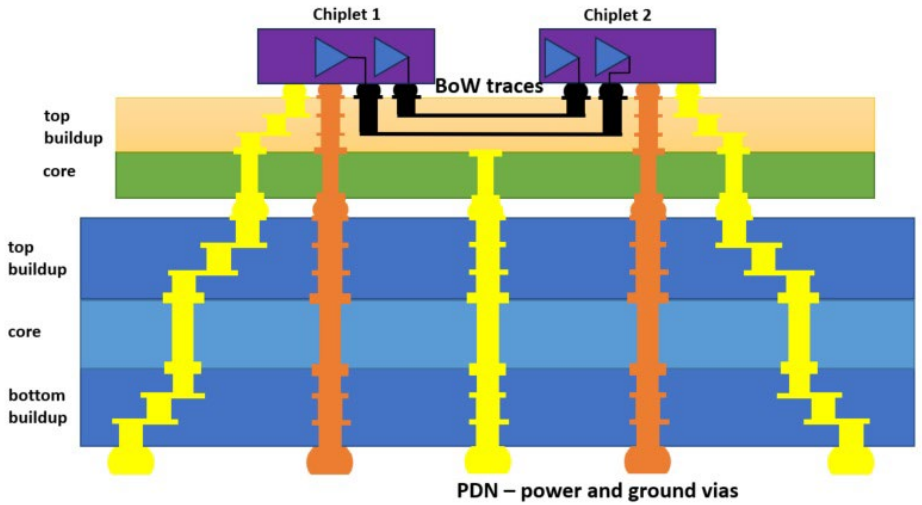
Power Delivery for Chiplet-Based SiP

Unlike chip-to-chip interconnects (Ucie/BoW) PDN interconnections must travel through several levels of integration which results in increase of complexity.

Top View



Cross-Section

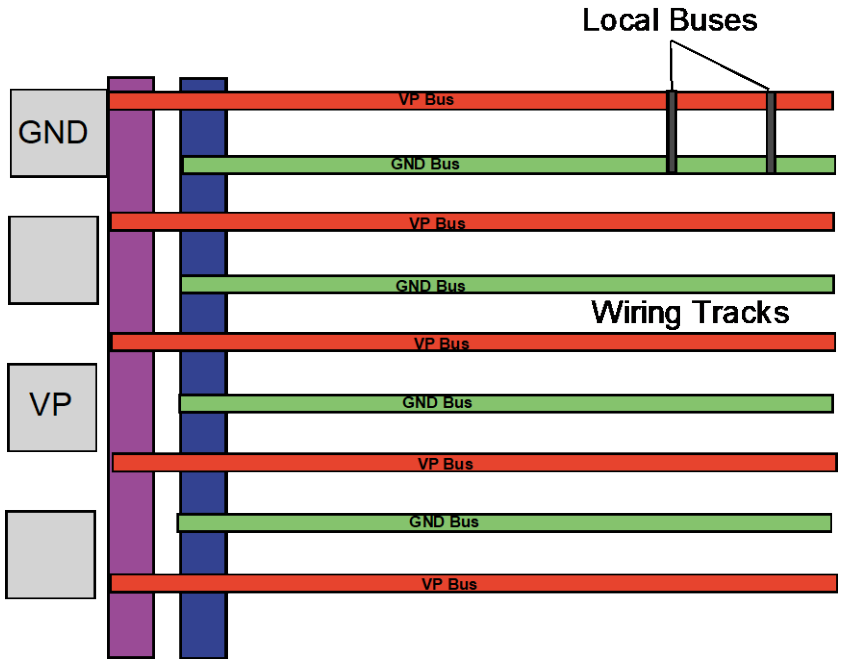


Chiplet-based design with PDN and D2D network

For 50 X 50 μBGA structure, extraction of network parameters takes more than a week!

On-Chip Power and Ground Distribution

- **Distribution Network for Peripheral Bonding**
  - Power and ground are brought onto the chip via bond pads located along the four edges
  - Metal buses provide routing from the edges to the remainder of the chip

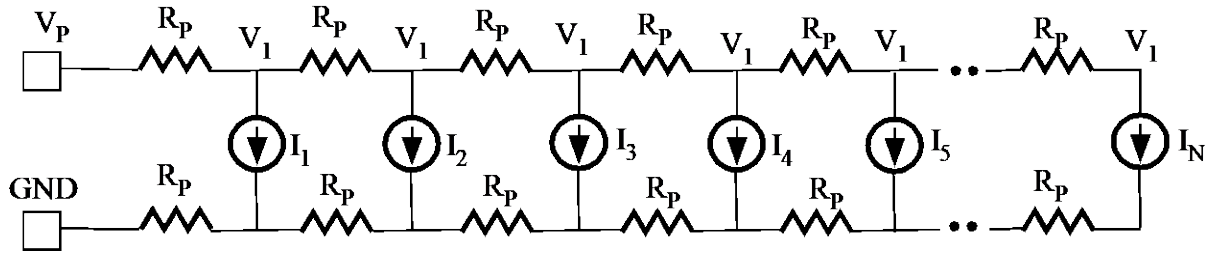


On-Chip IR Drop

- **Large Voltage Drop**
  - Example: V_{IR}=0.78V ➔ local supply down by 1.56V:unacceptable
  - Voltage drop across global buses is dependent only on the fraction of metal layer devoted to each bus

- **Remedy**
  - Use area bonded chip so that power need not be distributed from chip edge
  - Use more or thicker metal layers
  - Use on-chip bypass capacitors

Model for On-Chip Power Distribution



$$R_P = \frac{L_P r_w}{2NW_P} \qquad A_P = \frac{L_P W_P}{2Nk_P}$$

$$V_{IR} = \sum_{i=1}^{N/2} iJ_{pk} A_P R_P = \sum_{i=1}^{N/2} \frac{iJ_{pk} L_P^2 r}{4N^2 k_P}$$

in continuum,

$$V_{IR} = \int_0^{L_P/2} \frac{J_{pk} r_w x}{k_P} dx = \frac{J_{pk} r_w L_P^2}{8k_P}$$

r_w : resistivity

N : # of segments

A_P : Area

k_P : fraction of metal layer devoted to power buses

IR Drop - Example

Design a power distribution network for a peripherally bonded ASIC. Your chip is 15 mm × 15 mm in area and contains 1M gate equivalents. Each gate equivalent drives a 200-fF load (40 fF of gate and 160 fF of wire) and switches on average every third cycle of a 100MHz clock. What is the total power dissipation of your chip? Assuming a peak current to average current ratio of 4:1, what fraction of a metal layer (or how many metal layers) do you need to distribute power so the overall supply fluctuation of a 2.5V supply is ± 250 mV?

$$I_{avg} = C\frac{dV}{dt} = \frac{1}{3} * 1M * 200\,fF * 2.5V * 100MHz = 16.67\ A$$

$$J_{avg} = I_{avg} / (15mm)^2 = 0.0740\,A / mm^2$$

$$J_{peak} = 4J_{avg} = 0.296\,A / mm^2$$

IR Drop

Therefore, the number of metal layers is

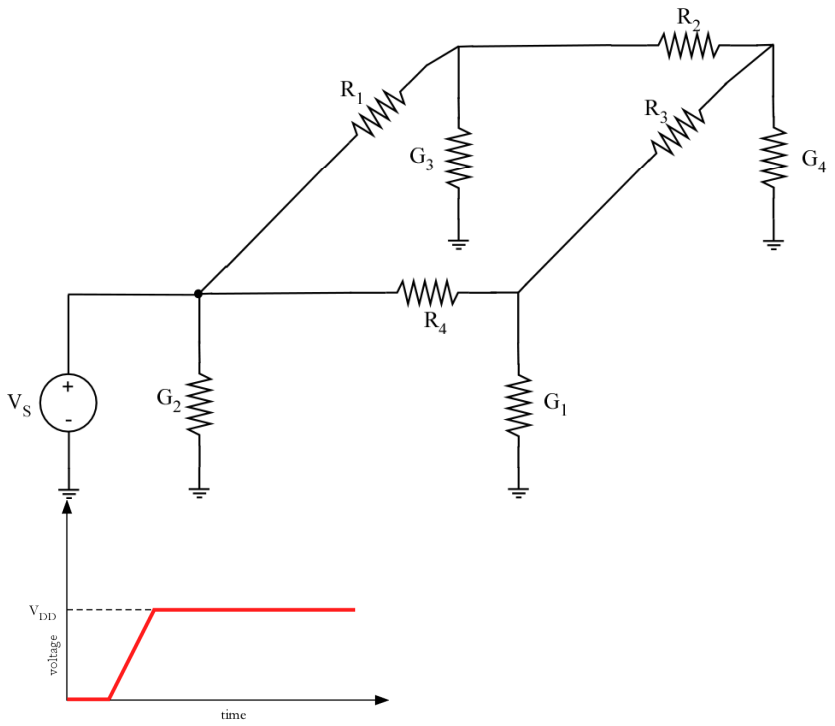
$$K_p = \frac{r_W \cdot L^2 \cdot J_{peak}}{8 \cdot V} = \frac{0.04 \cdot (15)^2 \cdot 0.296}{8 \cdot 0.25} = 1.332$$

If actual supply fluctuation is between Gnd and Vdd, each layer has less than ± 125mV fluctuation. Therefore, for each Gnd and Vdd,

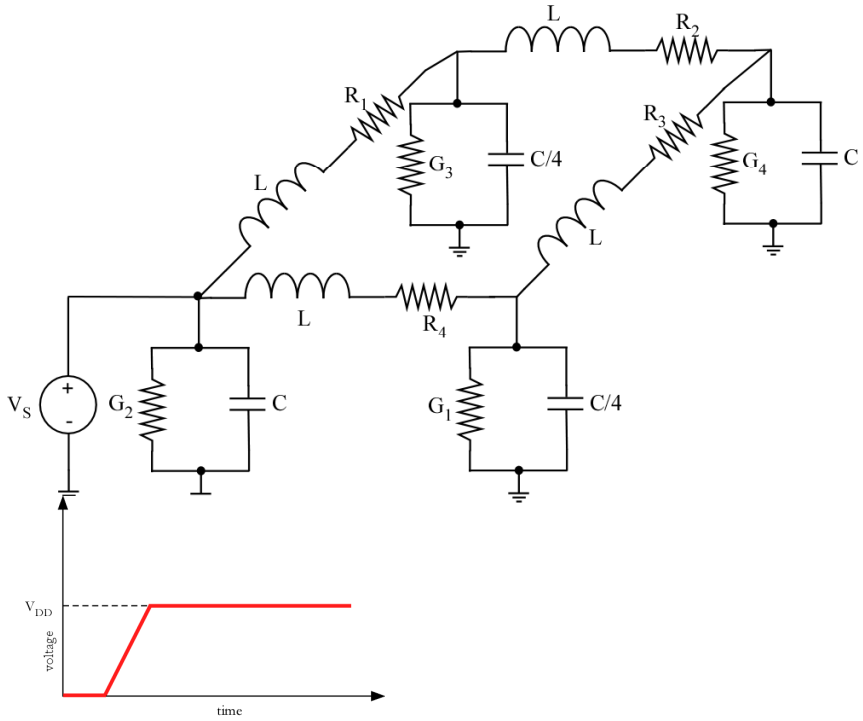
$$K_p = \frac{r_W \cdot L^2 \cdot J_{peak}}{8 \cdot V} = \frac{0.04 \cdot (15)^2 \cdot 0.296}{8 \cdot 0.125} = 2.664$$

IR Drop Calculation

Circuit A



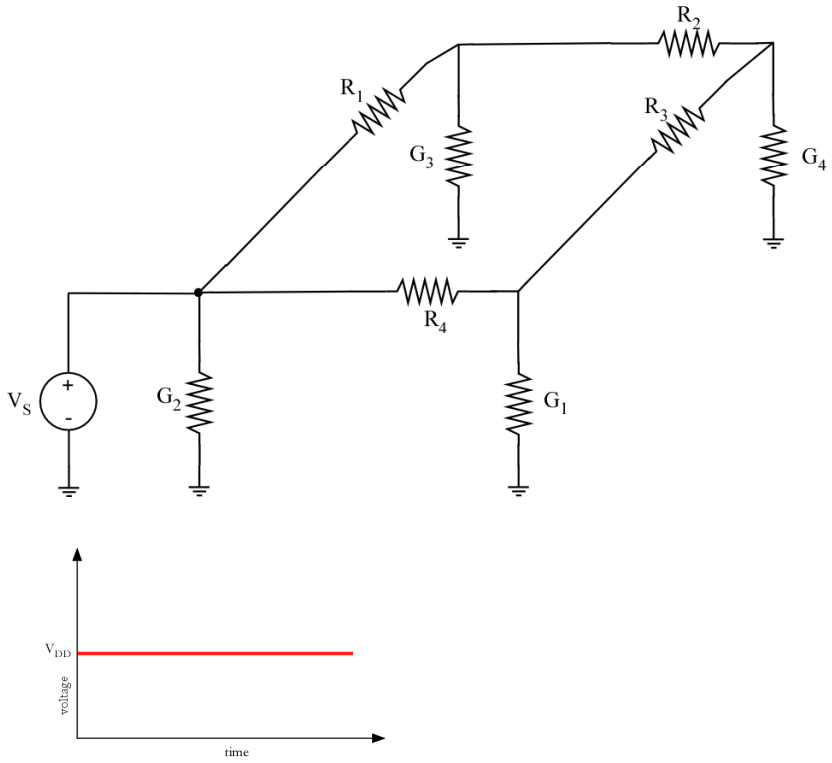
Circuit B



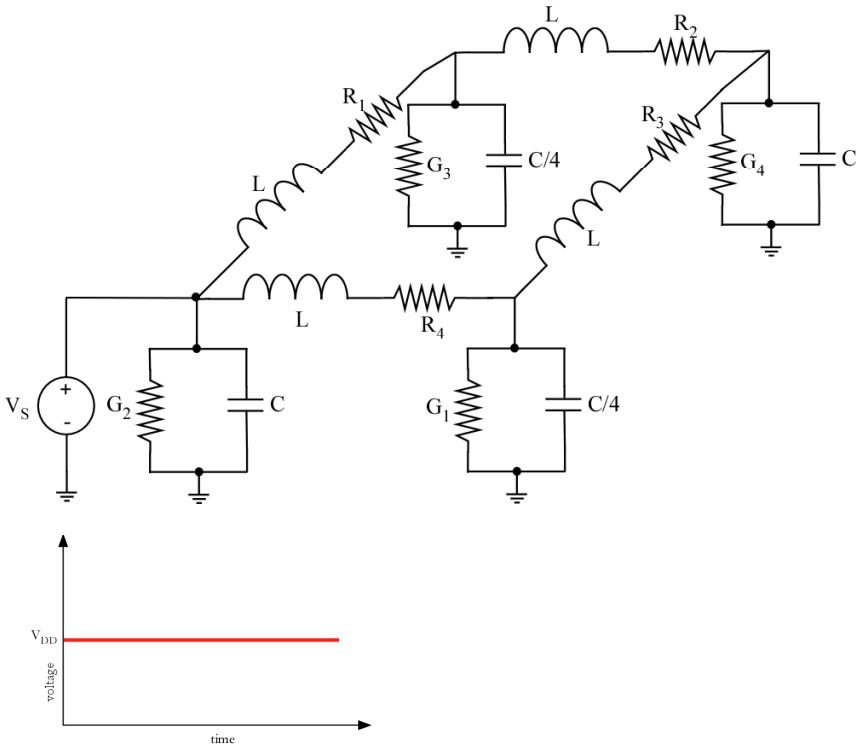
Circuit A and Circuit B will have different transient response to step excitation. However, their solutions for very large time will be same

IR Drop Calculation

Circuit A



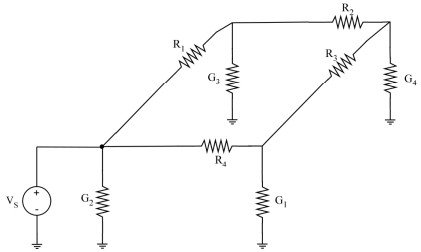
Circuit B



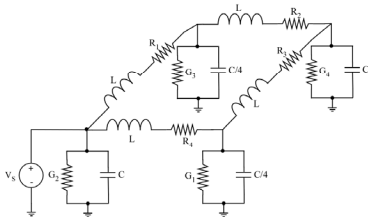
Circuit A and Circuit B have the same DC solution

IR Drop Computation

Circuit A



Circuit B

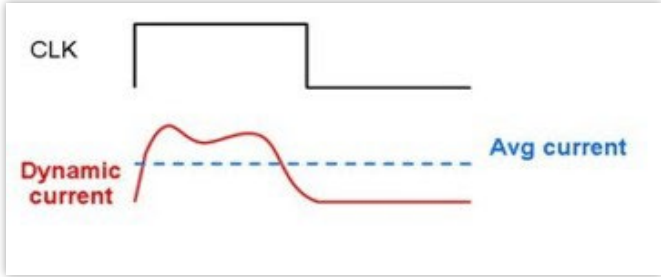


Proposition: In order to find the DC solution for Circuit A, we perform a LIM transient simulation on Circuit B and use the response for large time as the DC solution for Circuit A

For large networks this is FASTER than MNA solution

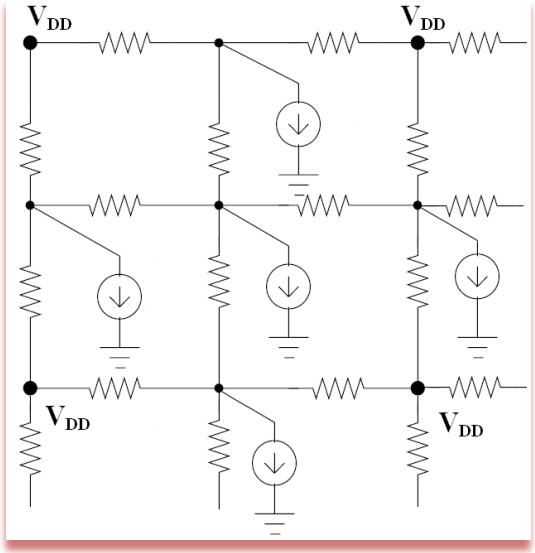
Analysis of a Power Distribution Network

- Analysis of a PDN → two types:
  - Steady state (DC) analysis
  - Dynamic (Transient simulation)



- Capacitors → open-circuited
- Inductors → short-circuited
- Power sources→ ideal voltage sources
- Power drains → constant current sources

- Transient Simulation
  - Effects of capacitance and inductance are taken into account
  - Time-varying (switching) current sources

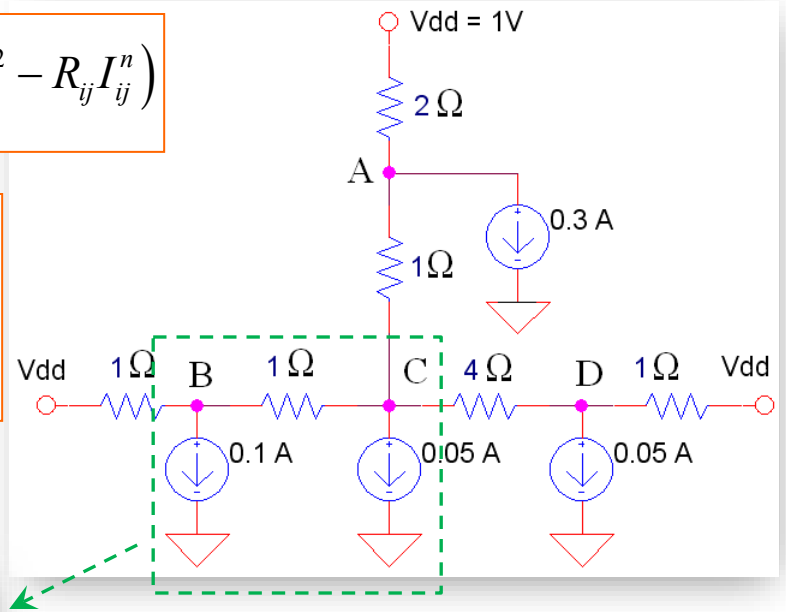


Circuit model for a steady state power grid

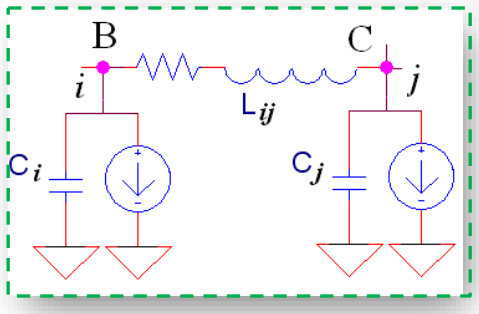
Steady State - Example

$$I_{ij}^{n+1} = I_{ij}^{n} + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^{n}\right)$$

$$V_i^{n+1/2} = \frac{\dfrac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \sum_{k=1}^{N_a} I_{ik}^n}{\dfrac{C_i}{\Delta t} + G_i}$$



Basic circuit example



Modified segment of the basic circuit with latency elements inserted

Steady state →

- capacitances are open- circuited
- inductances are shorts-circuited

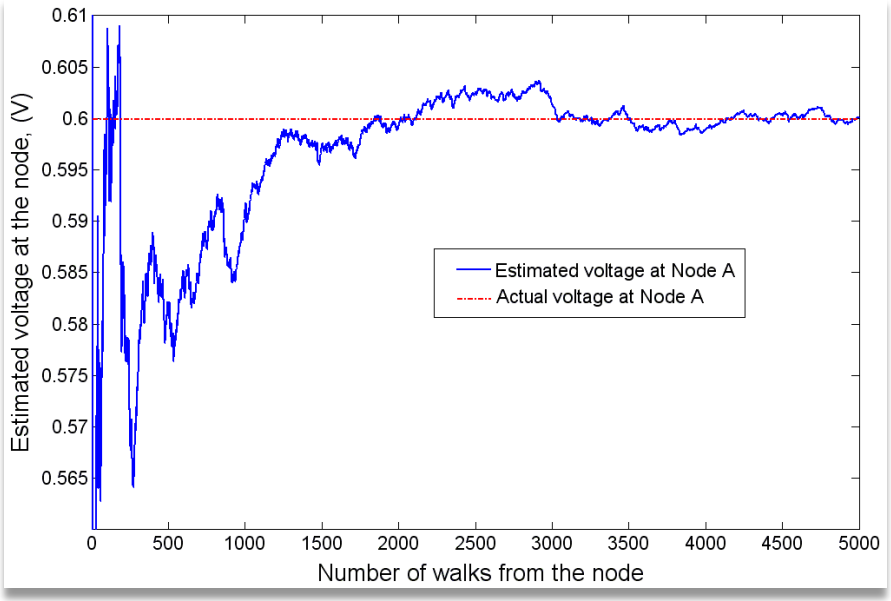
Node	Node voltage (V)
A	0.6
B	0.8
C	0.7
D	0.9

LIM requires latency elements →

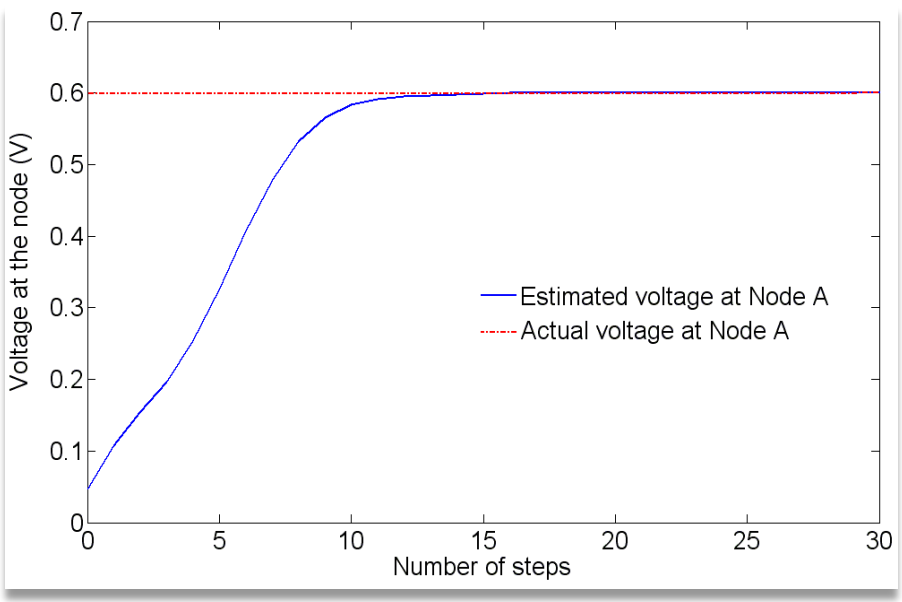
- small shunt capacitances must be added at all non-Vdd nodes
- small inductances must be inserted in all branches
- all latency is purely fictitious → there is no limit on the value of inserted latency

Convergence of the Simulation

Random Walk



LIM



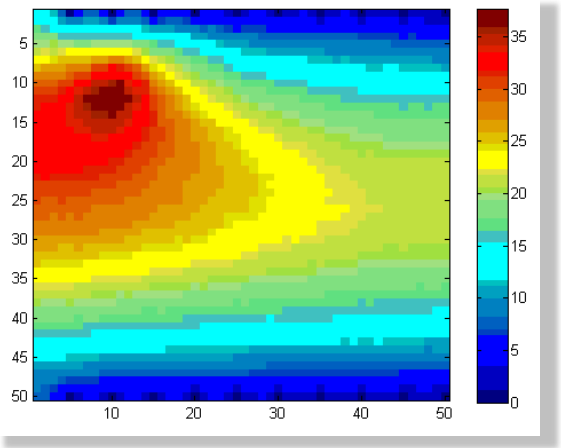
Node	Estimated voltage (V) (random walk)	Estimated voltage (V) (LIM)	Actual voltage (V) at the node
A	0.600140	0.600007	0.6
B	0.803245	0.800009	0.8
C	0.700986	0.700010	0.7
D	0.903905	0.900013	0.9

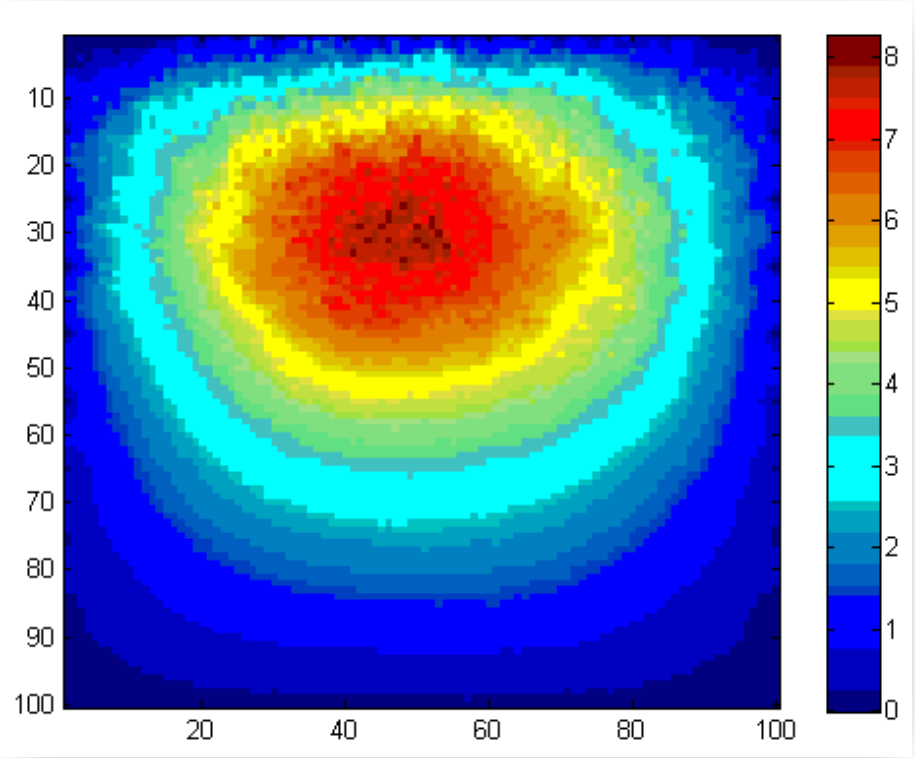
LIM simulation demonstrates fast convergence and allows to achieve high accuracy

Numerical Results

- Runtimes of the LIM simulations were compared to the ones of the Random-Walk method for several large circuits [7]

Number of nodes	Runtime (CPU sec) (LIM)	Runtime (CPU sec) (Random-Walk)
10 K	< 1	10
250 K	3	258
500 K	6	509
1 M	13	1126
2 M	28	2528





IR drop profile.
Color scale shows the percentage change of the supply voltage relative to Vdd

[7] D. Klokotov, P. Goh, and J. E. Schutt-Ainé, "Latency Insertion Method (LIM) for DC Analysis of Power Supply Networks," *IEEE Trans. Advanced Packaging,* in press