ECE 546
Lecture - 21
Noise in Digital Circuits

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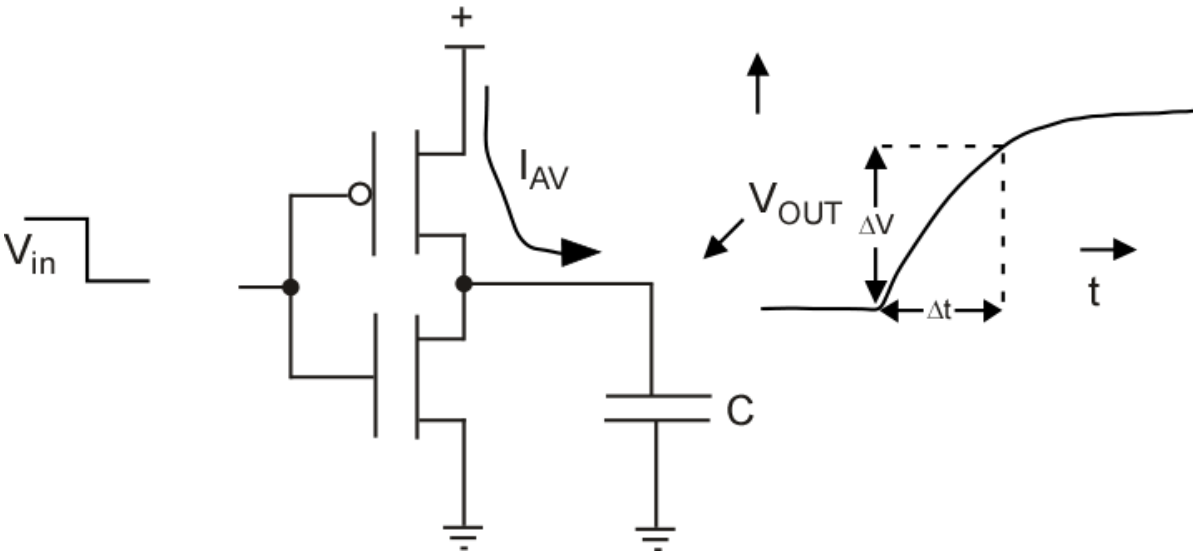
Circuit Delay



$$\Delta t = \frac{C\Delta V}{I_{av}}$$

To optimize circuit performance, the goal is to reduce the capacitive loading C and potential swing ΔV while keeping the average current drive I_{av} high

Scaling of Transistors

- When scaling is applied (scaling factor S >1)
  - All horizontal and vertical dimensions of transistors are scaled down
  - Substrate doping is increased by S
  - All voltages are reduced by 1/S

Scaling of Transistors

Drain Current

$$I_{DS} = \mu C_{ox} \frac{W}{2L}\left(V_{GS} - V_T\right)^2$$

$$I_{DS} \propto 1 \times S \times \frac{1/S}{1/S} \times \left(1/S\right)^2 = \frac{1}{S}$$

Time Delay

$$\tau = \frac{C_g \Delta V}{I_{av}}$$

$$\tau \propto \frac{1/S \times 1/S}{1/S} = \frac{1}{S}$$

Capacitance

$$C_g = WLC_{ox}$$

$$C_g \propto \frac{1}{S} \times \frac{1}{S} \times S = \frac{1}{S}$$

Power

$$P = IV$$

$$\propto \frac{1}{S} \times \frac{1}{S} = \frac{1}{S^2}$$

Ideal Scaling of Transistors

Dimensions (W, L, t_{gox}, X_j)	1/S
Substrate doping (N_{SUB})	S
Voltages (V_{DD}, V_{TN}, V_{TP})	1/S
Current per device (IDS)	1/S
Gate capacitance ($C_g = \varepsilon_{ox} WL/t_{gox}$)	1/S
Transistor on-resistance	1
Intrinsic gate delay($\tau = R_{tr} C_g$)	1/S
Power-dissipation per gate ($P = IV$)	$1/S^2$
Power-delay product per gate ($P \times \tau$)	$1/S^3$
Area per device ($A = WL$)	$1/S^2$
Power-dissipation density (P/A)	1

S: Scaling factor for device dimensions.

Optimal Chip Size

- **Delay Factor**
  - On-chip delay is usually kept much smaller than chip-to-chip delay
  - Choose chip delay to be 10% of chip-to-chip delay

- **Optimal**
  - If the chips are made larger, the system will become slower
  - If the chips are made smaller, the complexity of the package will increase

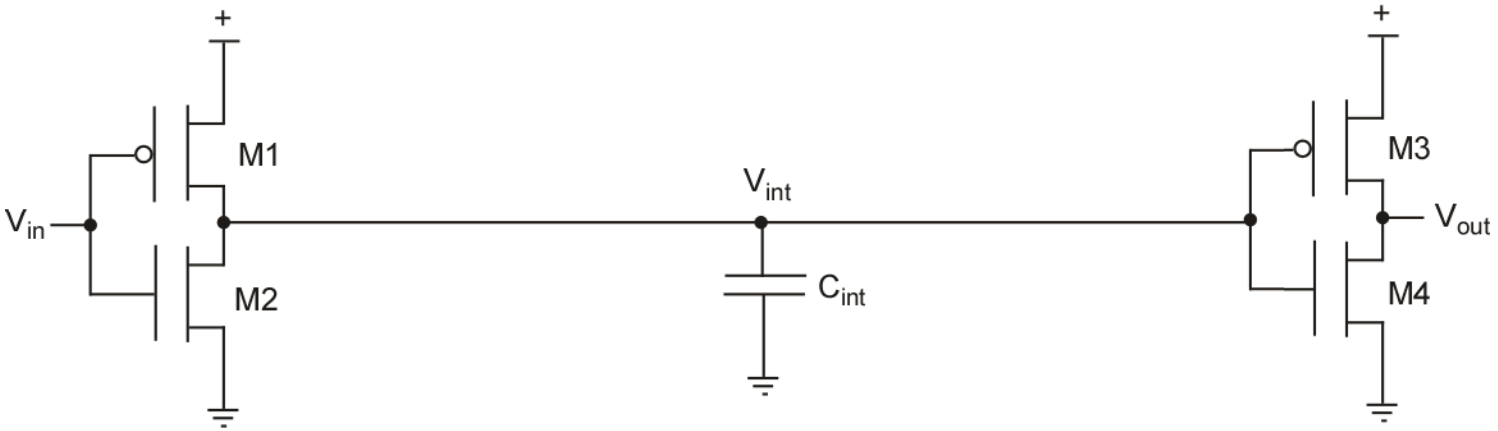
$$\sqrt{A_{chip}} = 0.16\sqrt{\frac{R_o C_o}{R_{chip} C_{chip}}} \ln\left(\frac{C_{pack}\sqrt{A_{package}}/2 + C_L}{C_o}\right)$$

$A_{chip} : Area\ of\ chip$

$A_{package} : Area\ of\ package$

Scaling of Interconnection Capacitance

- **Wiring Capacitance vs Device Capacitance**
  - Wiring capacitance becomes more important
  - Transistor input capacitance decreases with reduced size
  - Capacitance of chip-to-chip wire is an order of magnitude larger than on-chip capacitance



Scaling of Interconnection Capacitance

$$T_{50\%} = R_{tr}(C_{int} + C_{gate})$$

$$R_{tr} \approx \frac{1}{\frac{W}{L}\mu C_{gox}(V_{DD} - V_T)} \propto 1$$

$$C_{gate} = \varepsilon_{ox}\frac{W_n L_n + W_p L_p}{t_{gox}} \propto 1/S$$

$$C_{int} = \varepsilon_{ox}\frac{W_{inxt} l_{int}}{t_{ox}} \propto S_C$$

Scaling of Local Interconnections

Parameter	Ideal	Quasi-Ideal	Constant-R	Generalized
Thickness (H_{int})	1/S	$1/S^{1/2}$	$1/S^{1/2}$	$1/S_H$
Width (W_{int})	1/S	1/S	$1/S^{1/2}$	$1/S_w$
Separation (W_{sp})	1/S	1/S	$1/S^{1/2}$	$1/S_{sp}$
Insulator thickness	1/S	$1/S^{1/2}$	$1/S^{1/2}$	$1/S_{ox}$
Length (l_{loc})	1/S	1/S	1/S	1/S
Resistance (R_{int})	S	$S^{1/2}$	1	S_wS_H/S
Capacitance to subst	1/S	$1/S^{3/2}$	1/S	S_{ox}/SS_w
Capacitance between lines	1/S	$1/S^{1/2}$	1/S	S_{ox}/SS_H
RC delay (T)	1	$1/S^{1/2}$	1/S	S_wS_H/S^2
Voltage drop (IR)	1	$1/S^{1/2}$	1/S	S_wS_H/S^2
Current density (J)	S	$S^{1/2}$	1	S_wS_H/S

S: Scaling factor for device dimensions.

Scaling of Global Interconnections

Parameter	Ideal Scaling	Constant Dimension	Constant Delay	Generalized Scaling
Thickness (H_{int})	1/S	1	S_C	$1/S_H$
Width (W_{int})	1/S	1	S_C	$1/S_w$
Separation (W_{sp})	1/S	1	$1/S^{1/2}$	$1/S_{sp}$
Insulator thickness (t_{ox})	1/S	1	S_C	$1/S_{ox}$
Length (l_{int})	S_C	S_C	S_C	S_C
Resistance (R_{int})	S^2S_C	S_C	$1/S_C$	$S_wS_HS_C$
Capacitance (C_{int})	S_C	S_C	S_C	$\sim S_C$
RC delay (T)	$S^2S_C^2$	S_C^2	1	$S_wS_HS_C^2$

S: Scaling factor for device dimensions.
S_C: Scaling factor for chip size

Scaling of IR Voltage Drops

Parameter	Ideal scaling	Improved Scaling
Total chip current	$S^2S_c^2$	$S^2S_c^2$
Conductor thickness	$1/S$	S
Sheet resistance (R_{int})	S	$1/S$
Number of power planes	1	S
Number of power connections	1	SS_C^2
Effective resistance	S	$1/S^3S_C^2$
IR voltage drop	$S^3S_C^2$	$1/S$
Signal-to-noise ratio	$1/S^4S_C^2$	1

S: Scaling factor for device dimensions.
S_C: Scaling factor for chip size

Effect of Scaling on Signal-to-Noise Ratio

Signal-to-noise (S/N) ratio is reduced by: $S^4 S_C^3$

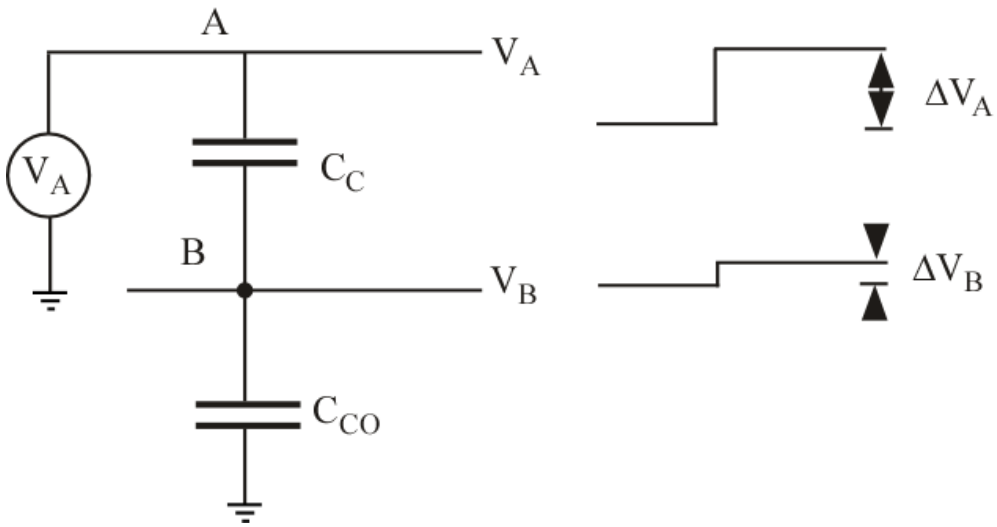
This is an alarming ratio

- **Severity is reduced by**
  - Off-chip wires have larger inductance
  - Their current demand does not increase as fast
  - Their large size allow easy decoupling
  - In general off-chip transients are slower
  - TAB and flip-chip technology can improve

Different Types of Crosstalk

- **Crosstalk Between Capacitive Lines**
  - Primarily on chip
  - Major effect is increase in delay
- **Crosstalk Between Transmission Lines**
  - Distributed and wave effects
  - Approximate as near and far end crosstalks
- **Signal return Crosstalk**
  - Imperfect ground reference
  - Unbalanced currents

Coupling to Floating Line

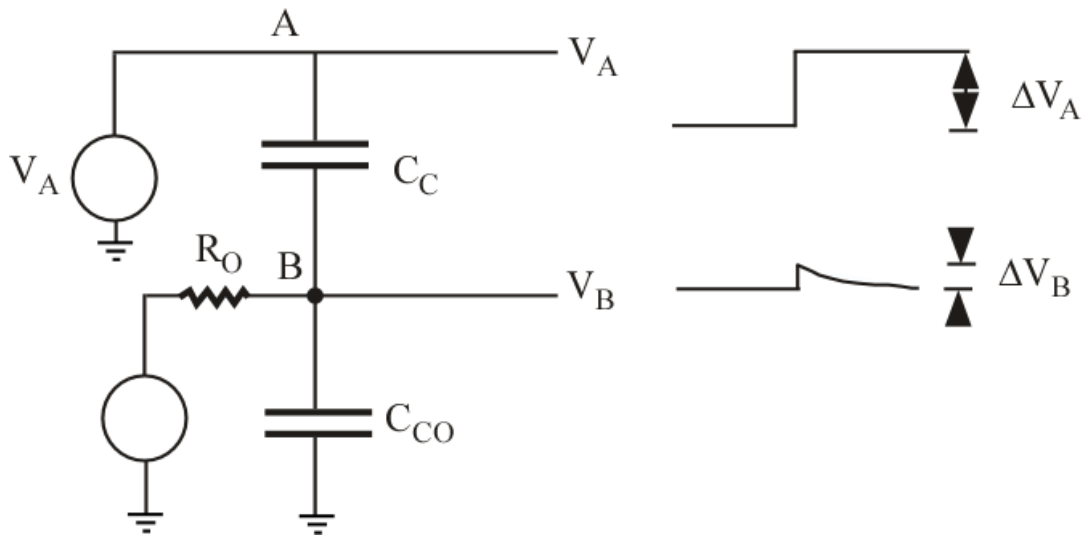


– Important when high-swing signal passes near a low-swing pre-charged signal (e.g. RAM)

$$k_c = \frac{C_C}{C_O + C_C}$$

k_c is capacitive coupling coefficient

Coupling to Driven Line



– Transient decays with a time constant $\tau_{xc} = R_o(C_C + C_o)$

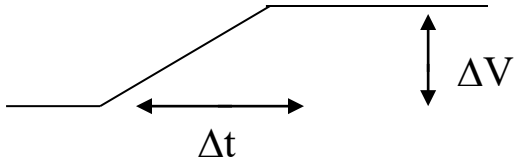
Capacitive Crosstalk Countermeasures

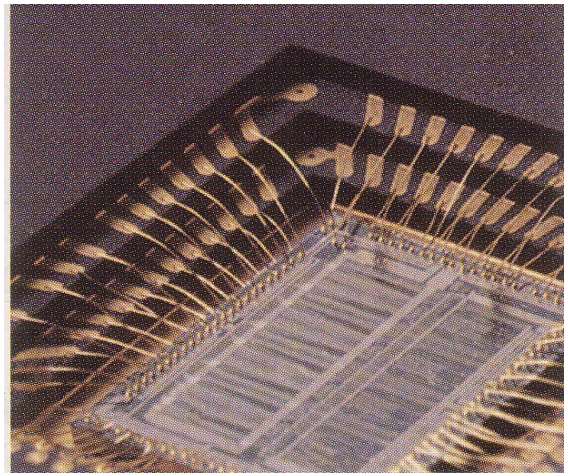
- Signals on adjacent layers should be routed in perpendicular directions
- Avoid floating signals
- Make rise time as large as possible
- Crosstalk can be made common mode by routing true and complement lines close to each other
- Provide shielding by placing conductors tied to GND and reference

Example

IC package modeled as lumped 5 nH inductor will house 128 full swing (3.3V) outputs into 50-Ω lines with 1 ns rise time

- How many return pins are needed if drop across returns must be less than 300 mV?
- How many pins if rise time is reduced to 3 ns?





Solution

Assume current ramp same as voltage ramp

$$\Delta I = \frac{\Delta V}{R} \times 128 = \frac{3.3}{50} \times 128 = 8.44A$$

$$L\frac{\Delta I}{\Delta t} \le V = 300mV \Rightarrow L \le 300\frac{\Delta I}{\Delta t} = 0.355nH$$

$$\frac{L}{n} \le 0.355nH \Rightarrow n \ge 140.8$$

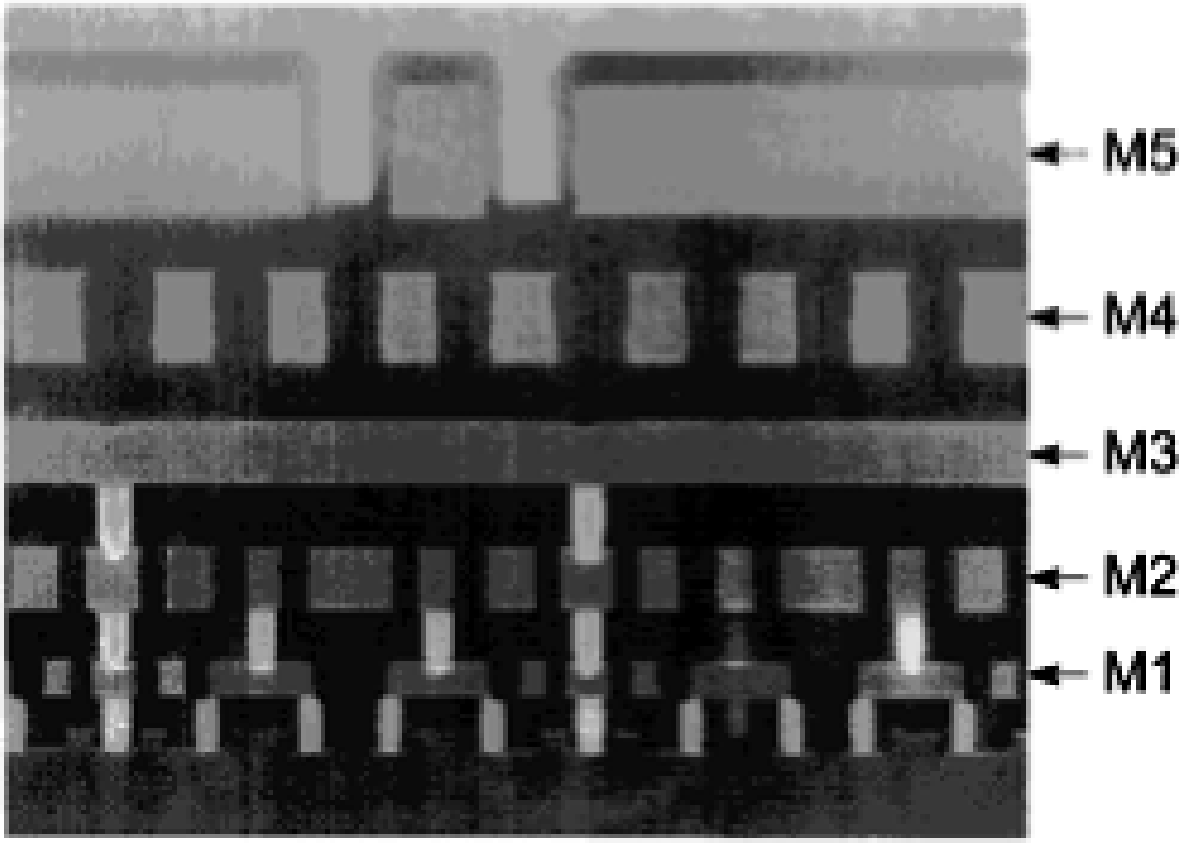
141 pins

– When rise time is 3 ns $n \ge \frac{L}{V}\frac{\Delta I}{\Delta t}$ $n \ge 46.9$

At least 46 pins

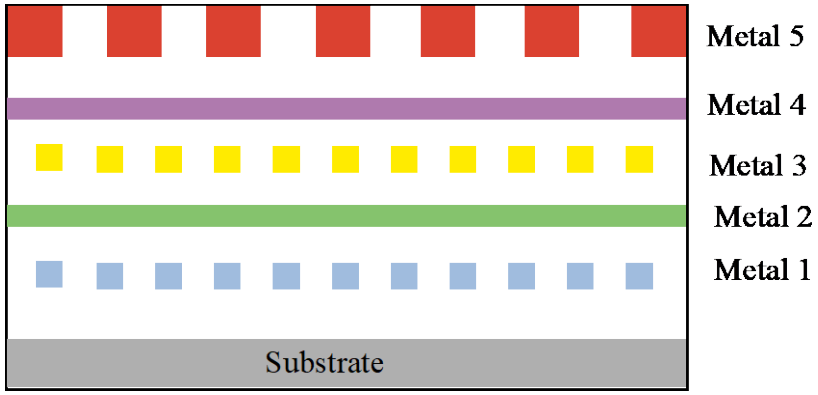
IC Wiring

Vertical parallel-plate capacitance	0.05 fF/μm^2
Vertical parallel-plate capacitance (min width)	0.03 fF/μm
Vertical fringing capacitance (each side)	0.01 fF/μm
Horizontal coupling capacitance (each side)	0.03



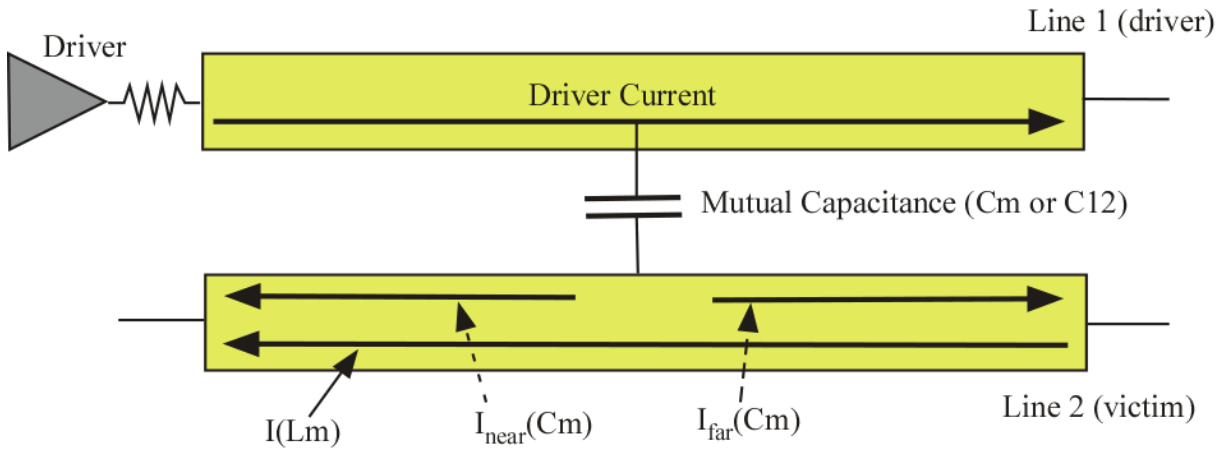
Source: M. Bohr and Y. El-Mansy - *IEEE TED Vol. 4, March 1998*

Integrated Circuit Wiring



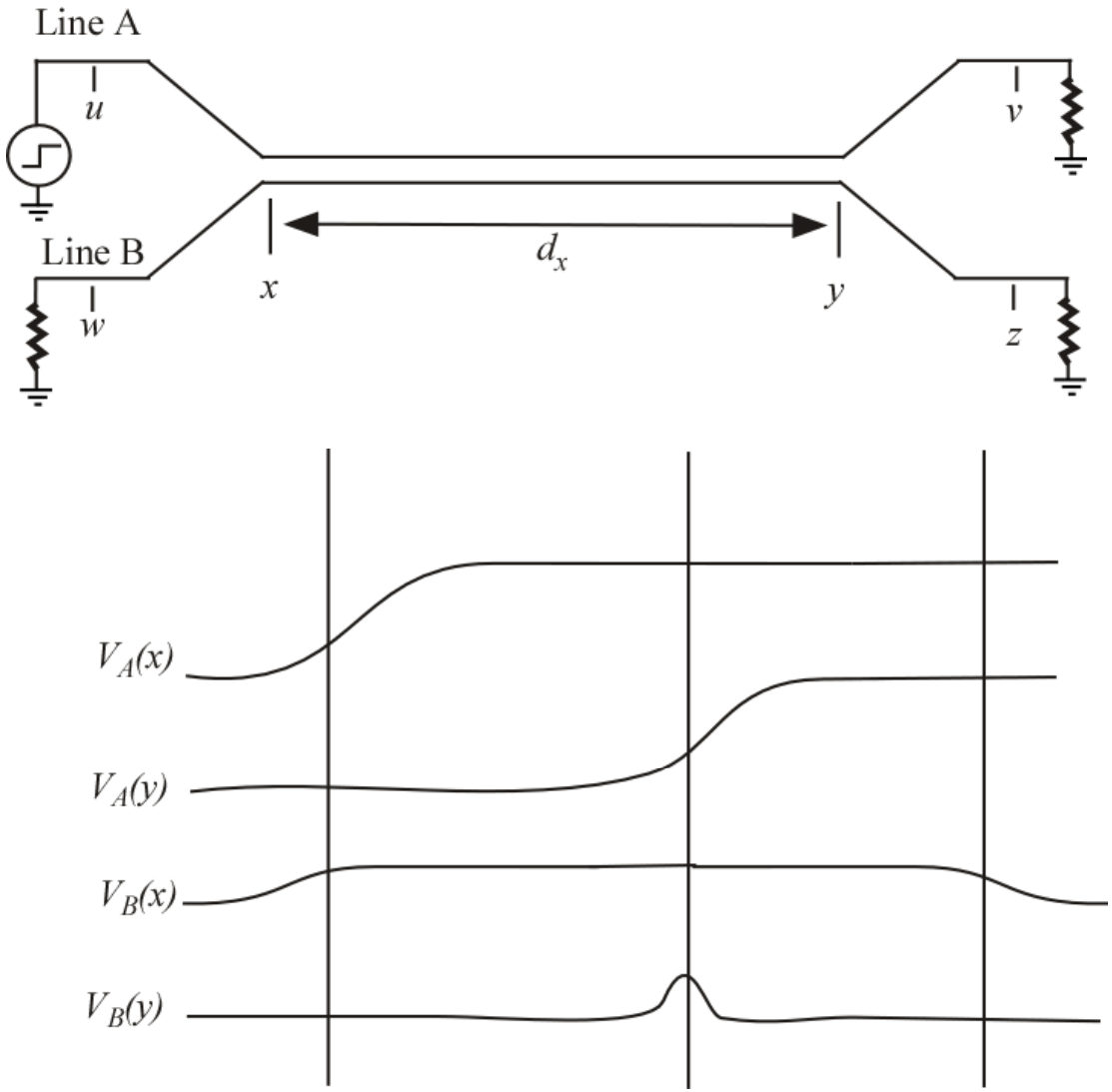
Vertical parallel-plate capacitance	0.05 fF/μm^2
Vertical parallel-plate capacitance (min width)	0.03 fF/μm
Vertical fringing capacitance (each side)	0.01 fF/μm
Horizontal coupling capacitance (each side)	0.03

Near- and Far-End Crosstalks

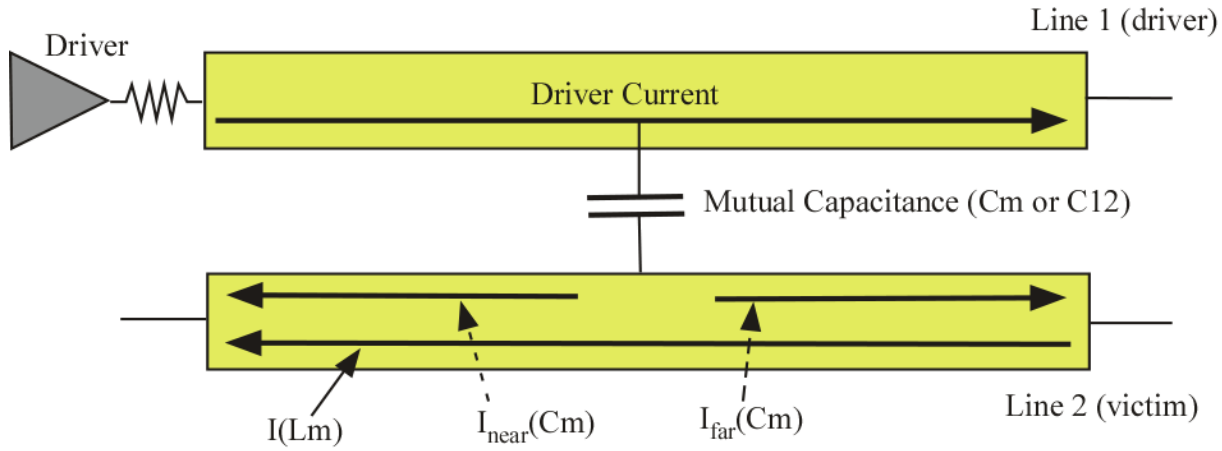


- **Crosstalk current due to mutual capacitance will split into 2 parts and flow toward both ends of victim line**
- **Crosstalk current due to mutual inductance will flow from the far end toward the near end of victim line**

Transmission-Line - Crosstalk



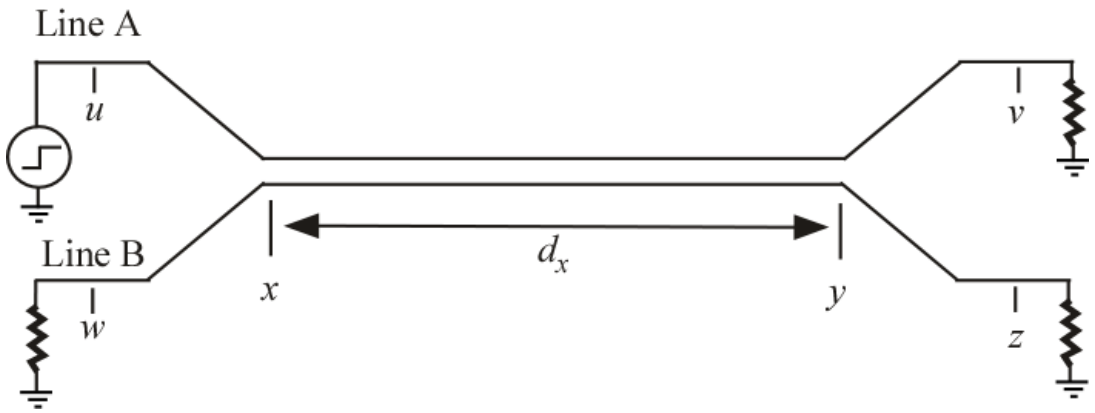
Near End Crosstalk



- Crosstalk seen on the victim line at the end closest to the driver
- Assumes that load is terminated with characteristic impedance of single isolated line
- Sum of contributions to reverse traveling wave that arrives at point x during period equal to time of flight

$$I_{near} = I(L_m) + I_{near}(C_m)$$

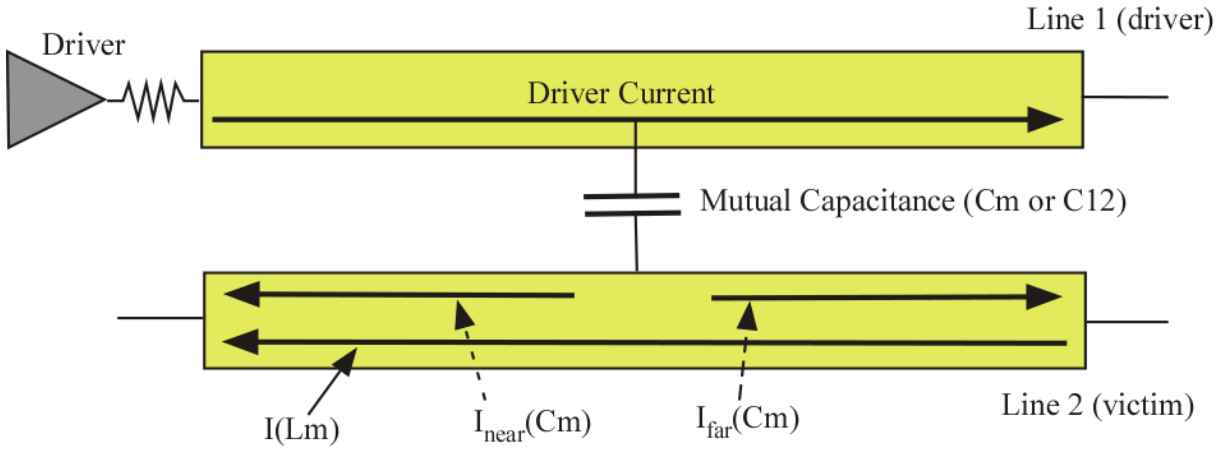
Near End Crosstalk



- Approximate quantity
- Assumes that load is terminated with characteristic impedance of single isolated line
- Sum of contributions to reverse traveling wave that arrives at point x during period equal to time of flight

$$k_{rx} = \frac{\left(k_{cx} + k_{lx}\right)}{4}$$

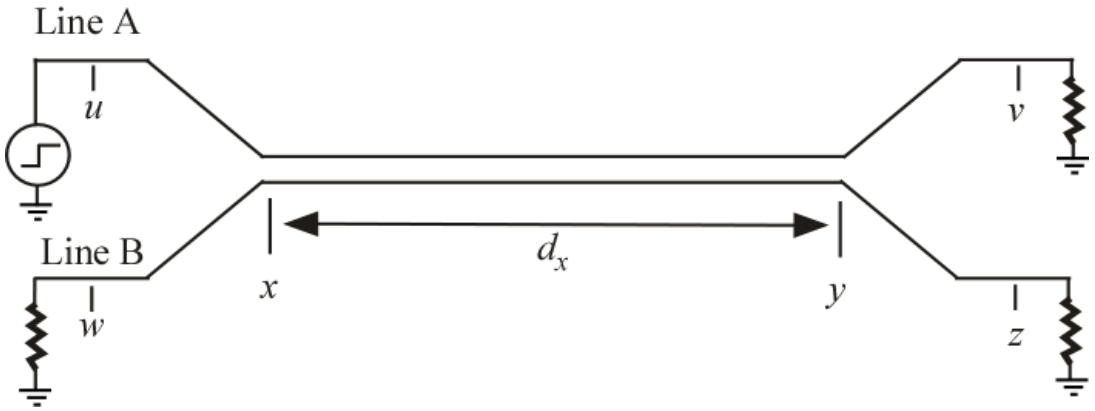
Far End Crosstalk



- **Crosstalk seen on the victim line at the end farthest away from the driver**
- **Assumes that load is terminated with characteristic impedance of single isolated line**

$$I_{far} = I_{far}(C_m) - I(L_m)$$

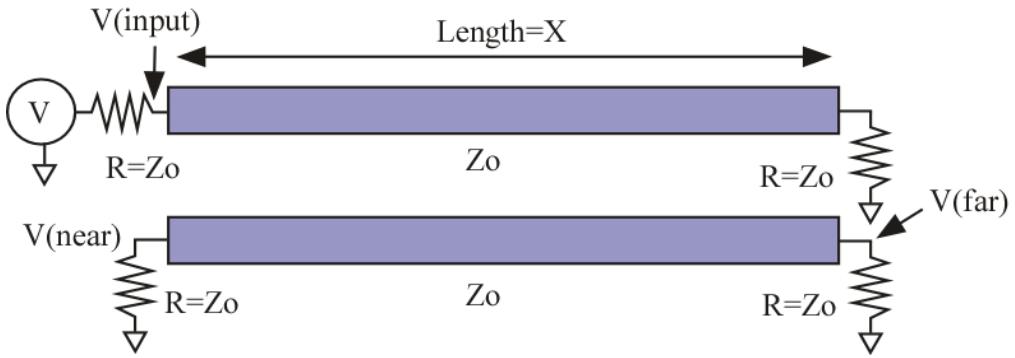
Far End Crosstalk

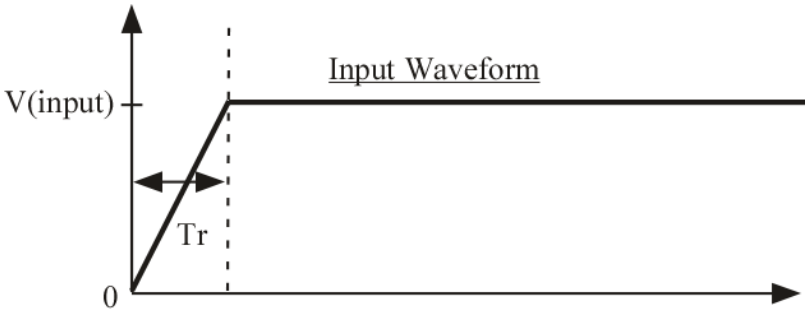


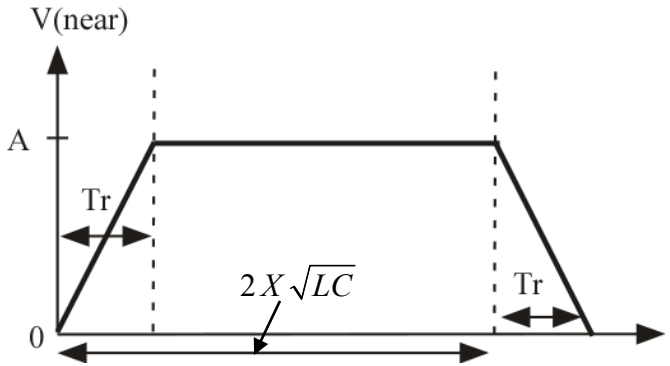
- **Approximate quantity**
- **Assumes that load is terminated with characteristic impedance of single isolated line**
- **Time derivative of signal on line A scaled by forward-coupling coefficient and coupling time**

$$k_{fx} = \frac{k_{cx} - k_{lx}}{4}$$

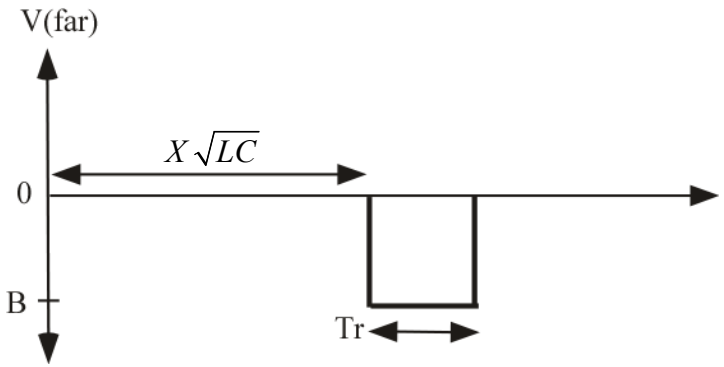
Digital Crosstalk - Case 1





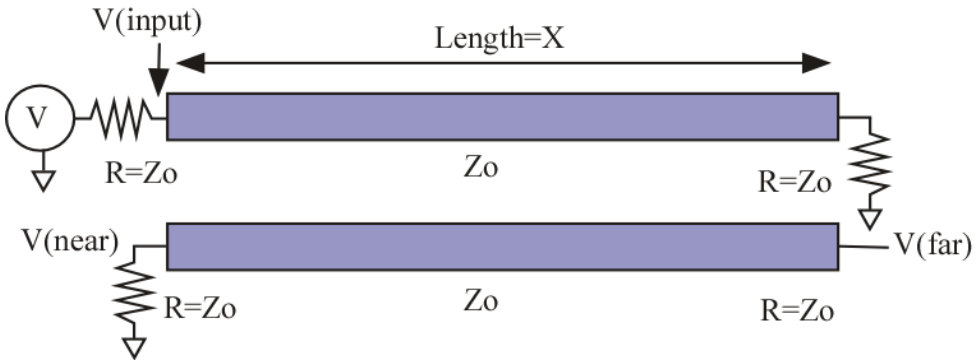


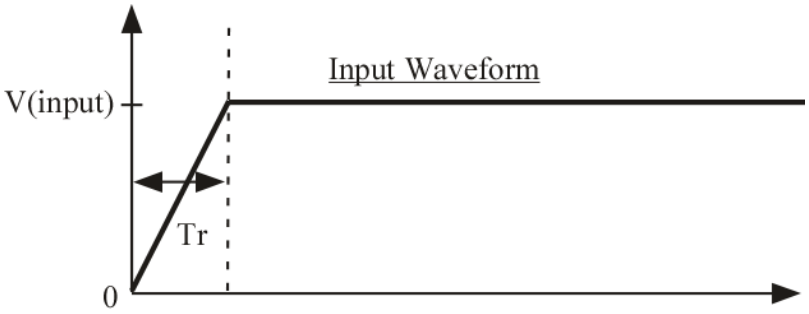
$$A = \frac{V(input)}{4}\left(\frac{L_M}{L} + \frac{C_M}{C}\right)$$

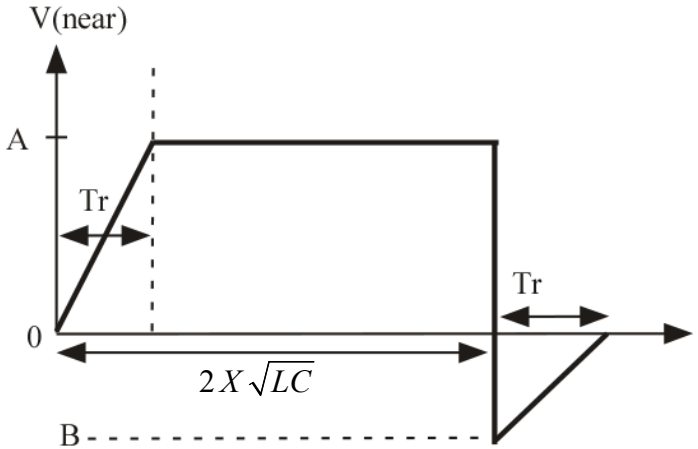


$$B = -\frac{V(input)\,X\sqrt{LC}}{2T_r}\left(\frac{L_M}{L} - \frac{C_M}{C}\right)$$

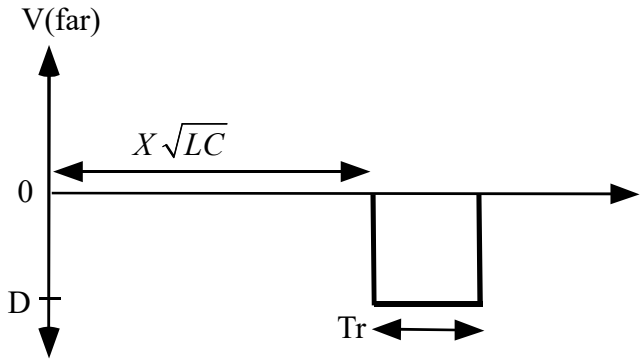
Digital Crosstalk - Case 2





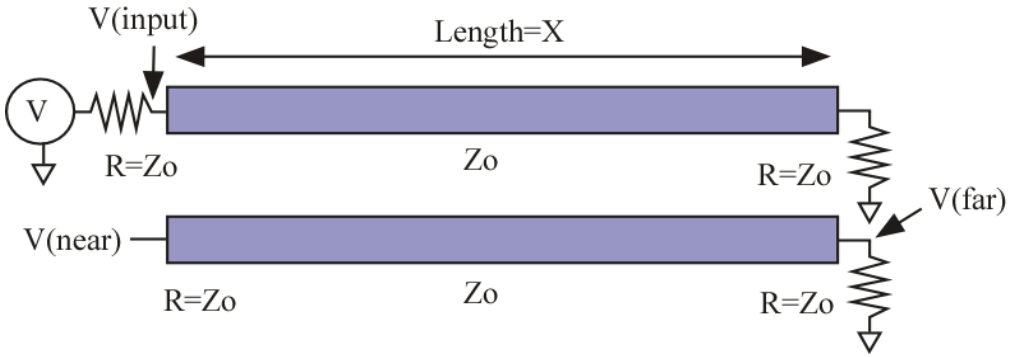


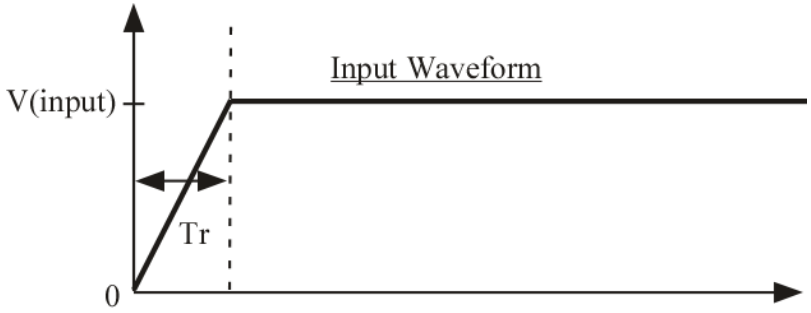
$$A = \frac{V(input)}{4}\left(\frac{L_M}{L} + \frac{C_M}{C}\right)$$

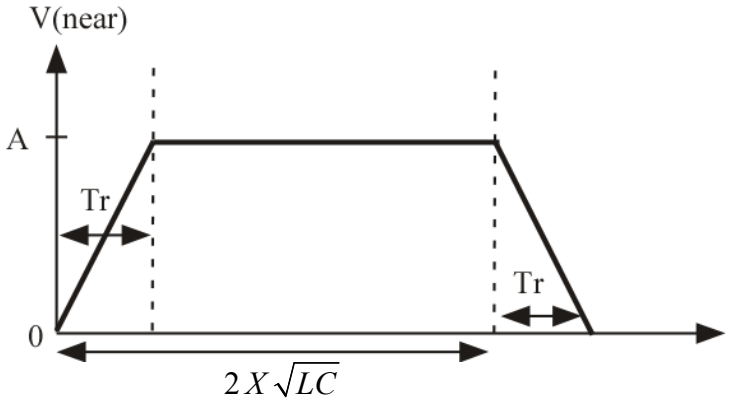


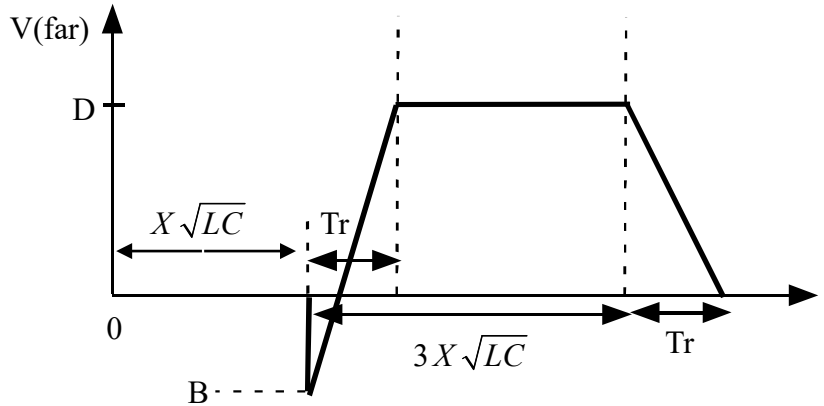
$$D = -\frac{V(input)\,X\sqrt{LC}}{T_r}\left(\frac{L_M}{L} - \frac{C_M}{C}\right)$$

Digital Crosstalk - Case 3









$$A = \frac{V(input)}{2}\left(\frac{L_M}{L} + \frac{C_M}{C}\right) \qquad B = -\frac{V(input)\,X\sqrt{LC}}{2T_r}\left(\frac{L_M}{L} - \frac{C_M}{C}\right) \qquad D = \frac{V}{4}\left(\frac{L_M}{L} - \frac{C_M}{C}\right)$$

Crosstalk Facts

- If the rise or fall time is short compared to the delay of the line, the near-end crosstalk noise is independent of the rise time.

- If the rise or fall time is long compared to the delay of the line, the near-end crosstalk noise is dependent on the rise time

- The far-end crosstalk is always dependent on the rise or fall time

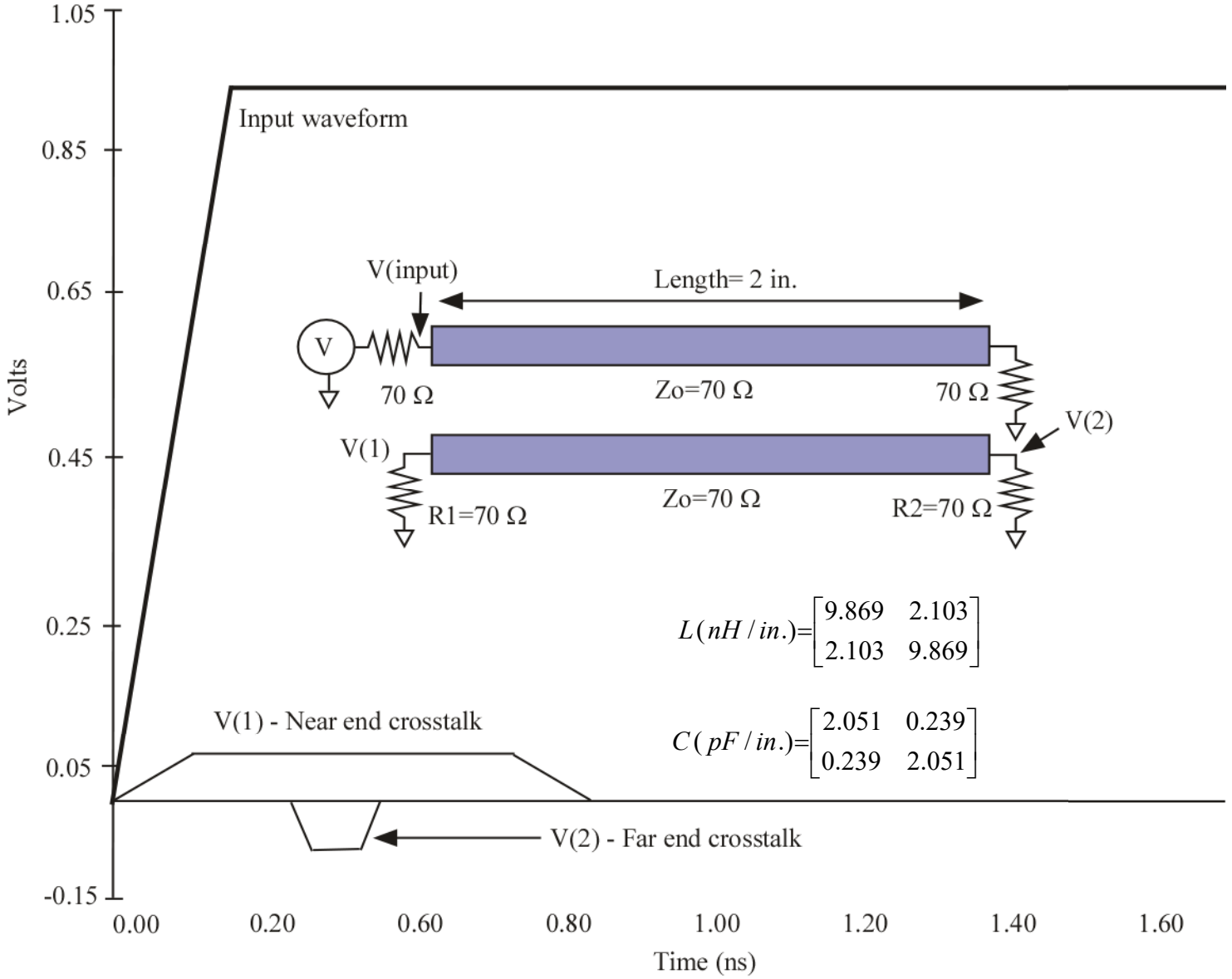
Crosstalk Facts

- Assume that the transmission lines are terminated
- The near-end crosstalk will begin at $t=0$ and have a duration of $2\,t_D$.
- The far-end crosstalk will occur at time $t=t_D$ and have a duration approximately equal to the signal rise or fall time

$$t_D = X\sqrt{LC}$$

X is the length of the lines

Example - Determine Near- and Far-End Crosstalk



Solution

$$V(1)=\frac{V(input)}{4}\left(\frac{L_{12}}{L_{11}}+\frac{C_{12}}{C_{11}}\right)=\frac{1}{4}\left(\frac{2.103\text{ nH}}{9.869\text{ nH}}+\frac{0.239\text{ pF}}{2.051\text{ pF}}\right)=0.082\text{ V}$$

$$\text{V}(2)=-\frac{V(input)\left(X\sqrt{LC}\right)}{2T_r}\left(\frac{L_{12}}{L_{11}}-\frac{C_{12}}{C_{11}}\right)$$

$$\text{V}(2)=-\frac{1\left[2\sqrt{(9.869\text{ nH})(2.051\text{ pF})}\right]}{2(100\text{ ps})}\left(\frac{2.103\text{ nH}}{9.869\text{ nH}}-\frac{0.239\text{ pF}}{2.051\text{ pF}}\right)=-0.137\text{ V}$$

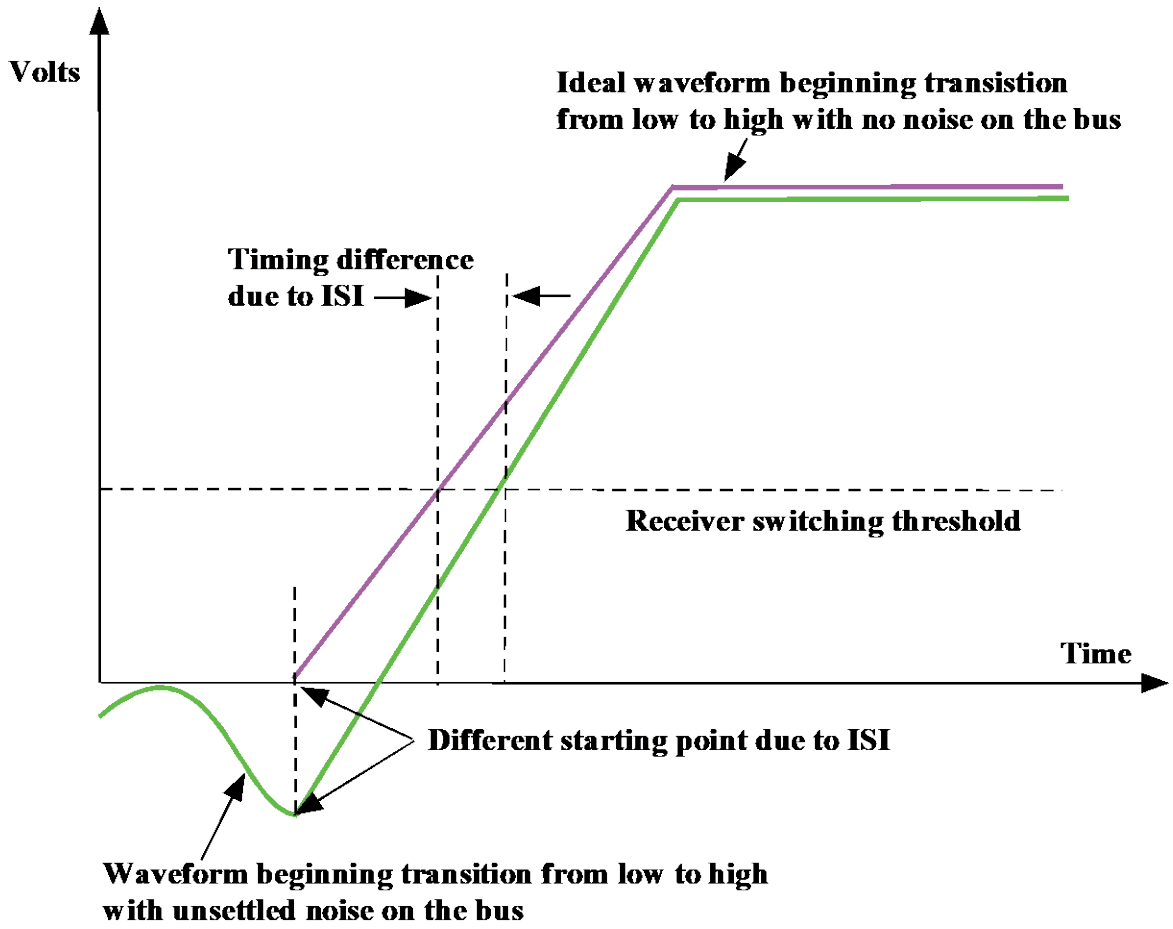
TL Crosstalk Countermeasures

- High-swing signals should not be routed on lines immediately
- Match k_{lx} and k_{cx} to eliminate far end crosstalk
- If k_{fx} is nonzero, avoid long parallel lines
- Terminate with Zs
- Make rise time as long as possible

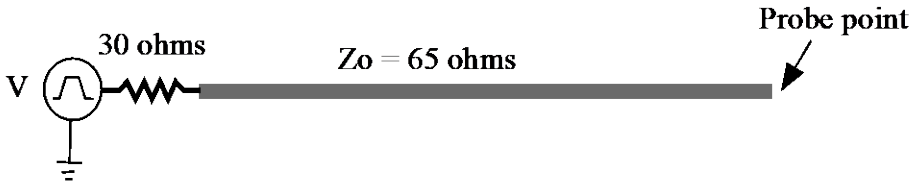
Intersymbol Interference (ISI)

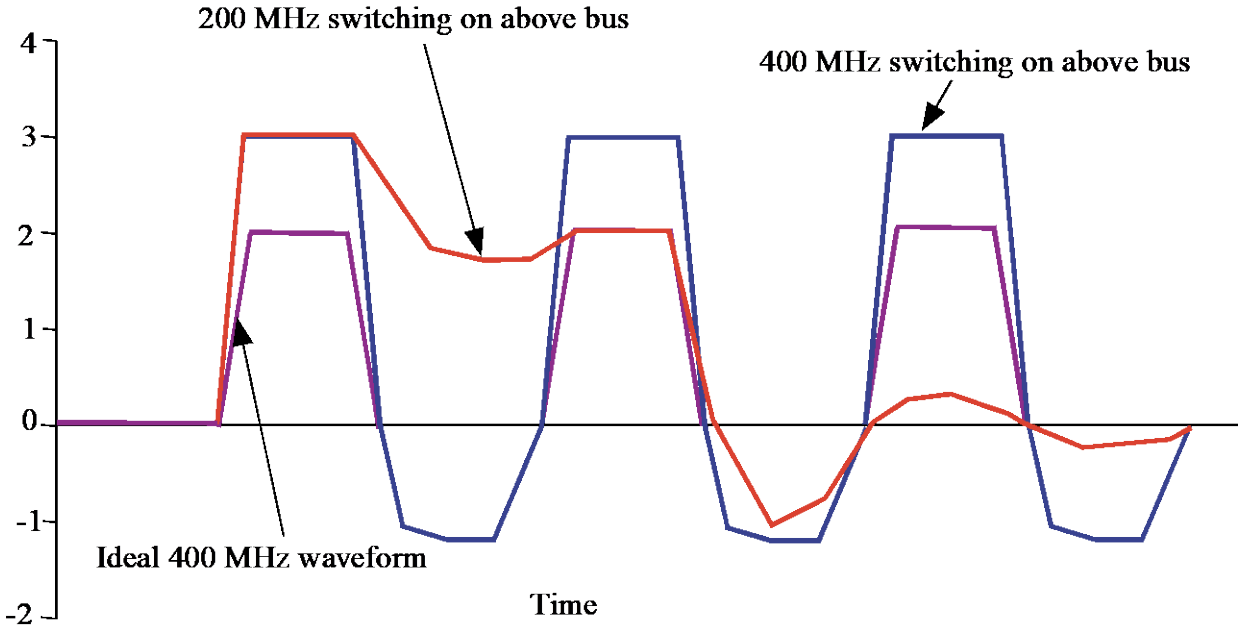
- Signal launched on a transmission line can be affected by previous signals as result of reflections
- ISI can be a major concern especially if the signal delay is smaller than twice the time of flight
- ISI can have devastating effects
- Noise must be allowed to settled before next signal is sent

Intersymbol Interference



Intersymbol Interference and Signal Integrity





Minimizing ISI

- Minimize reflections on the bus by avoiding impedance discontinuities
- Minimize stub lengths and large parasitics from package sockets or connectors
- Keep interconnects as short as possible (minimize delay)
- Minimize crosstalk effects