ECE 546
Lecture - 22
Timing & Signaling

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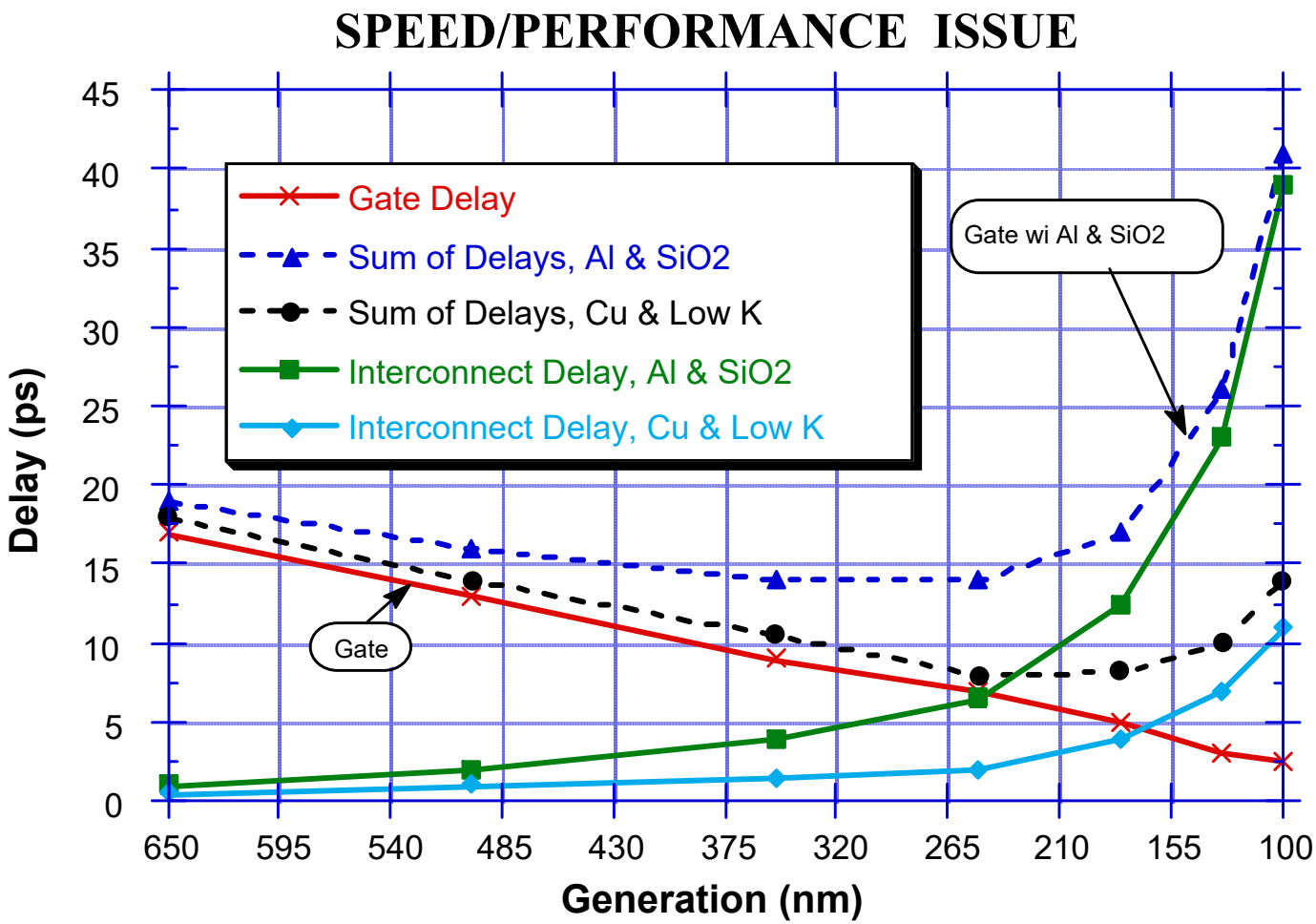
Semiconductor Technology Trends

	1997	2003	2006	2012
Chip size (mm^2)	300	430	520	750
Number of transistors (million)	11	76	200	1400
Interconnect width (nm)	200	100	70	35
Total interconnect length (km)	2.16	2.84	5.14	24

The Interconnect Bottleneck

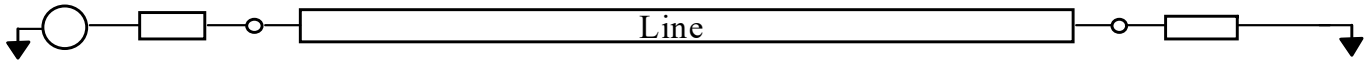
Technology Generation	MOSFET Intrinsic Switching Delay	Response Time
1.0 μm	~ 10 ps	~ 1 ps
0.01 μm	~ 1 ps	~ 100 ps

The Interconnect Bottleneck



Al 3.0 $\mu\Omega$-cm
Cu 1.7 $\mu\Omega$-cm
SiO2 $\kappa = 4.0$
Low κ $\kappa = 2.0$
Al & Cu .8μ *Thick*
Al & Cu Line 43μ *Long*

Chip-Level Interconnect Delay

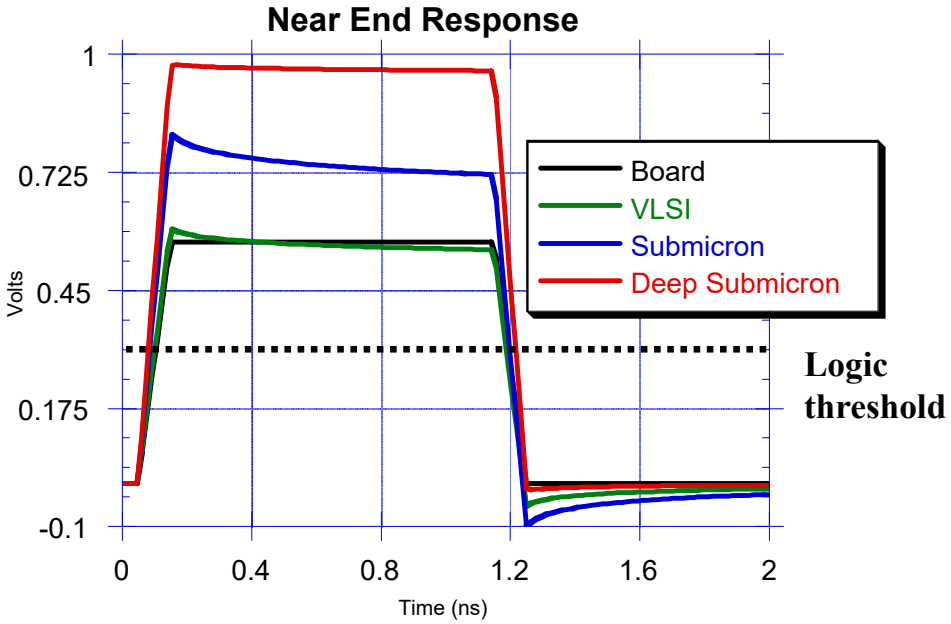


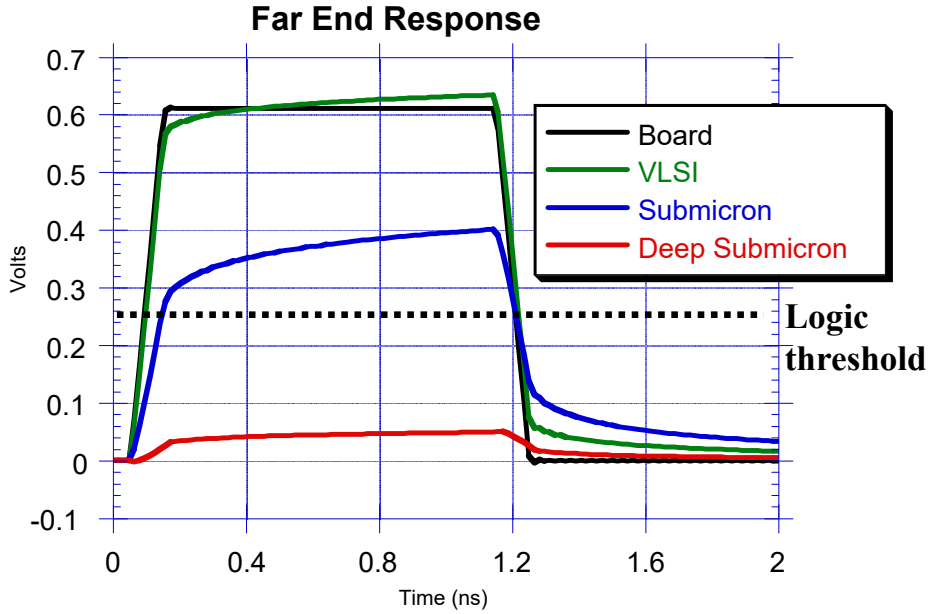
Pulse Characteristics:

rise time: 100 ps
fall time: 100 ps
pulse width: 4ns

Line Characteristics

length : 3 mm
near end termination: 50 Ω
far end termination 65 Ω





Interconnect

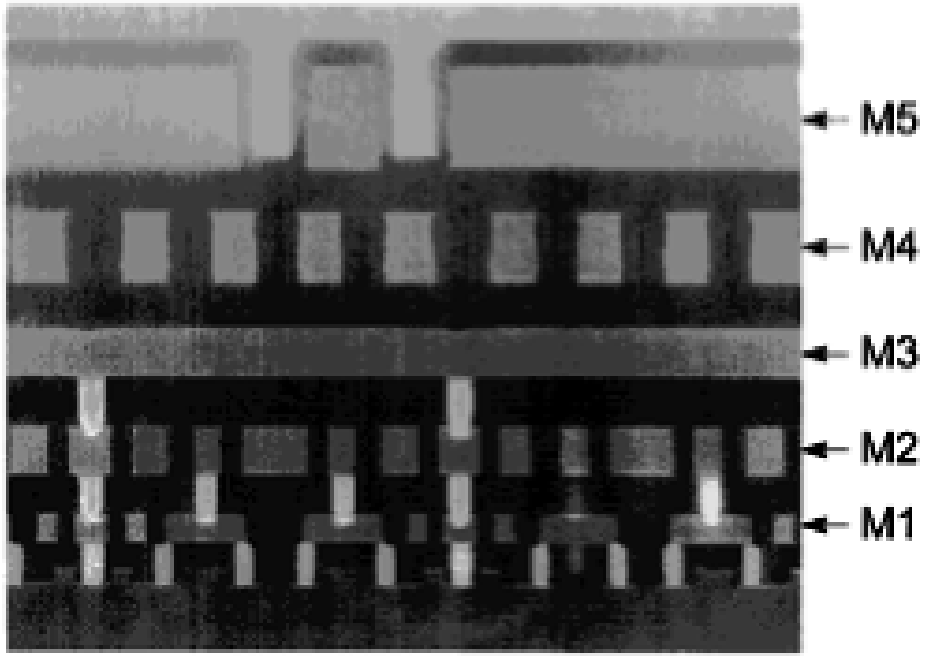
- **Total interconnect length (m/cm^2) – active wiring only, excluding global levels will increases:**

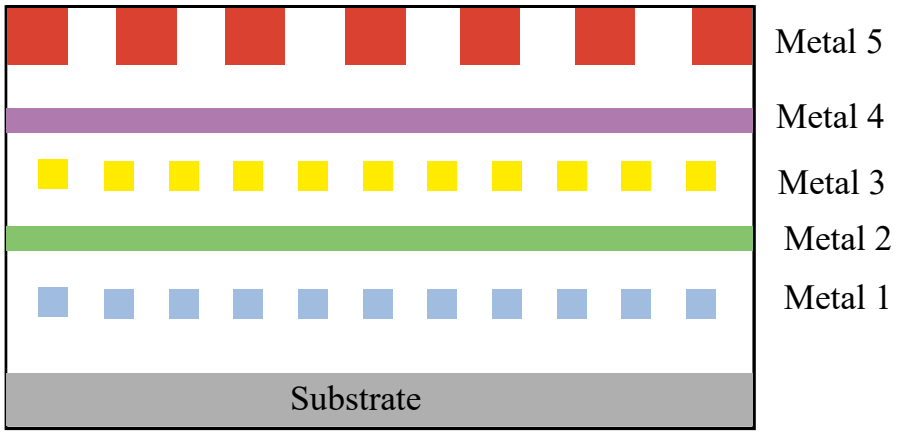
Year	2003	2004	2005	2006	2007	2008	2009
Total Length	579	688	907	1002	1117	1401	1559

- **Interconnect power dissipation is more than 50% of the total dynamic power consumption in 130nm and will become dominant in future technology nodes**

- **Interconnect centric design flows have been adopted to reduce the length of the critical signal path**

Integrated Circuit Wiring

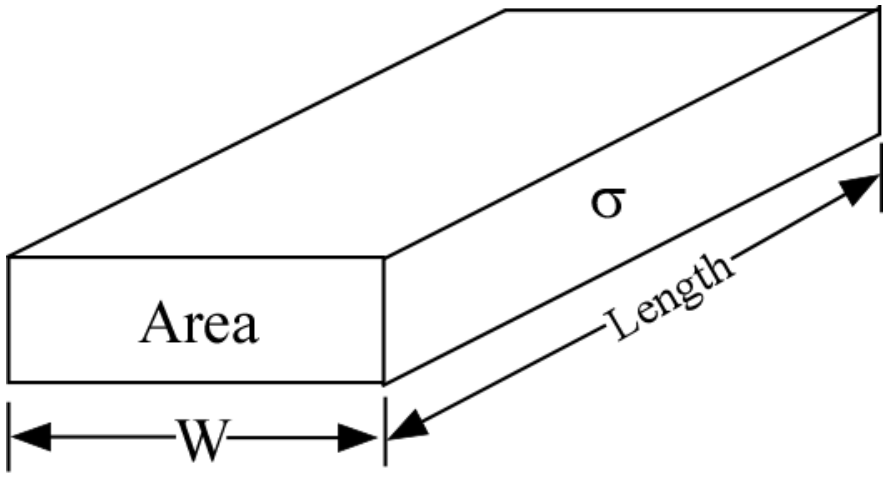




Source: M. Bohr and Y. El-Mansy - *IEEE TED Vol. 4, March 1998*

Vertical parallel-plate capacitance	0.05 fF/μm^2
Vertical parallel-plate capacitance (min width)	0.03 fF/μm
Vertical fringing capacitance (each side)	0.01 fF/μm
Horizontal coupling capacitance (each side)	0.03

Metallic Conductors



Resistance: R

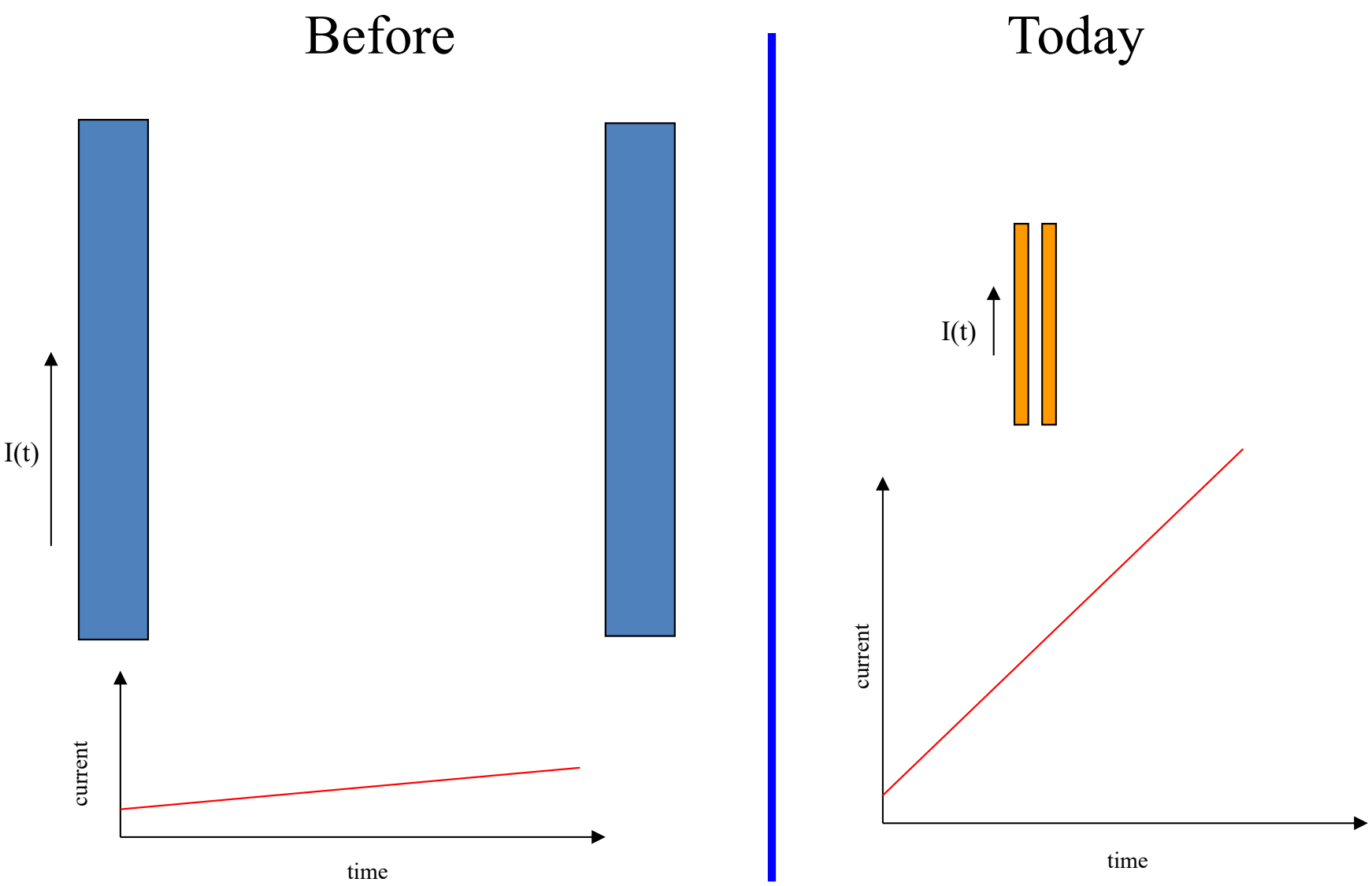
$$R = \frac{Length}{\sigma \cdot Area}$$

Resistance per unit length

Package level
W = 3 mils
R = 0.0045 Ω/mm

On-chip submicron
W = 0.25 microns
R = 422 Ω/mm

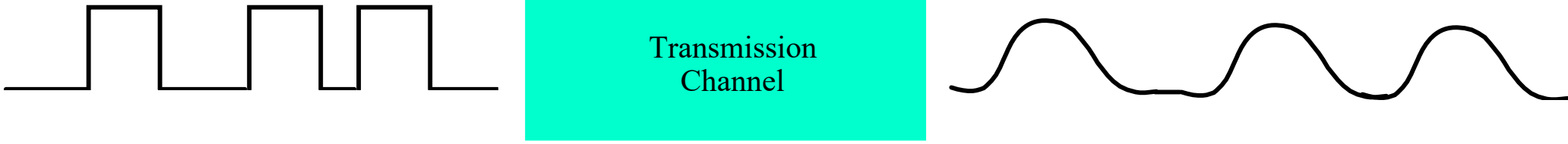
Integration & Signal Speed



Signal Integrity

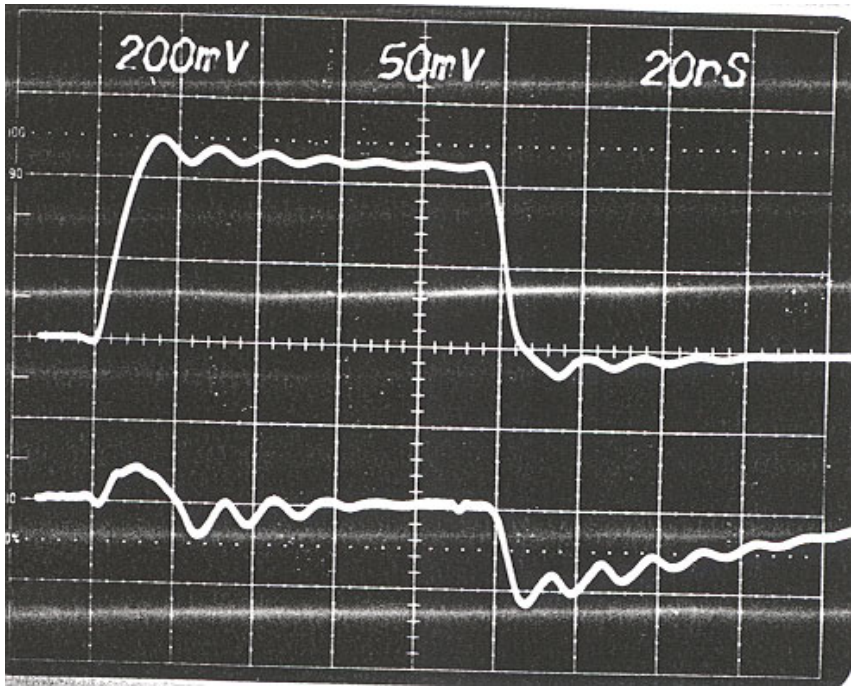
Ideal

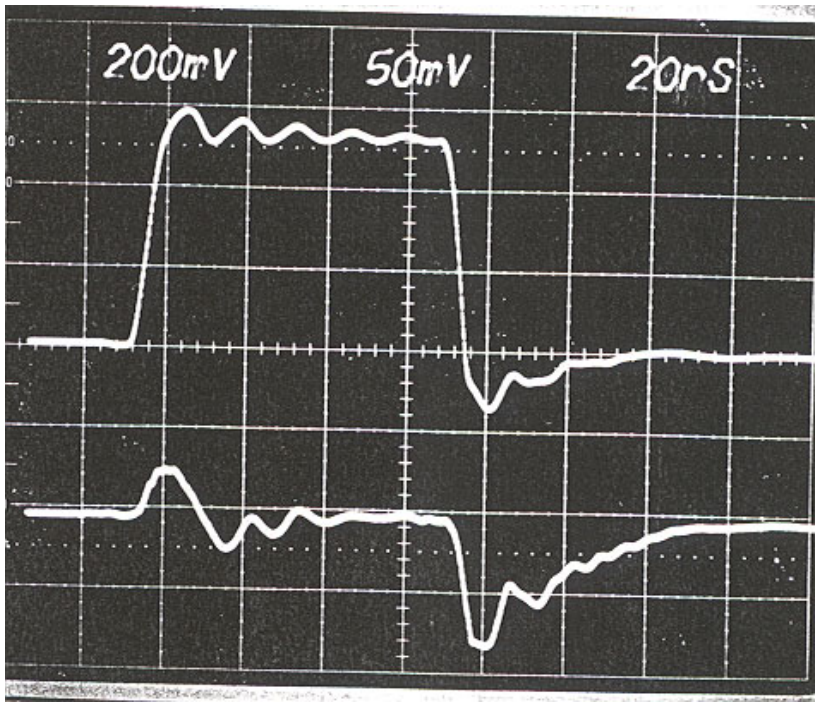
Common



Noisy

Signal Degradation



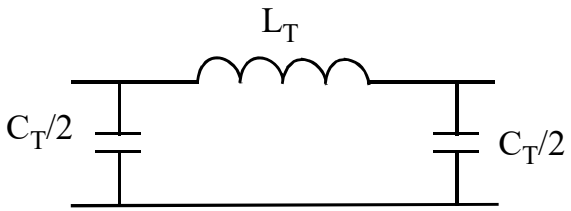


Modeling Interconnections

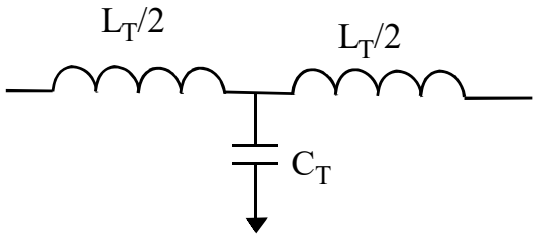
Low Frequency

Short

Mid-range Frequency

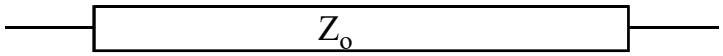


or



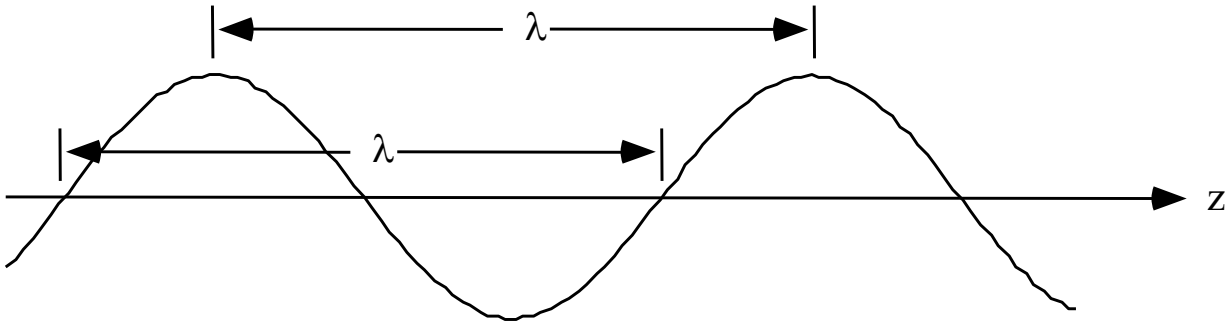
Lumped Reactive CKT

High Frequency



Transmission Line

WAVE PROPAGATION



Wavelength : λ

$$\lambda = \frac{\text{propagation velocity}}{\text{frequency}}$$

Why Transmission Lines ?

In Free Space

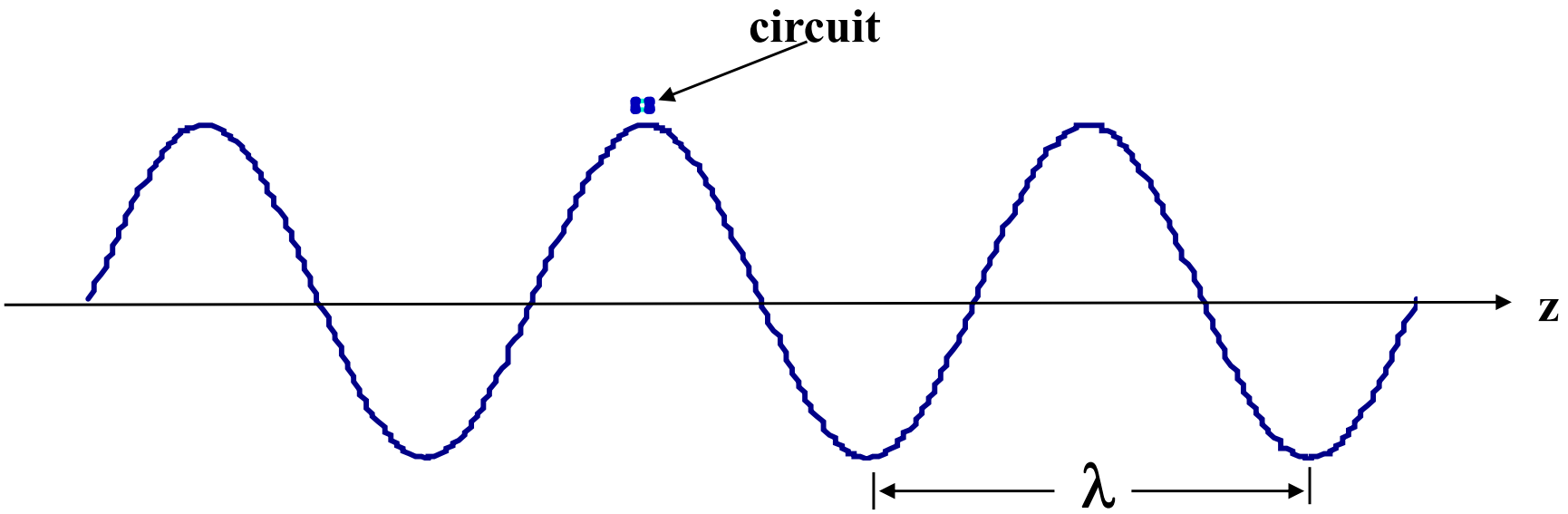
At 10 KHz : $\lambda = 30$ km

At 10 GHz : $\lambda = 3$ cm

Transmission line behavior is prevalent when the structural dimensions of the circuits are comparable to the wavelength.

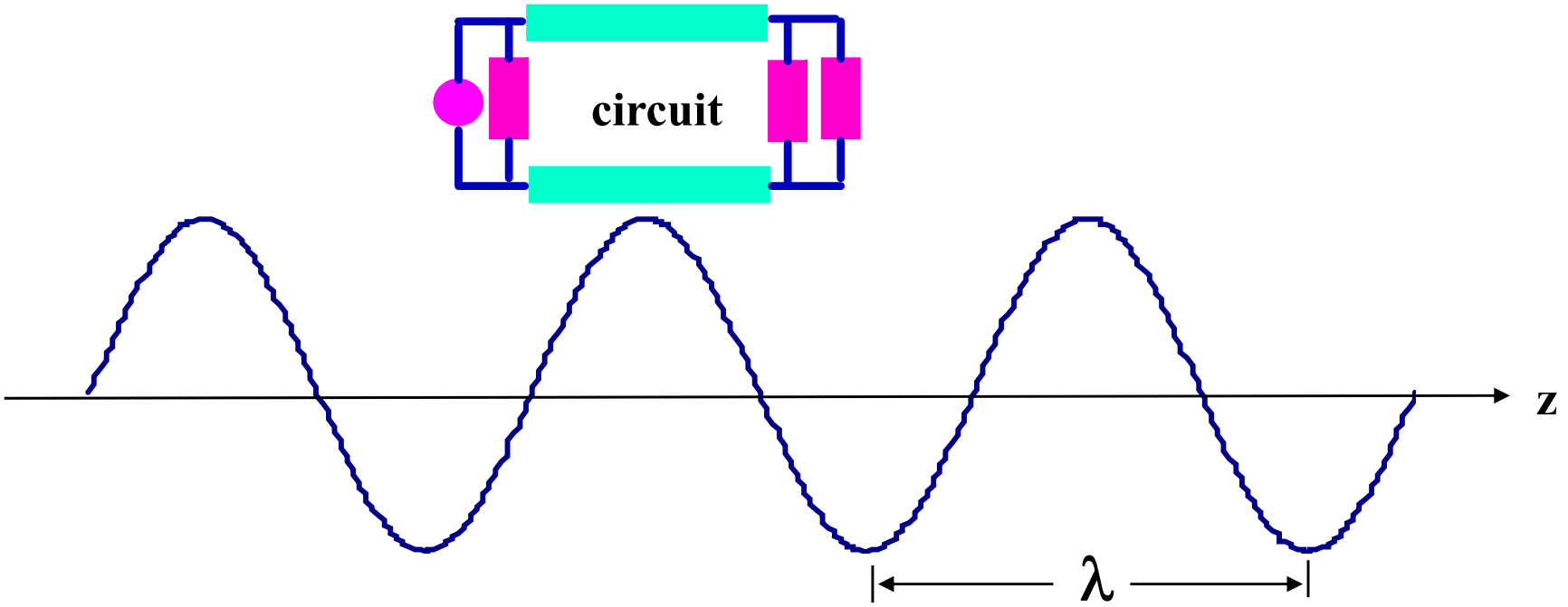
Transmission Line Model

Let d be the largest dimension of a circuit



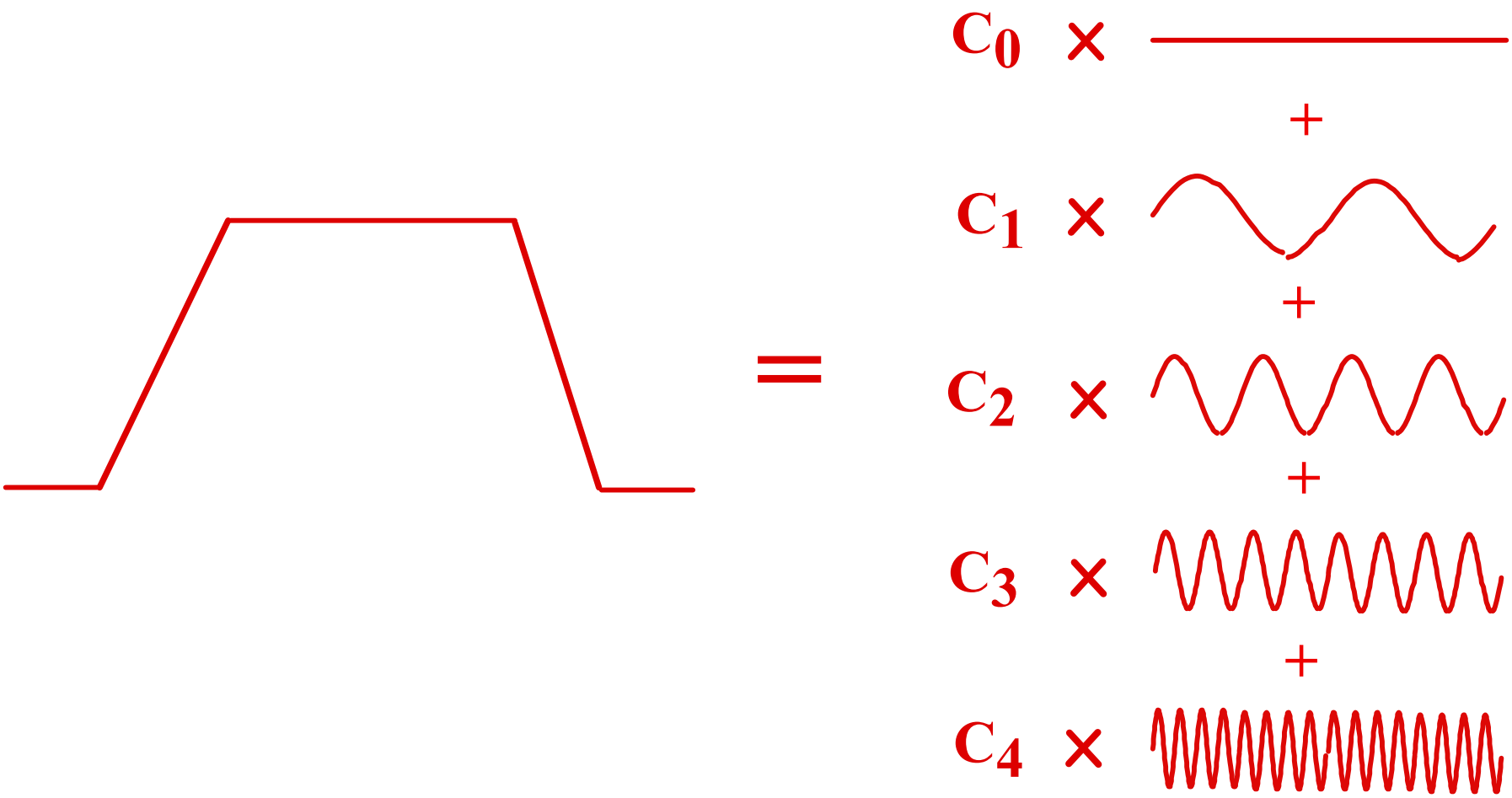
If d << λ, a lumped model for the circuit can be used

Transmission Line Model

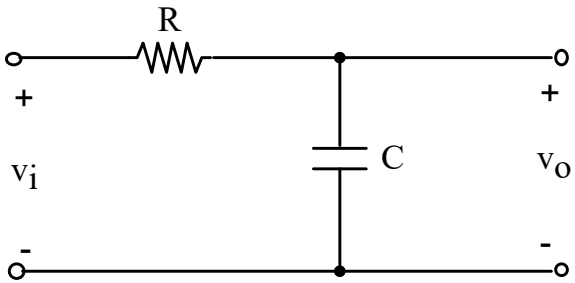


If d ≈ λ, or d > λ then use transmission line model

Frequency Components of Digital Signal



RC Network

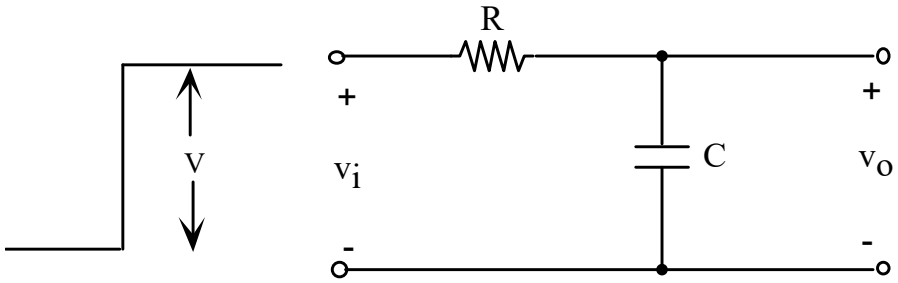


A is the steady-state gain of the network; $A = \frac{v_o(f)}{v_i(f)}$

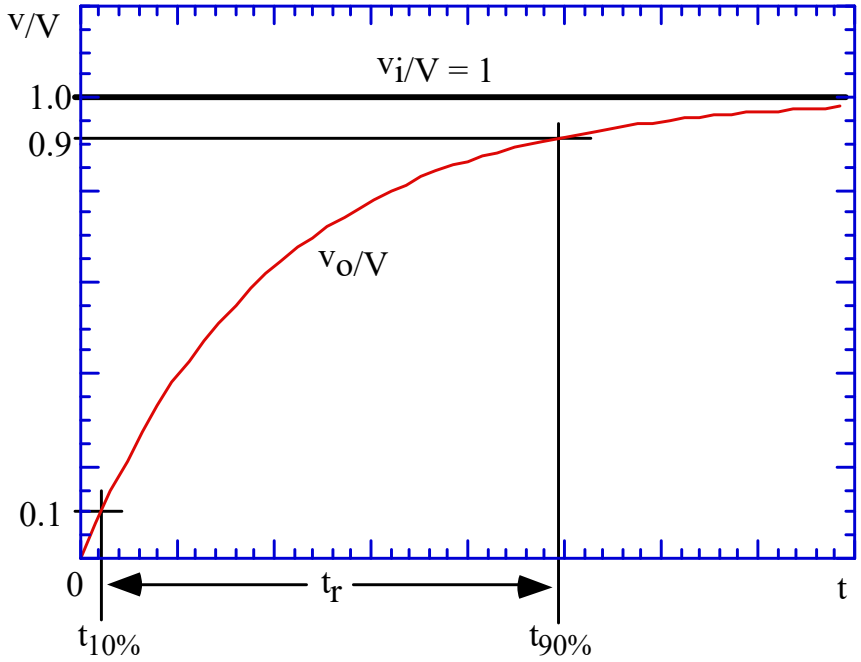
$$|A| = \frac{1}{\sqrt{1+(f/f_2)^2}} \qquad f_2 = \frac{1}{2\pi RC}$$

The gain falls to 0.707 of its low-frequency value at the frequency f_2. f_2 is the *upper 3-dB frequency* or the 3-dB bandwidth of the RC network.

RC Network



$$v_o = V\left(1 - e^{-t/RC}\right)$$



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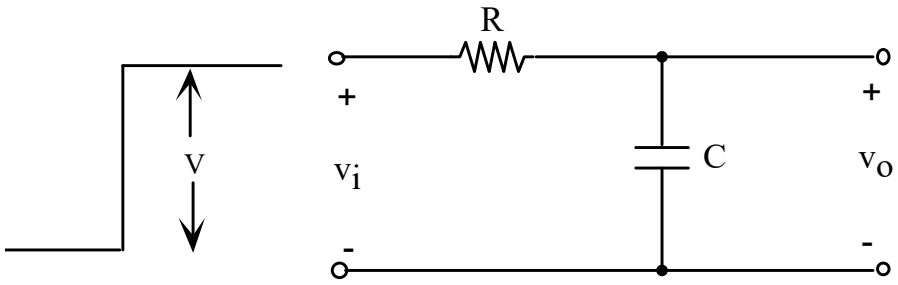


Rise time : $t_r = t_{90\%} - t_{10\%}$

$$t_r = 2.2RC = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2}$$

Observation: Simulating a 1-ns rise-time step requires a 3-dB bandwidth in the order of 350 MHz.

Rule of thumb: A 1-ns pulse requires a circuit with a 3-dB bandwidth of the order of 2 GHz.

Frequency Dependence of Lumped Circuit Models

At higher frequencies, a lumped circuit model is no longer accurate for interconnects and one must use a distributed model. Transition frequency depends on the dimensions and relative magnitude of the interconnect parameters.

$$f \approx \frac{0.3 \times 10^9}{10d\sqrt{\varepsilon_r}} \qquad t_r \approx \frac{0.35}{f}$$

Lumped Circuit or Transmission Line?

A) Determine frequency or bandwidth of the signal

-Microwave: f = operating frequency

-Digital: $f = \dfrac{0.35}{\text{rise time}}$

B) Determine propagation velocity in medium, v,

next calculate wavelength $\lambda = \dfrac{v}{f}$

Lumped Circuit or Transmission Line?

C) Compare wavelength with dimensions (feature size) d.

Case 1: If $\lambda >> d$ use lumped circuit equivalent

Total inductance = L x length

Total capacitance = C x length

Case 2: If $\lambda \approx 10d$ or $\lambda < 10d$, use transmission-line model

Frequency Dependence of Lumped Circuit Models

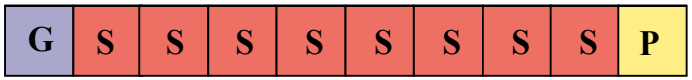
	Dimension	Frequency	Rise time
Printed circuit line (epoxy, glass)	10 in	>55 MHz	<7 ns
Package lead frame (ceramic)	1 in	>400 MHz	<0.9 ns
VLSI interconnection* (silicon)	100 μm	>8 GHz	<50 ps

* Using RC criterion for distributed effect

Connector Design

- Minimize physical length of connector pins.
- Maximize the ratio of power and ground pins to the signal pins. If possible these ratios should be < 1.
- Place each signal pin as close as possible to a current return pin.
- Place power pins adjacent to ground pins.

8-Bit Connector Pin-Out Options



inferior

improved

More improved

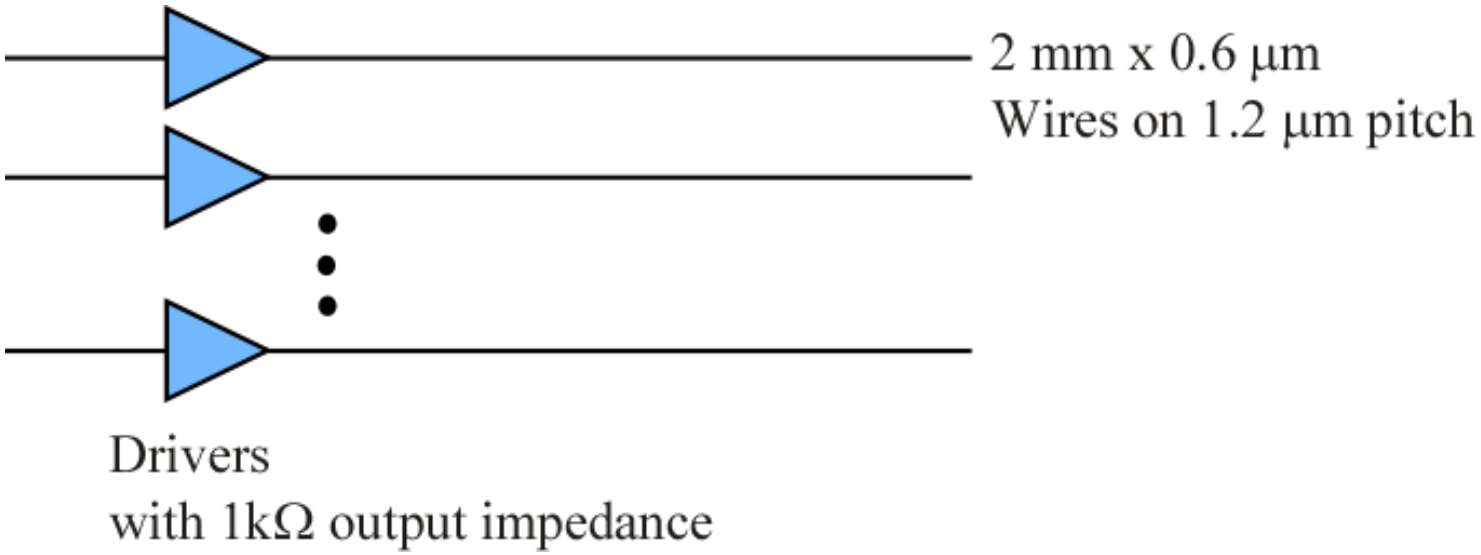
Optimal

Capacitive Crosstalk and Delay

Description	Capacitance	Units
Vertical parallel-plate capacitance	0.05	fF/μm^2
Vertical parallel-plate capacitance (minimum width)	0.03	fF/μm
Vertical fringing capacitance (each side)	0.01	fF/μm
Horizontal coupling capacitance (each side)	0.03	fF/μm

A chip has a 2-mm-long data bus of 0.6-μm wires on 1.2μm centers. Use the table values. Assume that the perpendicular wires on adjacent layers are all grounded. Each driver can be modeled as a voltage source in series with a 1-kΩ resistor. All lines switch simultaneously to random states. What is the worst-case maximum and minimum delay of a line.

Capacitive Crosstalk and Delay



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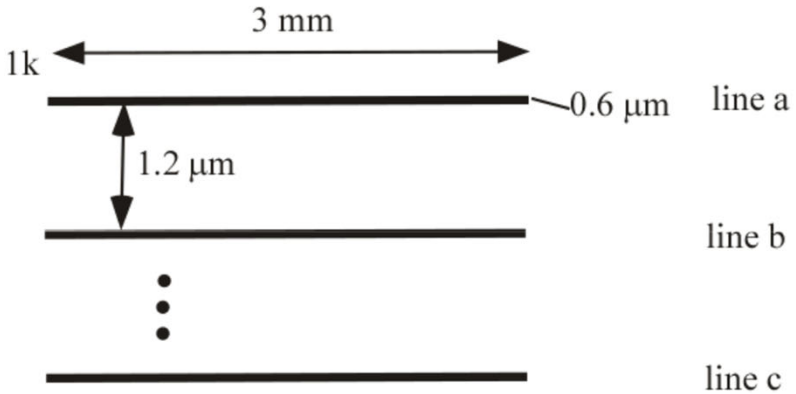
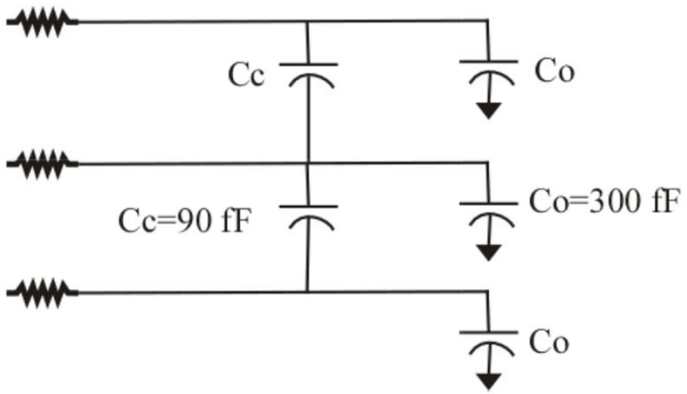
Capacitive Crosstalk and Delay





The resistance of the wires are much smaller than the 1kΩ of the drivers and thus can be ignored

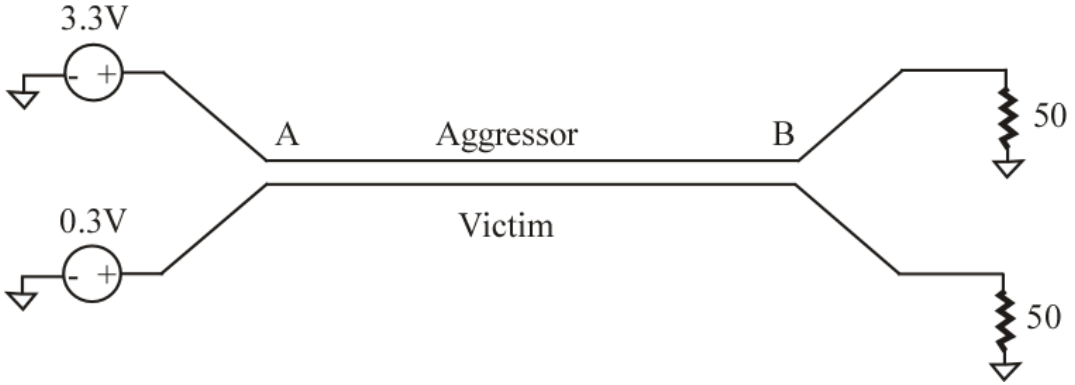
Worst case condition which will cause maximum delay is when the effective capacitance is maximum. If the 2 side aggressor lines transition in the opposite direction of the main driver on the victim line, this will create the most amount of capacitance (Miller effect)

Typical TL Parameters and Coupling Coefficients

Dimensions			Electrical Parameters					Coupling Coefficients			
W	S	H	C	C_m	L	M	Z	k_{ex}	k_{lx}	k_{fx}	k_{rx}
8	8	6	88	6.4	355	57.5	63	0.068	0.162	−0.047	0.058
8	8	3	137	3.0	240	18.5	42	0.021	0.077	−0.028	0.025
8	16	6	87	2.0	356	28.7	64	0.023	0.081	−0.029	0.026
8	16	3	136	1.0	240	8.2	42	0.007	0.034	−0.013	0.010
8	8	6*	148	6.6	302	13.4	45	0.043	0.044	0.000	0.022
8	8	3*	233	1.2	191	1.0	29	0.005	0.005	0.000	0.003
8	16	6*	147	1.3	302	2.6	45	0.008	0.009	0.000	0.004
8	16	3*	233	0.3	191	0.2	29	0.001	0.001	0.000	0.001

Example

Full-swing (3.3V) CMOS signal with a fast 500 ps rise time next to a low-swing (300 mV) signal for a 10 cm run of microstrip line. The lines are each 8 mils wide spaced 6 mils above a ground plane and spaced 8 mils from one another (see previous Table).Is the noise induced in the low-swing line a concern?



– From table, we get k_{fx}=-0.047, k_{rx}=0.058

Far end crosstalk

C=C+C_m=88+6.4=94.4 pF/m

L = 355 nH/m

$$v=\frac{1}{\sqrt{LC}}=\frac{1}{\sqrt{94.4\,pF/m\times 355nH/m}}=1.73\times 10^8 \text{ m/s} \qquad t_x=\frac{10cm}{1.73\times 10^8}=0.578\ ns$$

Example

In worst case, near- and far-end crosstalk will be added➔ add absolute values

$$V_{xtalk} = k_{fx} \times t_x \times \frac{\Delta V_{aggressor}}{\Delta t} + \Delta V_{aggressor} \times k_{rx} \times k_r$$

$$= 0.047 \times 0.578ns \times \frac{3.3}{500\,ps} + 3.3 \times 0.058 \times 1 = 0.37\ V$$

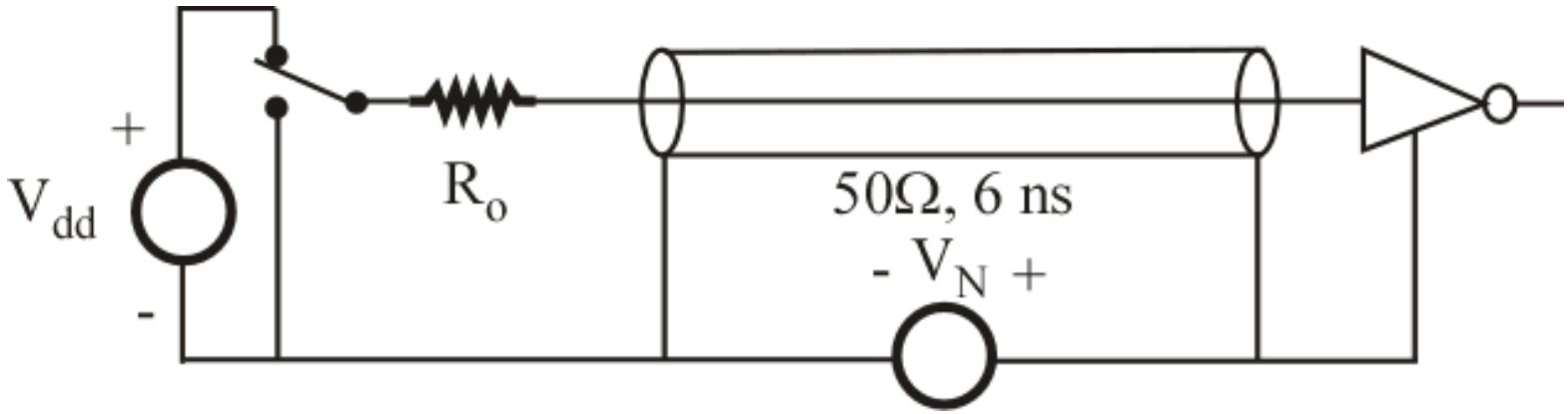
0.37 V is bigger than 300 mV/2=150 mV ➔ This will cause problem to the system

Victim line also produces crosstalk on the agressor. However, only second order effect is considered.

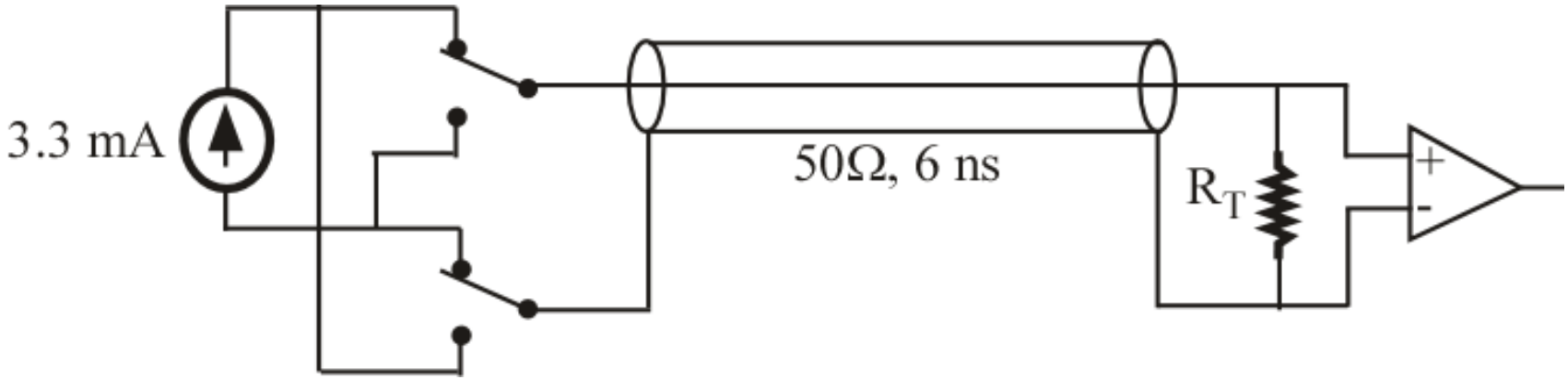
Signaling Conventions

- A good signaling convention isolates a signal from noise to provide noise immunity.
- Most signaling conventions in common use are based on standards and are actually quite poor.
- Many modern systems define their own signaling conventions rather than employ the standards

Transmission Systems



Full-swing CMOS transmission system



Low-swing current-mode transmission system

Transmission Systems

	CMOS	LSC
Signaling	Voltage mode: 0=GND, 1=V_{dd}	Current mode: 0=-3.3 mA 1=+3.3 mA
Reference	Power supply: $V_r \sim V_{dd}/2$	Self-centered: I_r=0 mA
Termination	Series terminated in output impedance of driver	Parallel-terminated at receiver with R_T within 10% of Z_o
Signal energy	1.3 nJ	22 pJ
Power dissipation	130 mW	11mW
Noise immunity	1.2:1 actual:required signal swing (with LSC receiver)	3.6:1
Delay	18 ns	6 ns

Transmission Systems

	CMOS (V)	LSC (mV)
V_{OH}	0.3	165
V_{OL}	0.0	-165
V_{IH}	2.2	10
V_{IL}	1.1	-10
V_{MH}	1.1	155
V_{ML}	1.1	155

	CMOS (mV)	LSC (mV)
Receiver sensitivity	300	10
Receiver offset	250	10
Power supply noise	300	3
Total noise (swing-independent)	850	23

	CMOS (%)	LSC (%)
Self-induced power supply noise (K_{in})	10	0
Crosstalk from other signals (K_{xt})	250	10
Reflections of the same signal from previous clock cycles (K_r)	large(>5)	5
Transmitter offset (K_{to})	10	10
Total proportional noise fraction (K_N)	>35	25

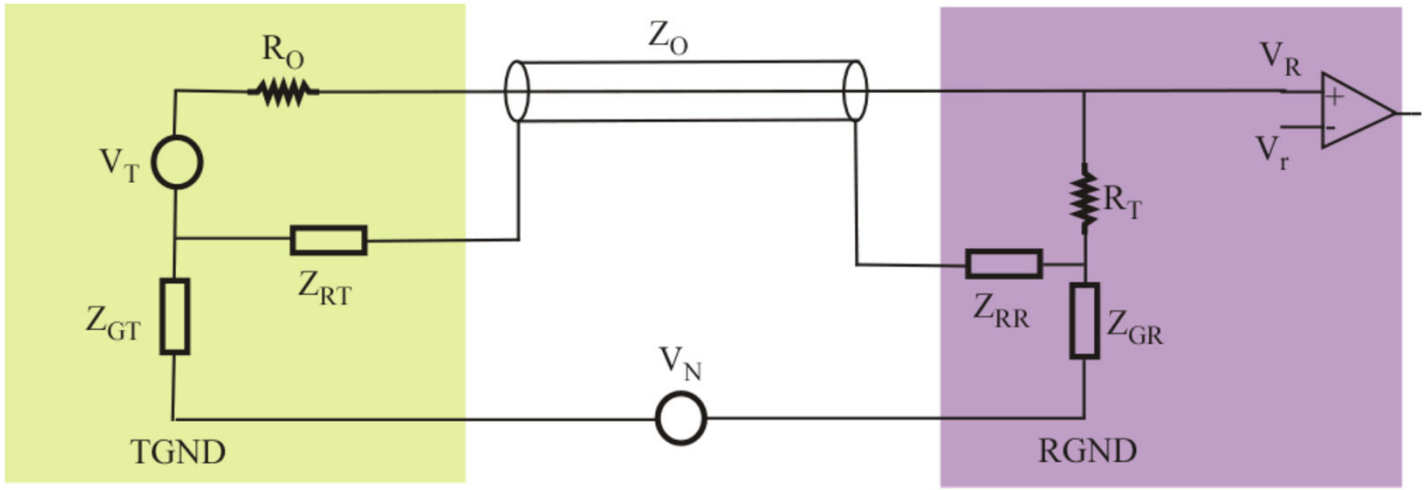
CMOS vs LSC

- With the worst-case combinations of noise sources the CMOS signaling system will fail
- The LSC system has 3.6 times the signal swing required.
- The transmission delay of the LSC system is the one-way delay of the transmission line.
- The CMOS driver must wait for the line to ring up to the full voltage.

CMOS vs LSC

- Basic CMOS system is most commonly used and yet is far from optimal
- Large energy signal is used where it is not needed
- Transmitted signal not isolated from supply noise
- Receiver uses reference that changes significantly with process variations

Signaling Modes for Transmission Lines

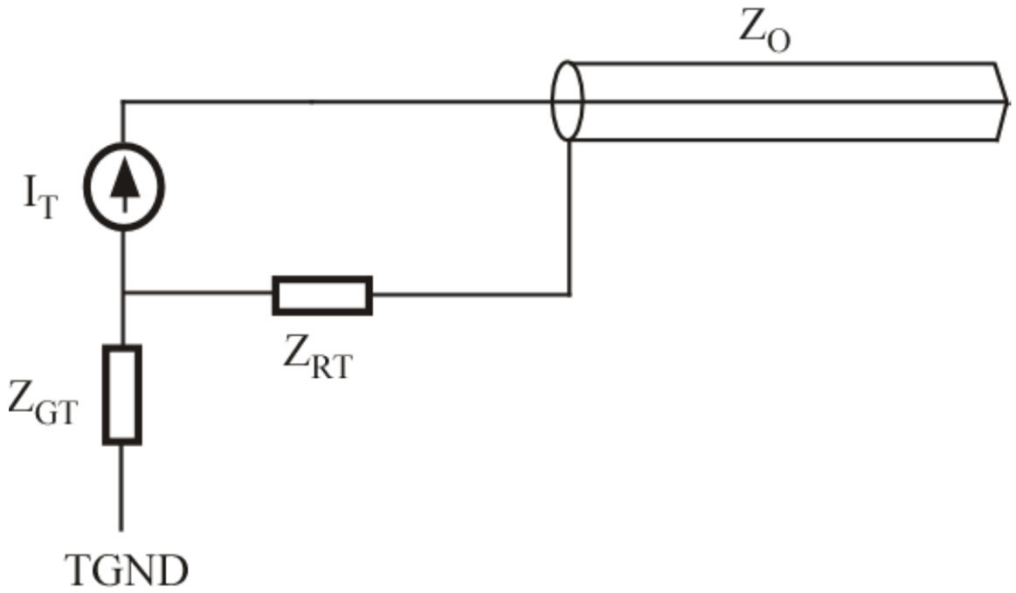


- Signal return impedances Z_{RT} and Z_{RR}
- Coupling to local power supply Z_{GT} and Z_{GR}
- Introduce noise V_N
- Sections can be separated if TL is terminated into match impedance

Transmitter Signaling Parameters

- Output impedance, R_o
- Coupling between signal and power supply Z_{GT}
- Polarity of signal
- Amplitude of signal

Current-Mode Transmission

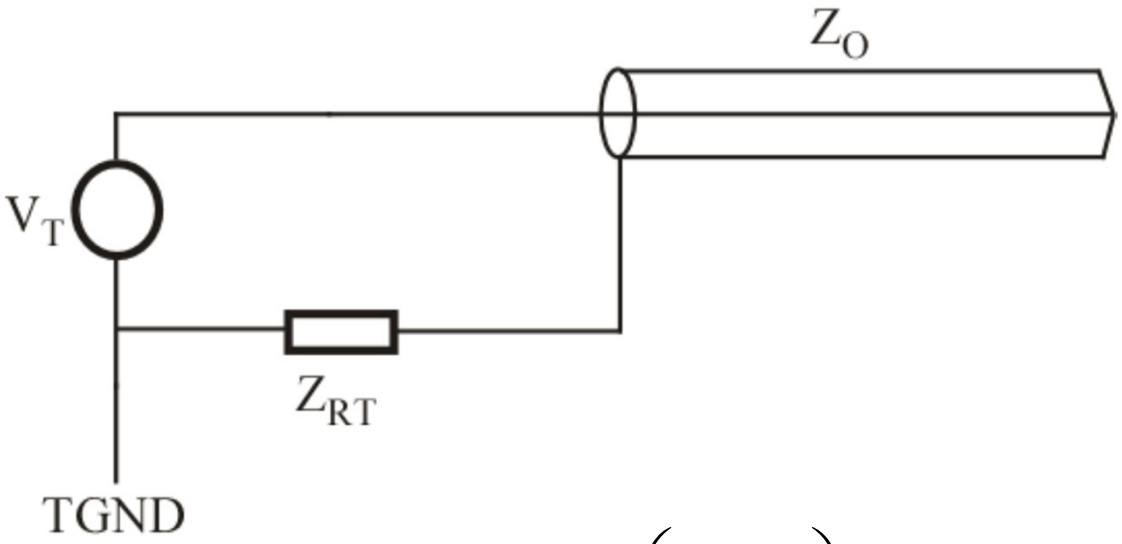


$$V(t,x) = I_T\left(t - \frac{x}{v}\right)Z_o$$

Provides isolation of both the signal and current return from the local power supplies

- Large Z_{GT}

Voltage-Mode Transmission



$$V(t,x) = V_T\left(t - \frac{x}{v}\right)$$

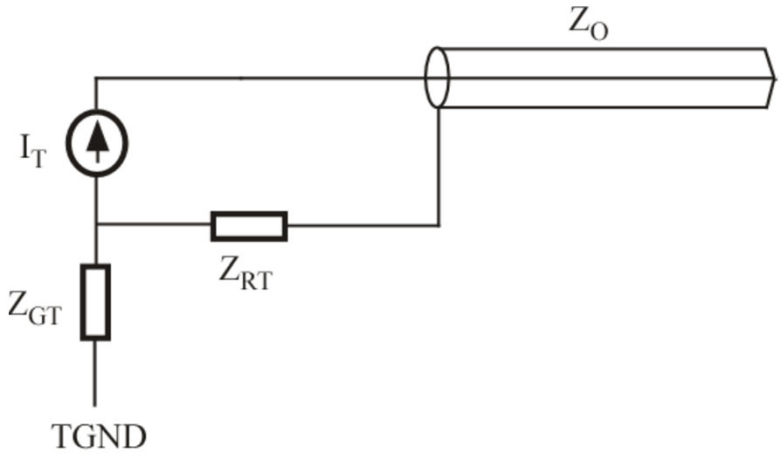
Makes a difference in:

- Signal return crosstalk

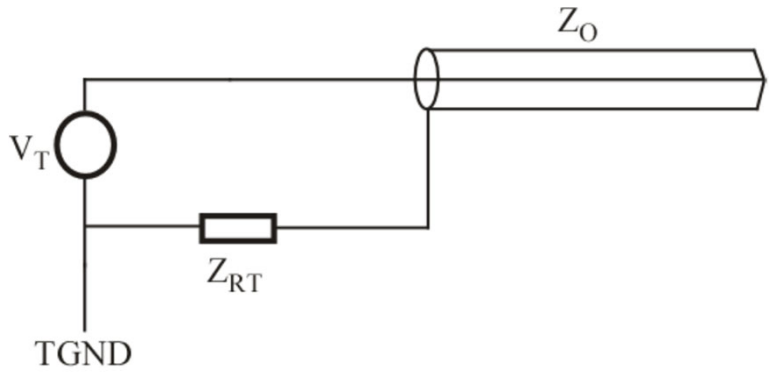
- Single power supply noise

Current- & Voltage-Mode Transmission

Current-Mode Transmission



Voltage-Mode Transmission



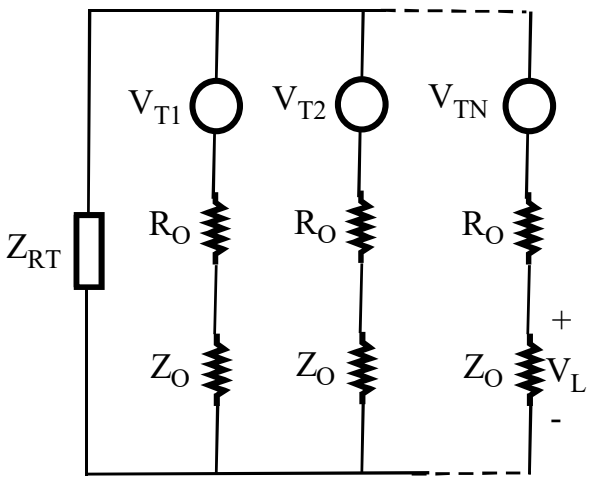
Output impedance >> Z_o

Output impedance << Z_o

Transmitter Signal-Return Crosstalk

- A signal return path is typically shared among a group of N signals (typically 2 to 8) to reduce cost.
- Sharing occurs at both ends of line.
- Z_{RT} approximates the return path impedance at the transmitter end.
- The return current from all N transmission lines passes through impedance Z_{RT}.
- The current $I_{T1} = V_{T1}/Z_o$ sees the shared return impedance in parallel with the series combination of the line and output impedances from other signals.
- The total return impedance is Z_X.

Transmitter Signal Return Crosstalk



$$Z_X = Z_{RT} \parallel \left(\frac{R_O + Z_O}{N-1} \right) = \frac{Z_{RT}\left(R_O + Z_O\right)}{\left(N-1\right)Z_{RT} + R_O + Z_O}$$

Current through each of the N-1 line impedance is:

$$I_X = I_{T1}\left(\frac{Z_X}{R_O + Z_O} \right) = I_{T1}\left[\frac{Z_{RT}}{\left(N-1\right)Z_{RT} + R_O + Z_O} \right]$$

Induced voltage across line impedance is:

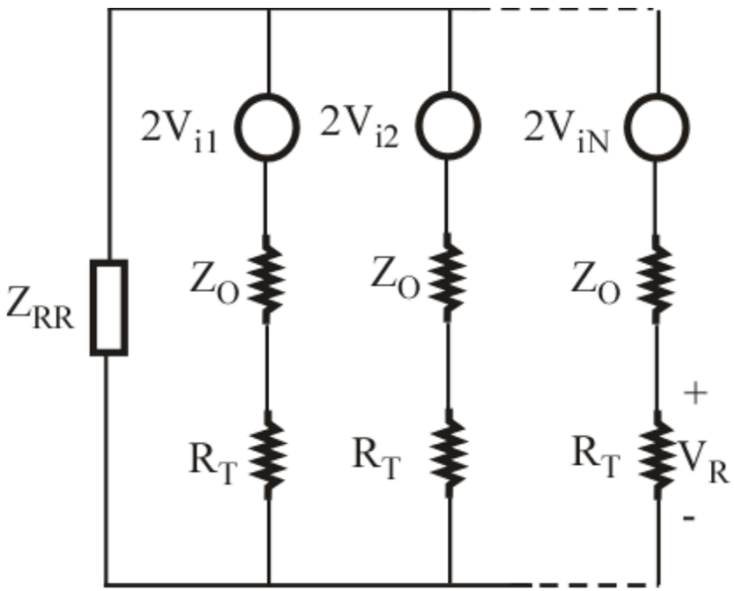
$$V_X = I_X Z_O = V_{T1}\left[\frac{Z_{RT}}{\left(N-1\right)Z_{RT} + R_O + Z_O} \right]$$

Considering worst case where N-1 signals switch simultaneously

$$K_{XRT} = \frac{(N-1)V_X}{V_{T1}} = \frac{\left(N-1\right)Z_{RT}}{\left(N-1\right)Z_{RT} + R_O + Z_O} \le \frac{\left(N-1\right)Z_{RT}}{R_O + Z_O}$$

With voltage-mode signaling, R_o=0, the transmitter signal return crosstalk is a maximum. For current-mode signaling, R_o is infinite and this form of crosstalk is eliminated.

Receiver Signal Return Crosstalk



$$K_{XRR} = \frac{(N-1)Z_{RR}}{(N-1)Z_{RR} + 2Z_O} \leq \frac{(N-1)Z_{RR}}{2Z_O}$$

- All N terminators return their current through Z_{RR} (shared impedance)

- No crosstalk advantage to current-mode signaling

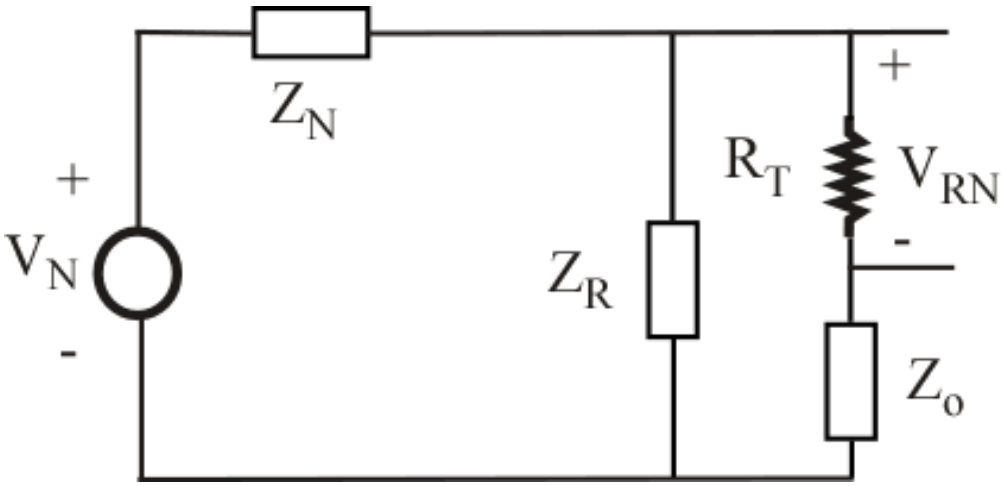
- TL is like a matched source

Power Supply Noise

$$V_{RN} = V_N \left[\frac{Z_O Z_R}{2Z_O Z_R + (2Z_O + Z_R) Z_N} \right]$$

- if $\mathbf{Z_R << Z_o}$

$$V_{RN} = \frac{V_N Z_R}{2(Z_R + Z_N)}$$



To reject power supply noise, $Z_N = Z_{GT} + Z_{GR}$ must be made as large as possible. This is accomplished by using a current-mode transmitter.

Nonideal Return Paths

- A nonideal return path will appear as an inductive discontinuity
- A nonideal return path will slow the edge rate by filtering out high-frequency components
- If the current divergence path is long enough, a nonideal return path will cause signal integrity problems at the receiver
- Nonideal return paths will increase current loop area and exacerbate EMI
- Nonideal return paths may significantly increase the coupling coefficient between signals

Signal Return Crosstalk

- Return crosstalk can be reduced with rise-time control
- As rise times get faster, every signal requires its own return ➔ might as well use differential signaling
- With voltage-mode signaling, the transmitter signal return crosstalk is a maximum
- High output impedance offers advantage and reduces transmitter return crosstalk
- For current-mode signaling, this form of crosstalk is completely eliminated

Application: Return Signal Optimization

Voltage-mode signaling with Z_o=50 Ω and rise time t_r=2 ns and Z_{RT} dominated by 5 nH inductance.

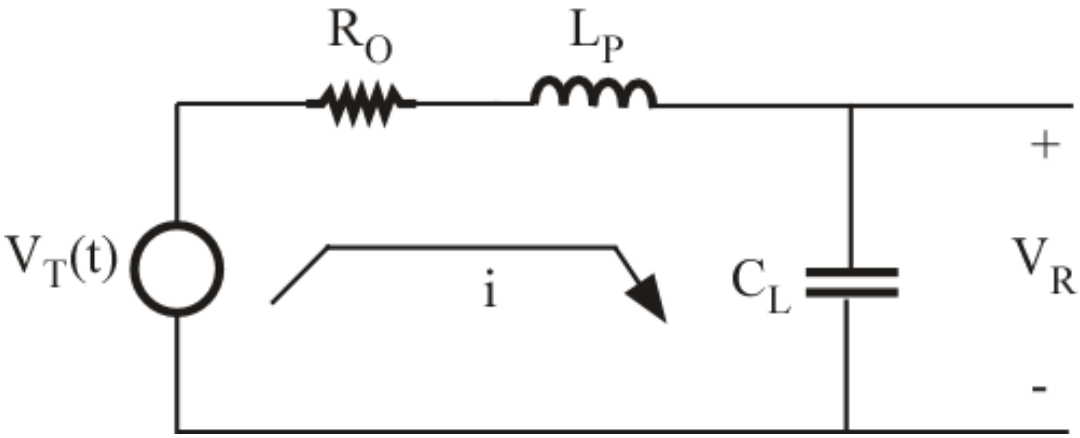
Approximate $Z_{RT}=L/t_r$= 2.5 Ω
Want k_{XRT} = 0.1

Solving for N shows that we will need 1 return for every 3 signal traces to meet the spec.

If the rise time is decreased to 1 ns, we will need 1 return for every 2 signal line to keep the same spec

If the rise time is lower than 1 ns, we will need 1 return for every signal ➔ might as well use differential signaling

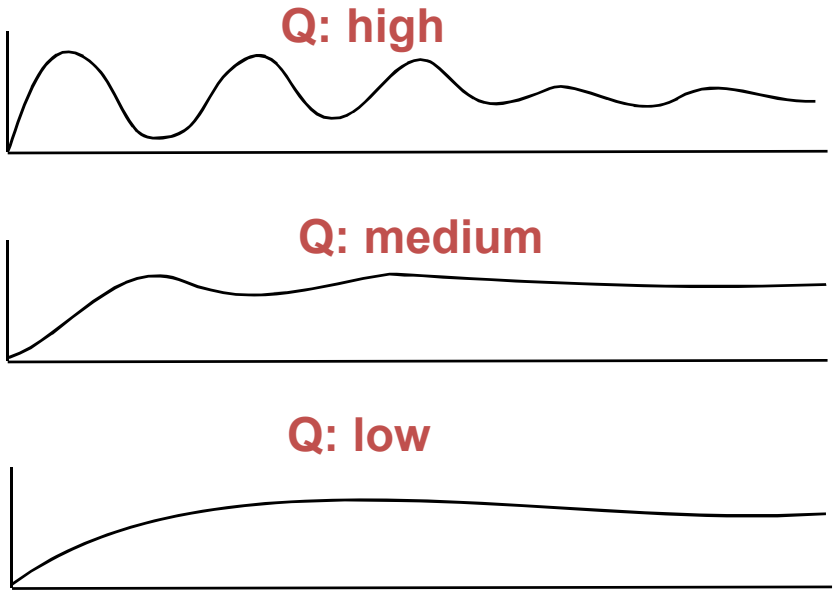
Signaling Over Lumped RLC Interconnect



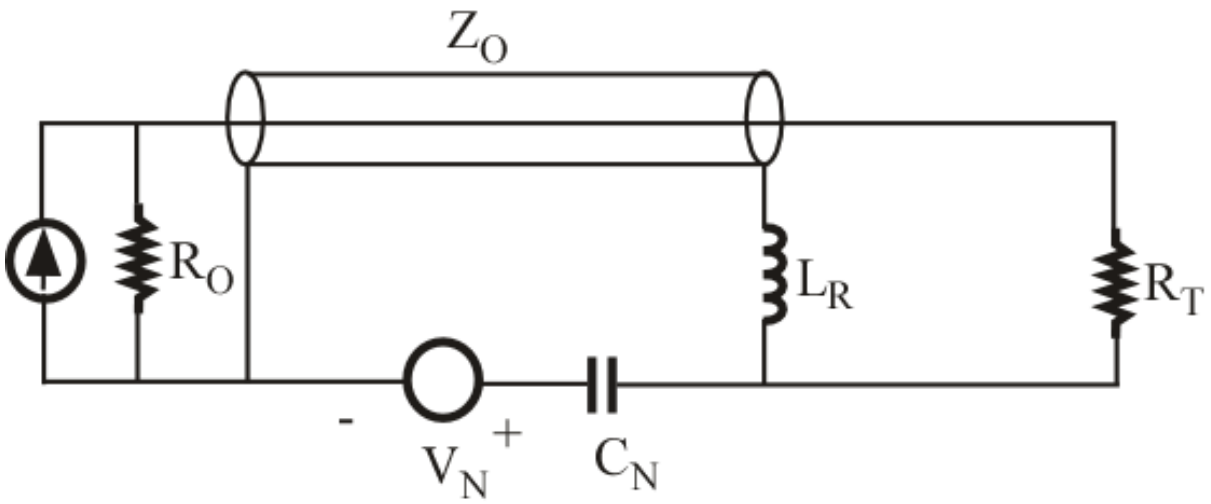
$$\omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

$$V_R(t) = 1 - \exp\left(-\frac{RT}{2L}\right)\cos(\omega t)$$

$$Q = \frac{1}{\pi R}\sqrt{\frac{L}{C}}$$



Example

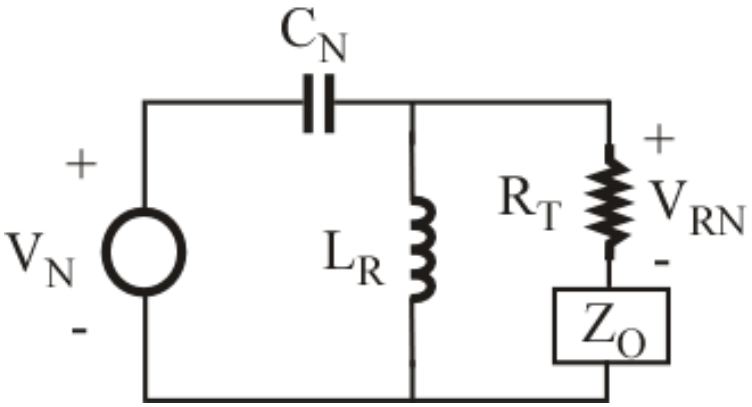


$Z_O=R_T=50\Omega$
$R_O=1\ k\Omega$
$C_N=5\ pF$

$L_R=5\ nH$
$V_N=500\ mV$

Determine the amount of supply noise V_N that appears across R_T as a function of frequency. How much signal swing is required to keep the power-supply noise less than 10% of the signal swing across the spectrum from DC to 1GHz

Example



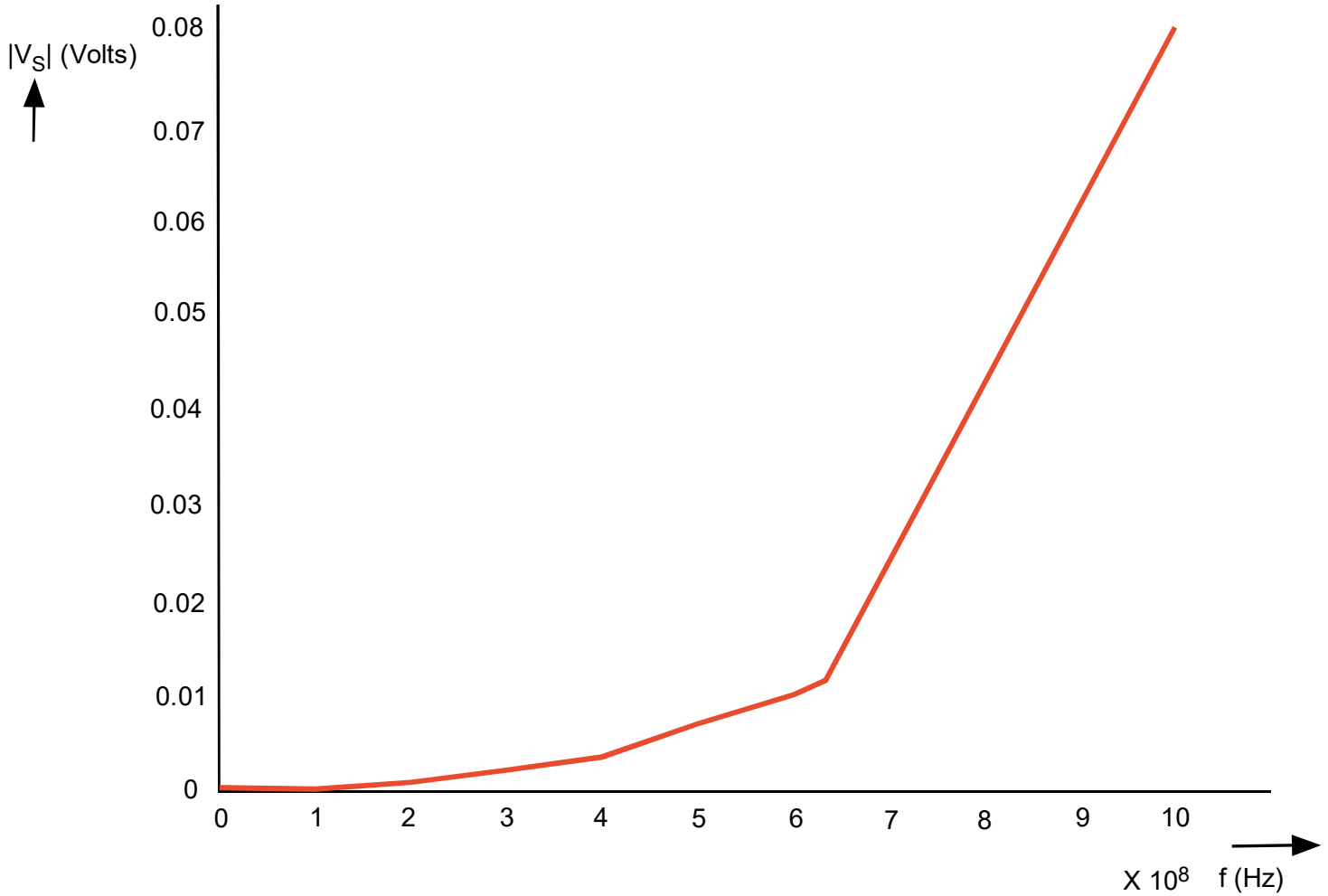
$$V_{RN} = \frac{V_N\left(Z_O j\omega L_R\right)}{2Z_O j\omega L_R + \left(2Z_O + j\omega L_R\right)\left(j\omega C\right)^{-1}}$$

$$= \frac{V_N 4\pi^2 Z_O L_R C f^2}{8\pi^2 Z_O L_R C f^2 + 2Z_O + 2\pi f L_R}$$

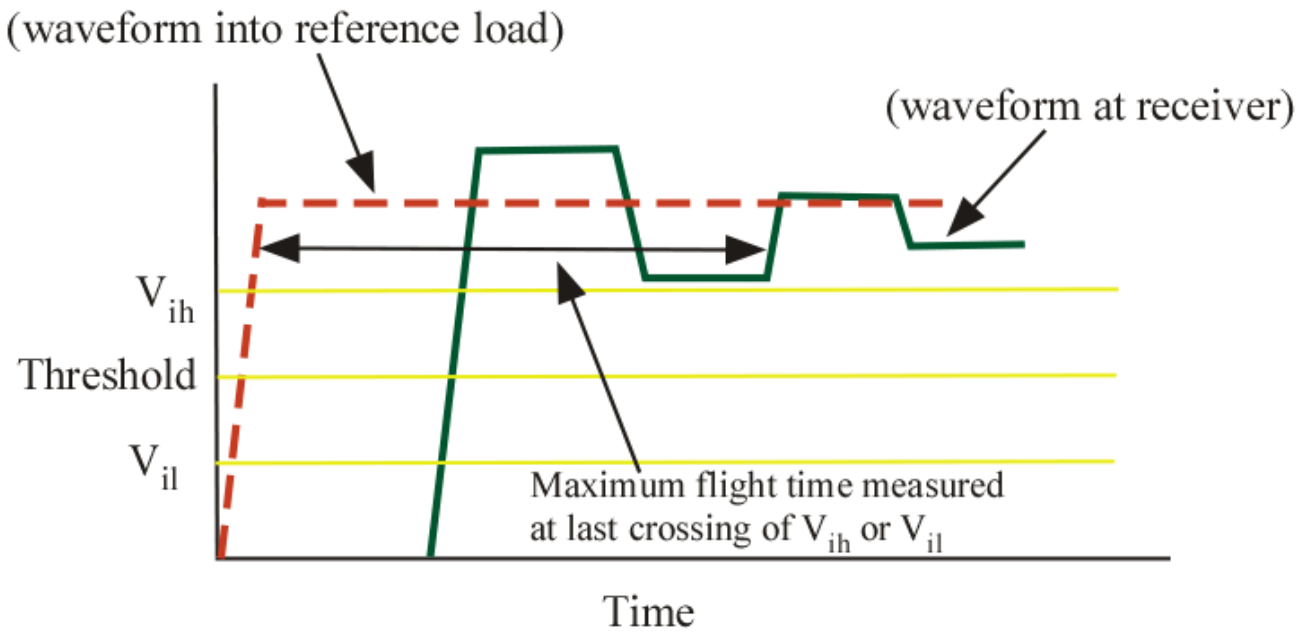
$$= \frac{-2.5\times10^{-18} f^2}{-98.5\times10^{-18} f^2 + 100 + j31.4\times10^{-9} f}$$

We want 0.1 V_s > V_{RN} ➔ VS > 10V_{RN}

Required Voltage Swing

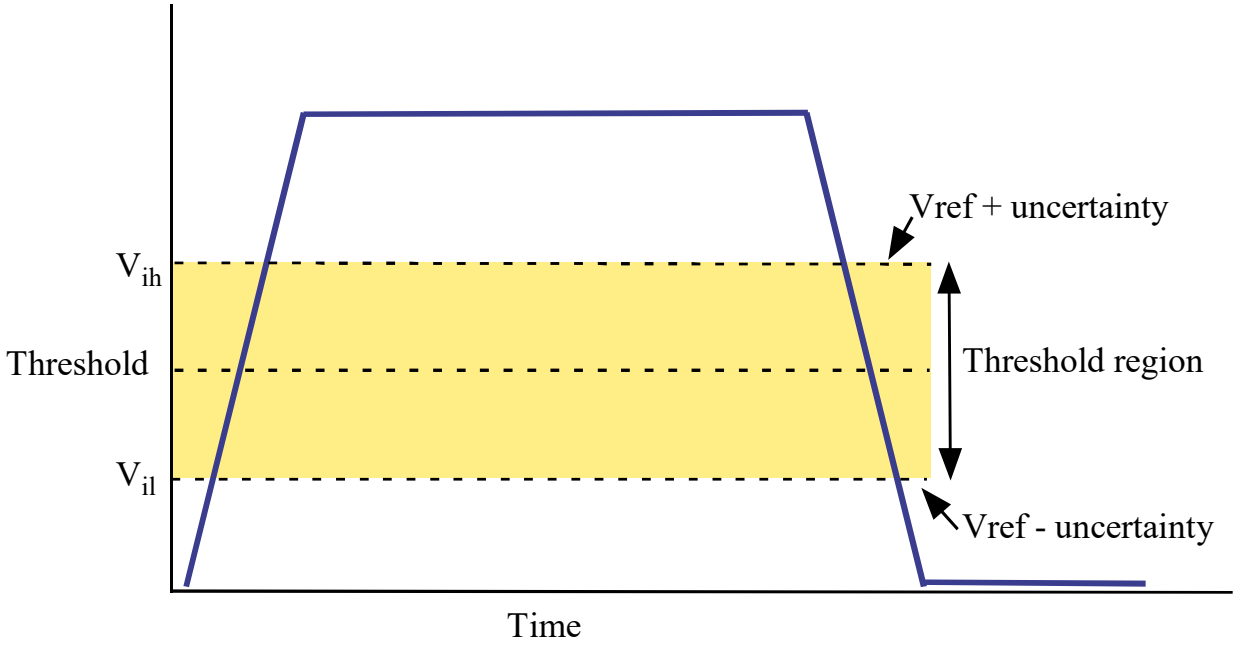


Ringback and Rise Time Control



- Violation into threshold region
- Detrimental even if threshold is not crossed
- Can exacerbate ISI
- Can be aggravated by nonlinear (time varying) terminations
- Can increase skew between signals

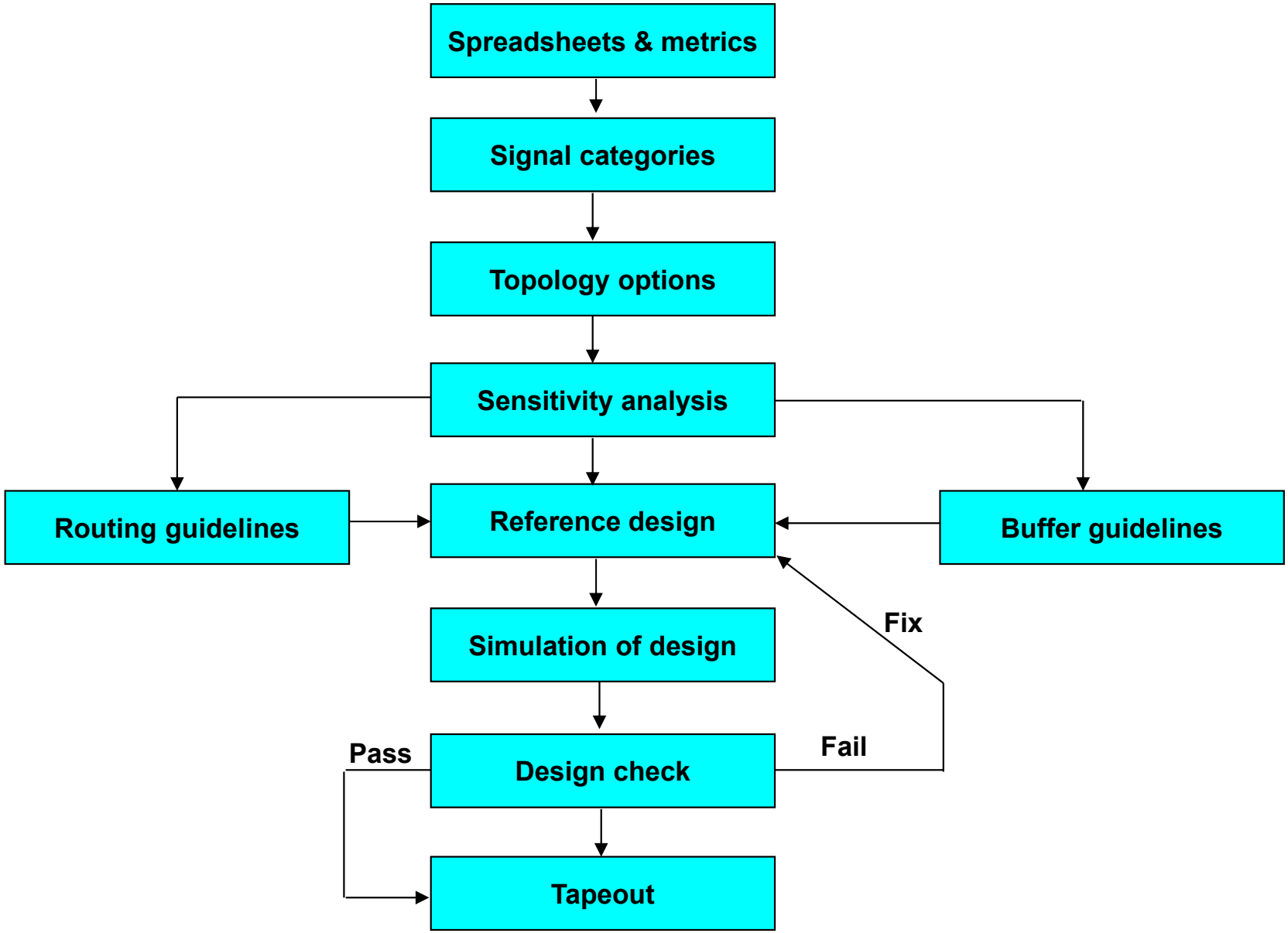
Voltage Reference Uncertainty



Major Contributors

- Power supply effects (SSN, ground bounce, rail collapse)
- Noise from IC
- Receiver transistor mismatches
- Return path discontinuities
- Coupling to reference voltage circuitry

Efficient Bus Design Methodology



Bus System Variables

- I/O capacitance
- Trace length, velocity, and impedance
- Interlayer impedance variations
- Buffer strengths and edge rates
- Termination values
- Receiver setup and hold times
- Interconnect skew specifications
- Package, daughtercard, and parameters

Differential vs Single-Ended

Line impedance: Z_o = 50 Ω
Source Resistance: R_o = 50 Ω
Lead Inductance: L = 5 nH
Pin count: P = 32
Data rate: TBR = 8GB/s

B: Bit rate per signal pin
TBR: Total bit rate
S: Number of signal pins
N: Number of return pins

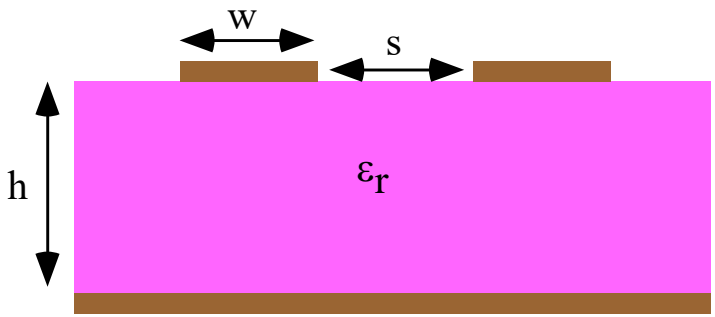
$$S+N=P$$

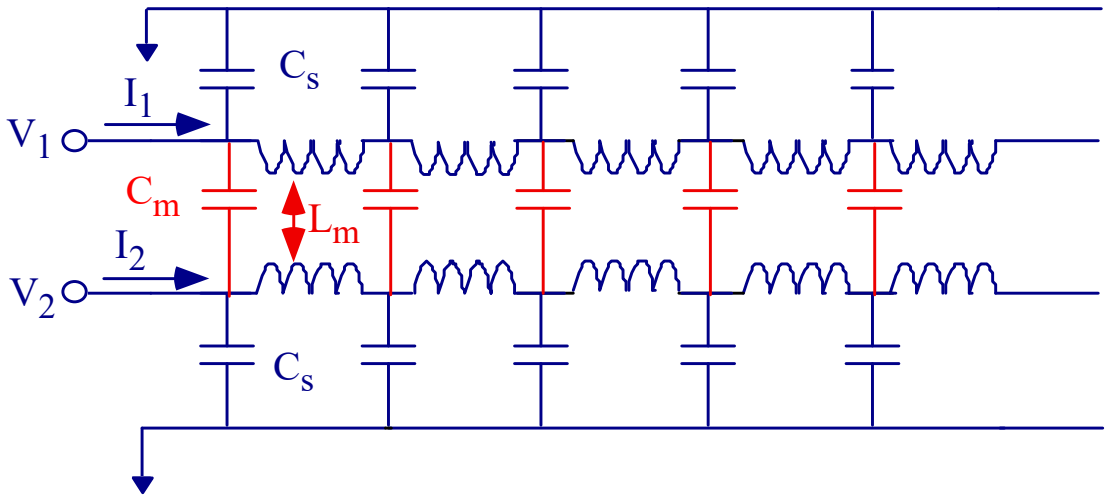
$$S*B=TBR$$

$$K_{XRT} \le \frac{(N-1)Z_{RT}}{R_O + Z_O}$$

Z_{RT} is due to the lead inductance
Z_{RT} ➔ Z_{RT}/N since there are N ground pins
Need to determine S and N

Coupled Transmission Lines





Even Mode

$$-\frac{\partial V_e}{\partial z} = \left(L_{11} + L_{12}\right)\frac{\partial I_e}{\partial t}$$

$$-\frac{\partial I_e}{\partial z} = \left(C_{11} + C_{12}\right)\frac{\partial I_e}{\partial t}$$

Add voltage and current equations

V_e : Even mode voltage $\quad V_e = \frac{1}{2}\left(V_1 + V_2\right)$

I_e : Even mode current $\quad I_e = \frac{1}{2}\left(I_1 + I_2\right)$

$$Z_e = \sqrt{\frac{L_{11} + L_{12}}{C_{11} + C_{12}}} = \sqrt{\frac{L_s + L_m}{C_s}}$$

Impedance

$$v_e = \frac{1}{\sqrt{(L_{11} + L_{12})(C_{11} + C_{12})}} = \frac{1}{\sqrt{(L_s + L_m)C_s}}$$

velocity

Odd Mode

$$-\frac{\partial V_d}{\partial z} = \left(L_{11} - L_{12}\right)\frac{\partial I_d}{\partial t}$$

$$-\frac{\partial I_d}{\partial z} = \left(C_{11} - C_{12}\right)\frac{\partial I_d}{\partial t}$$

Subtract voltage and current equations

V_d : Odd mode voltage

$$V_d = \frac{1}{2}\left(V_1 - V_2\right)$$

I_d : Odd mode current

$$I_d = \frac{1}{2}\left(I_1 - I_2\right)$$

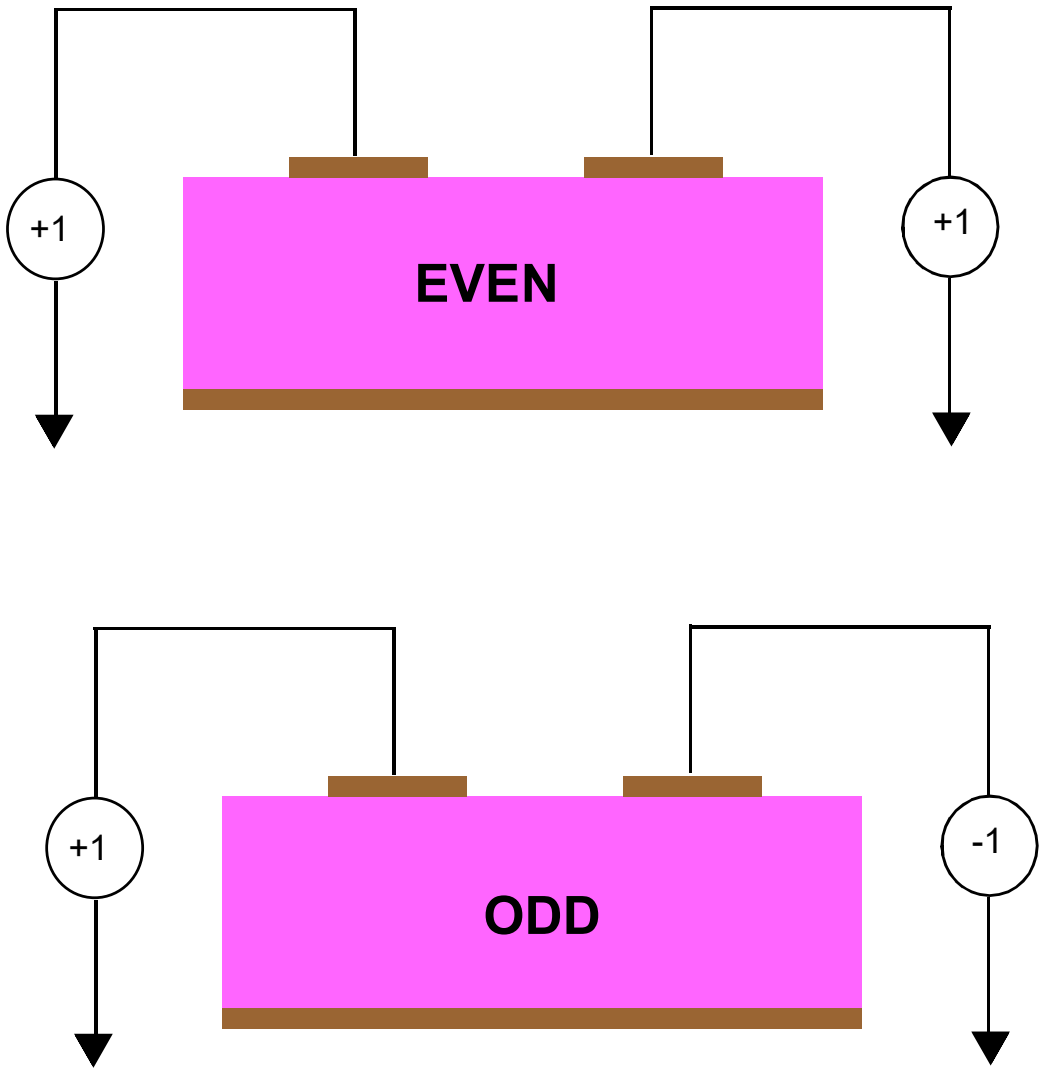
$$Z_d = \sqrt{\frac{L_{11} - L_{12}}{C_{11} - C_{12}}} = \sqrt{\frac{L_s - L_m}{C_s + 2C_m}}$$

Impedance

$$v_d = \frac{1}{\sqrt{(L_{11} - L_{12})(C_{11} - C_{12})}} = \frac{1}{\sqrt{(L_s - L_m)(C_s + 2C_m)}}$$

velocity

Mode Excitation



PHYSICAL SIGNIFICANCE OF EVEN- AND ODD-MODE IMPEDANCES

* Z_e and Z_d are the wave resistance seen by the even and odd mode travelling signals respectively.

* The impedance of each line is no longer described by a single characteristic impedance; instead, we have

$$V_1 = Z_{11} I_1 + Z_{12} I_2$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2$$

Definitions

Even-Mode Impedance: Z_e

Impedance seen by wave propagating through the coupled-line system when excitation is symmetric (1, 1).

Odd-Mode Impedance: Z_d

Impedance seen by wave propagating through the coupled-line system when excitation is anti-symmetric (1, -1).

Common-Mode Impedance: $Z_c = 0.5Z_e$

Impedance seen by a pair of line and a common return by a common signal.

Differential Impedance: $Z_{diff} = 2Z_d$

Impedance seen across a pair of lines by differential mode signal.

Mutual Impedances

Z_{11}, Z_{22} : Self Impedances

Z_{12}, Z_{21} : Mutual Impedances

For symmetrical lines,

$Z_{11} = Z_{22}$ and $Z_{12} = Z_{21}$

Even and Odd Modes

$$v_d = \frac{1}{\sqrt{(L_s - L_m)(C_s + 2C_m)}} \qquad Z_d = \sqrt{\frac{L_s - L_m}{C_s + 2C_m}}$$

$$v_e = \frac{1}{\sqrt{(L_s + L_m)C_s}} \qquad Z_e = \sqrt{\frac{L_s + L_m}{C_s}}$$

In general, odd-mode impedance is smaller than even-mode impedance.

In general, odd-mode velocity is larger than even-mode velocity.

Coupled Lines

Line Space

$$V_1 = Z_{11} I_1 + Z_{12} I_2$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

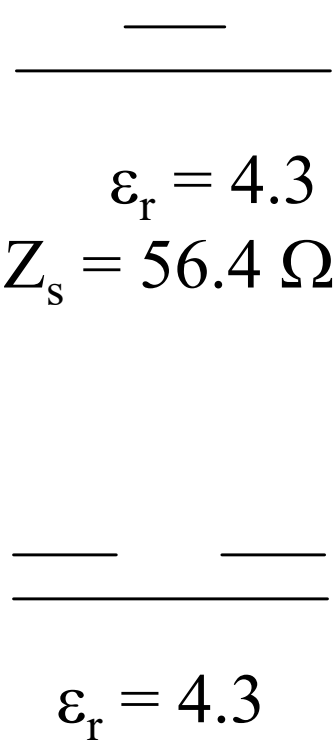
Modal Space

$$V_e = Z_e I_e$$

$$V_d = Z_d I_d$$

$$\begin{bmatrix} V_e \\ V_d \end{bmatrix} = \begin{bmatrix} Z_e & 0 \\ 0 & Z_d \end{bmatrix} \begin{bmatrix} I_e \\ I_d \end{bmatrix}$$

Example - Microstrip



Single Line

Dielectric height = 6 mils

Width = 8 mils

Coupled Lines

Height = 6 mils

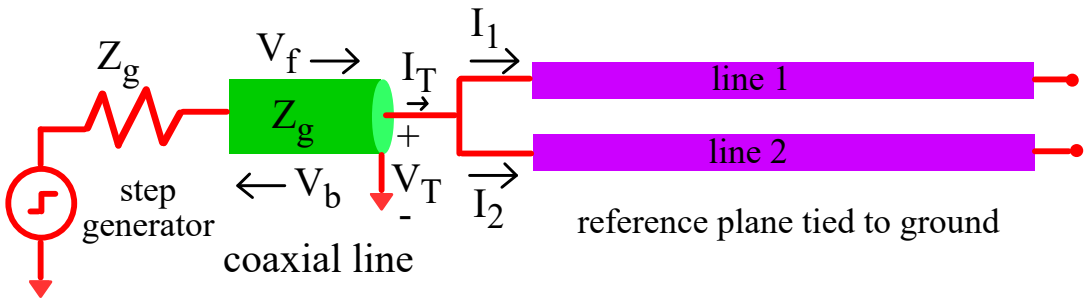
Width = 8 mils

Spacing = 12 mils

$Z_e = 68.1\ \Omega$ **$Z_d = 40.8\ \Omega$**

$Z_{11} = 54.4\ \Omega$ **$Z_{12} = 13.6\ \Omega$**

Even Mode

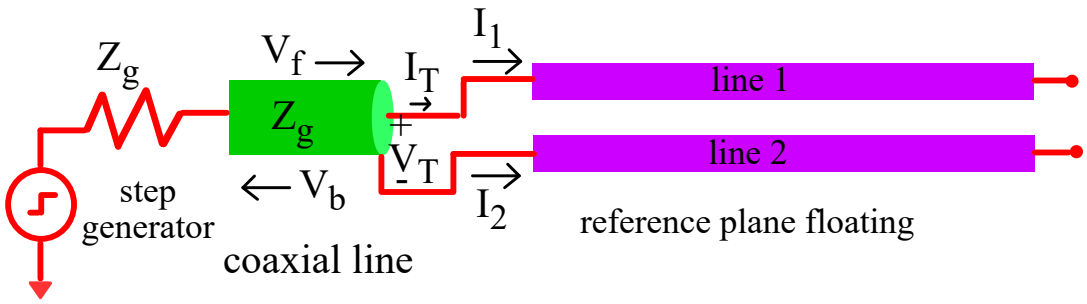


$$I_{tdr} = \left[\frac{a_e(t,0)}{Z_e} + \frac{a_d(t,0)}{Z_d}\right] + \left[\frac{a_e(t,0)}{Z_e} - \frac{a_d(t,0)}{Z_d}\right]$$

$$V_{tdr} = a_e(t,0) - a_d(t,0) \qquad a_d(t,0) = 0$$

$$\frac{V_{tdr}}{I_{tdr}} = \frac{Z_e}{2} \qquad Z_e = 2\left(\frac{1+\rho_e}{1-\rho_e}\right) Z_g \qquad v_e = \frac{2l}{\tau_e}$$

Odd Mode



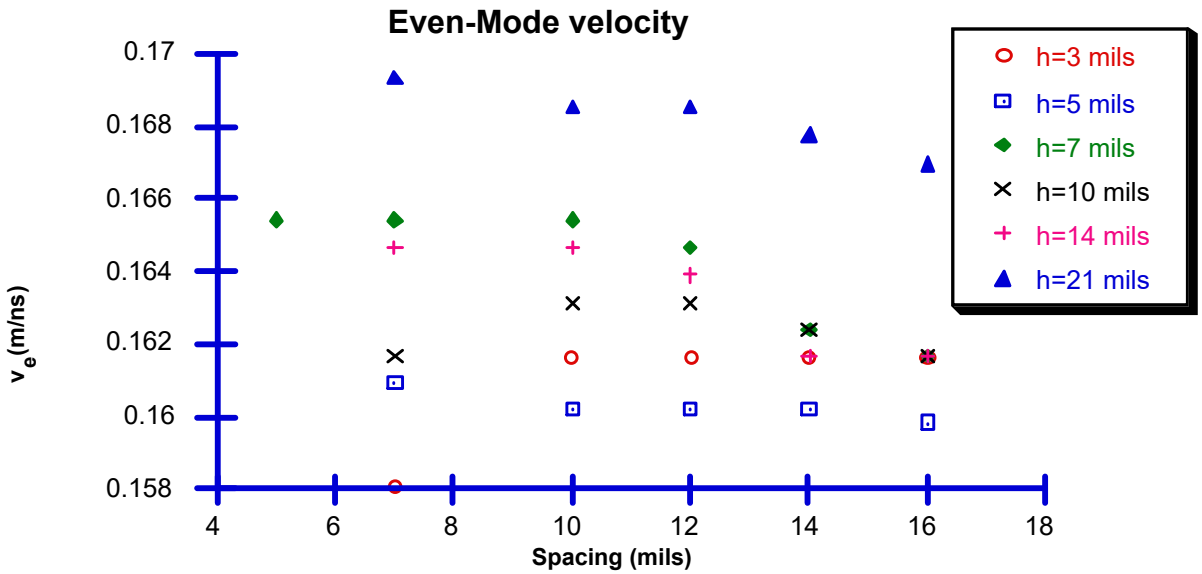
$$V_{tdr} = a_e(t,0) + a_d(t,0) - \left[a_e(t,0) - a_d(t,0)\right] = V_f + V_b$$

$$\mathrm{I}_{\mathrm{tdr}} = \left[\frac{a_e(t,0)}{Z_e} + \frac{a_d(t,0)}{Z_d}\right] \qquad \mathrm{I}_{\mathrm{tdr}} = -\left[\frac{a_e(t,0)}{Z_e} - \frac{a_d(t,0)}{Z_d}\right]$$

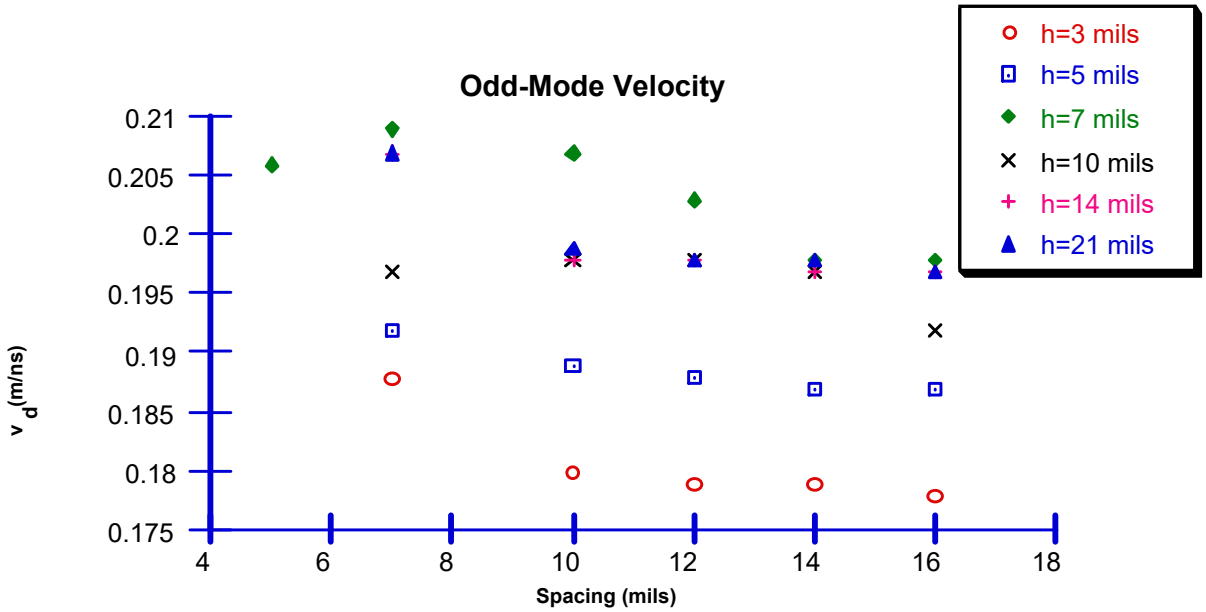
$$a_e(t,0) = 0, \qquad \frac{V_{tdr}}{I_{tdr}} = 2Z_d$$

$$Z_d = \frac{1}{2}\left(\frac{1+\rho_d}{1-\rho_d}\right)Z_g, \qquad \mathrm{v_d} = \frac{2l}{\tau_d}$$

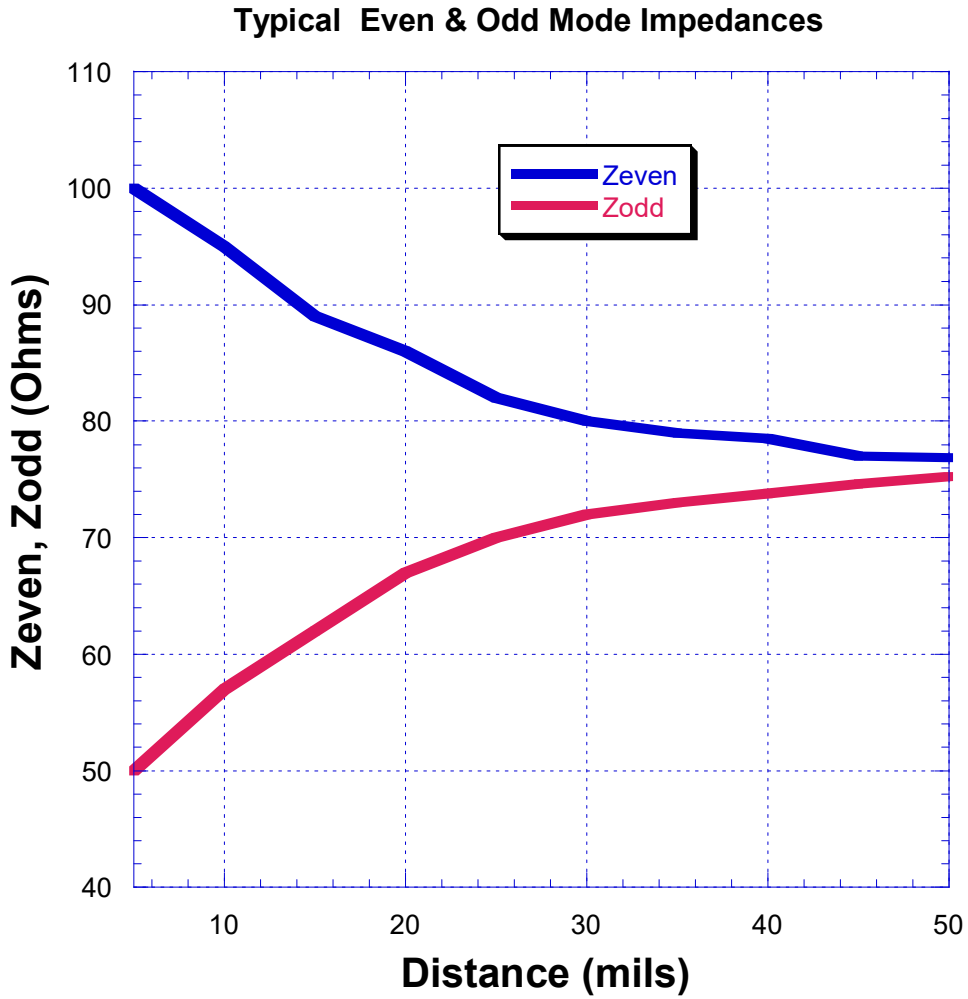
Measured Even-Mode Velocity



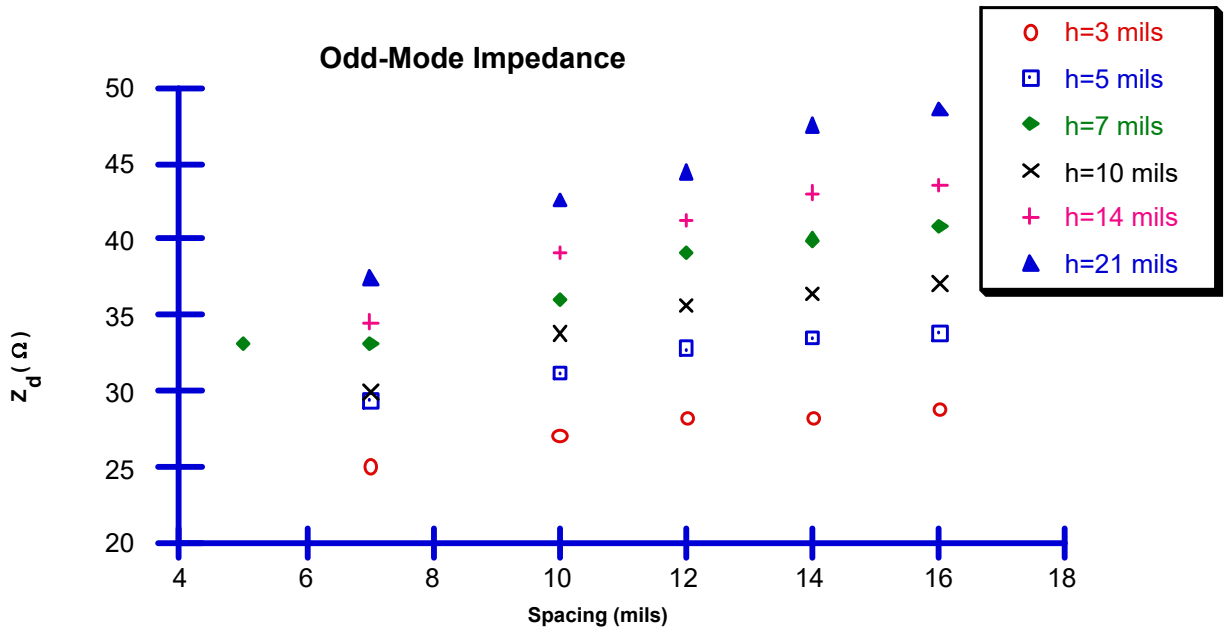
Measured Odd-Mode Velocity



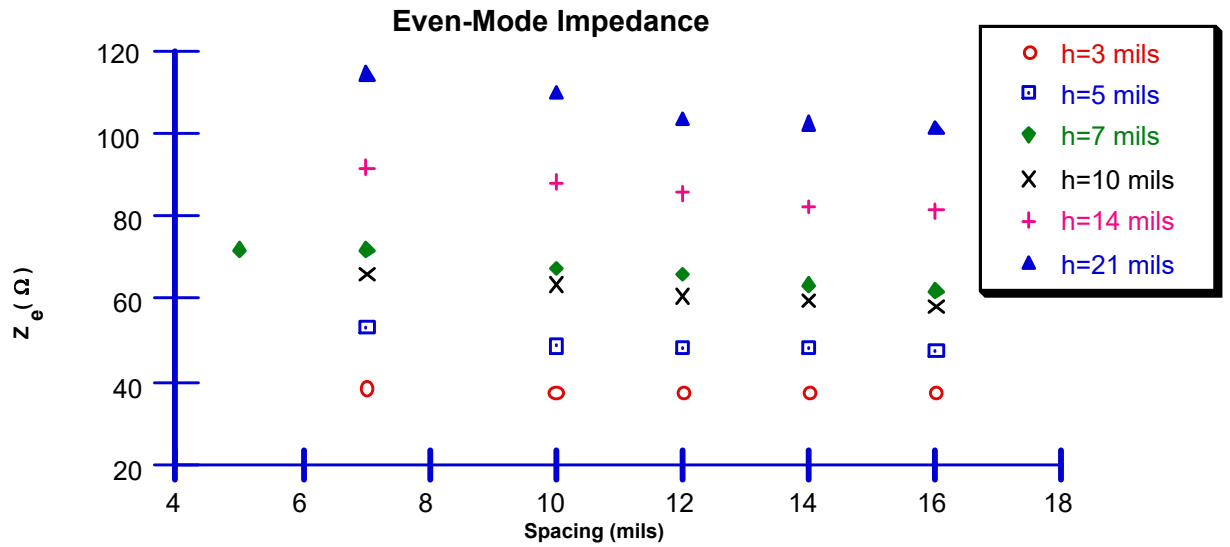
Even and Odd-Mode Impedances



Measured Odd-Mode Impedance



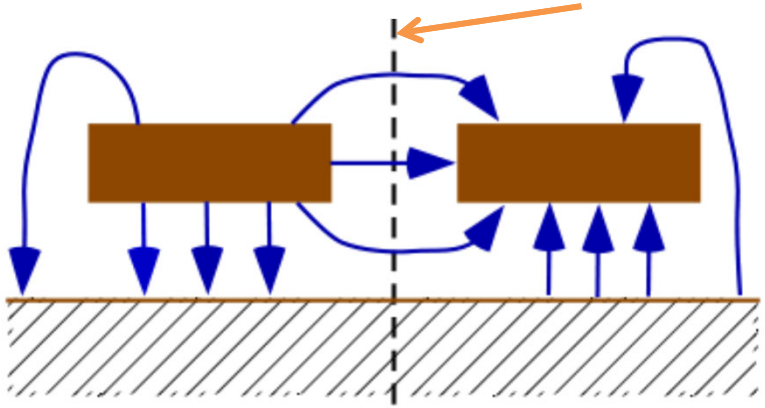
Measured Even-Mode Impedance



Virtual Reference Plane

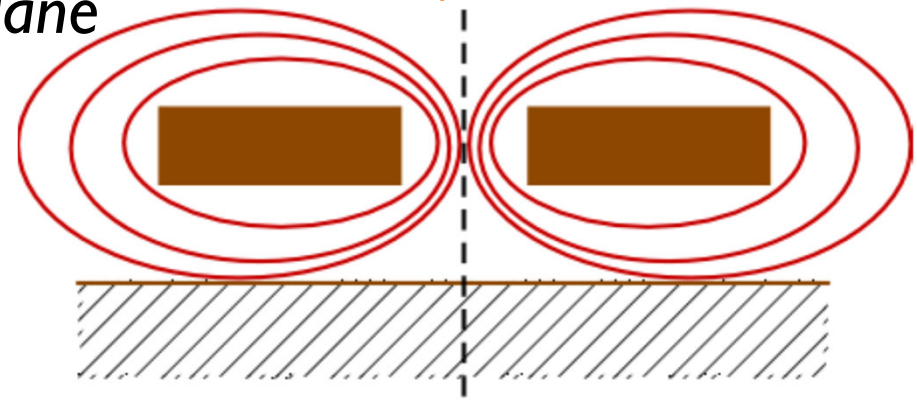
For odd modes, there exists a virtual reference plane between the conductors

Electric field is perpendicular to virtual plane



Electric Field

Magnetic field is tangent to virtual plane



Magnetic Field

Virtual reference plane

Low-Voltage Differential Signaling (LVDS)

Definition: Method to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces or a balanced cable

Criteria for high-performance communication

- **Bandwidth**
- **Low Power**
- **Low Noise**

Solution exists for very short and very long distances; however for board-to-board or box-to-box, this is a challenge

Why LVDS?

1. Differential transmission is less susceptible to common mode noise

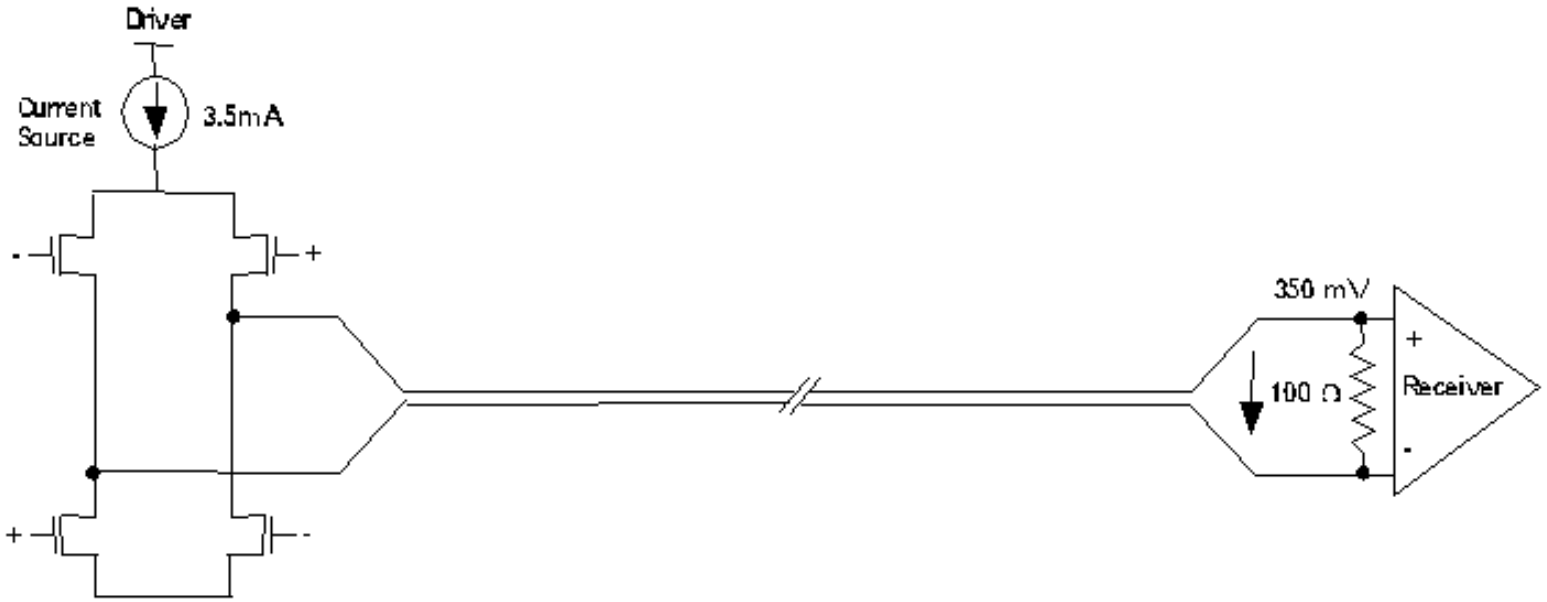
2. Consequently they can use lower voltage swings

3. In PC board (microstrip) odd-mode propagation is faster

LVDS Attributes for EMI

1. Low output voltage swing
2. Slow edge rates
3. Odd-mode operation (magnetic fields cancel)
4. Soft output corner transitions

LVDS Driver and Receiver



- Majority of current flows across 100-ohm resistor
- Switching changes the direction of current
- Logic state determined by current direction

LVDS Standard

- **Maximum Switching Speed**
  - Depends on line driver
  - Depends on selected media (type and length)

- **LVDS Saves Power**
  - Power dissipated in load is small
  - LVDS devices are in CMOS=>low static power
  - Lowers system power through current-mode

- **Design Practices**
  - Matching is critical
  - Preserve balance

Differential Signaling Technologies

	RS-422	PECL	LVDS
Differential Driver Output Voltage	±2 to ±5V	±600-1000 mV	±250-450 mV
Receiver Input Threshold	±200 mV	±200-300mV	±100 mV
Data Rate	<30Mbps	>400Mbps	>400Mbps
Supply Current Quad Driver (no load, static)	60 mA (max)	32-65mA (max)	8.0mA
Supply Current Quad Receiver (no load, static)	23mA (max)	40mA (max)	15mA (max)
Propagation Delay of Driver	11ns (max)	4.5ns (max)	1.7ns (max)
Propagation Delay of Receiver	30ns (max)	7.0ns (max)	2.7ns (max)
Pulse Skew (Driver or Receiver)	N/A	500ps (max)	400ps (max)