ECE 546
Lecture - 23
PLL & Clocks

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Motivation

Clock generation is a fundamental function in high-speed digital and mixed-signal systems. In applications such as:

- **Phase-Locked Loops (PLLs)**
- **Clock and Data Recovery (CDR)**
- **SerDes links**
- **Memory interfaces (DDR, HBM)**

quality of the clock directly determines system performance.

Why need PLLs?

- Reduces jitter.
- Reduces clock-skew in high-speed digital ckts.
- Instrumental in frequency synthesizers.
- Essential building block of CDRs.

Phase Locked Loop (PLL)

A PLL is a voltage-controlled oscillator which has its frequency controlled by an external source

- Loop oscillator frequency can be same or multiple of reference frequency
- If reference signal comes from a crystal oscillator, other frequencies can be derived with same stability as crystal frequency
- Loop oscillator frequency will track that of input
- Principle used in FM and FSCK demodulators tracking filters and instrumentation

Phase Locked Loop (PLL)

A PLL synchronizes the output phase and frequency of a controlled oscillator with the phase and frequency of a reference oscillator

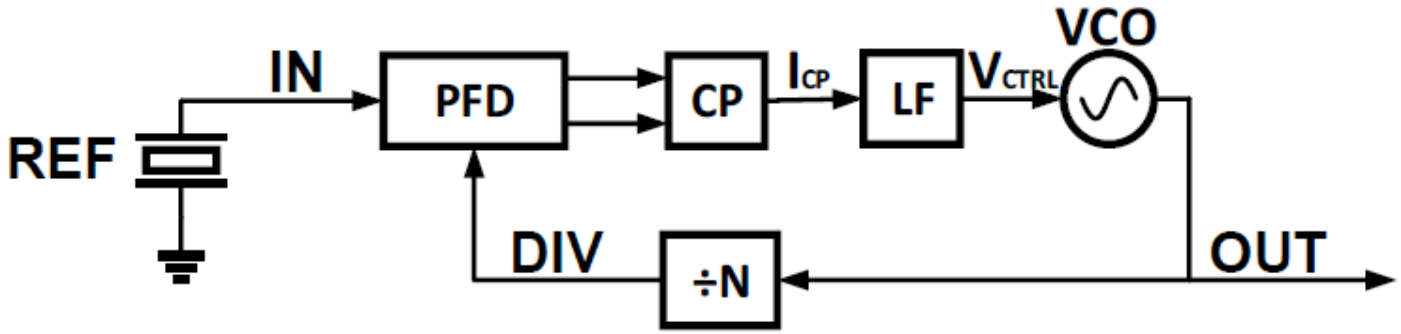
The task of the PLL is to maintain coherence between the reference signal frequency and the output frequency via phase comparison

Functional Blocks

- Voltage controlled oscillator (VCO)
- Phase detector (PD or PFD)
- Loop filter
- Feedback divider (=1 for the simplest case)

Clock Synthesizer

- PLL based clock-generating circuit needed to have a high-speed system master clock at the TX side.
- Reference clock generated by piezoelectric crystal but can only produce a stable, low-jitter clock in the MHz range.
- Basic Idea: take the reference signal and generate a scaled up clock at a higher frequency by eliminating static phase errors using a negative feedback control system in form of PLL.



PLL Architecture

- **PFD → CP → LF → VCO → Divider**

PLL Architecture:

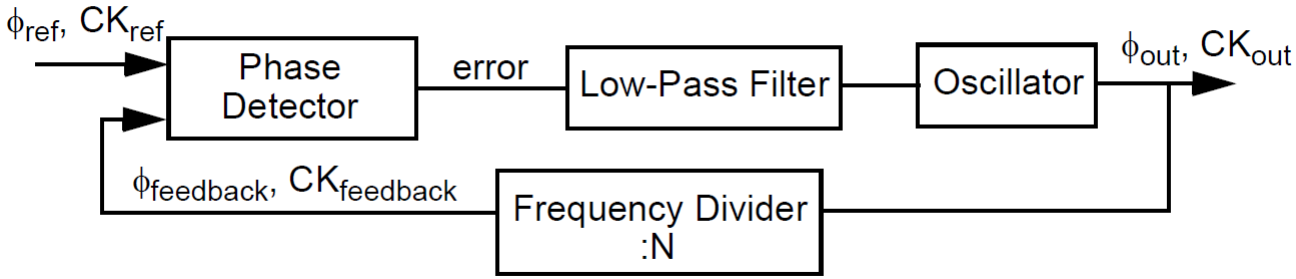
- Phase Detector (PD)
- Charge Pump (CP)
- Loop Filter (LF)
- Voltage-Controlled Oscillator (VCO)
- Frequency Divider

CDR Architecture:

- Phase Detector (linear or bang-bang)
- Loop filter
- VCO / DCO
- Sampler / slicer

PLL Overview

Basic PLL Block Diagram:



- Closed-loop feedback system that synchronizes the output CLK phase with that of the reference CLK.
- Tracks phase changes w/i the specified BW.
- Idea is that the PD (Phase Detector) will compare the reference CLK phase with that generated by the VCO.
  - Goal: Stabilize $\Delta\phi_e^{SS} \rightarrow 0$ such that VCO output CLK and reference CLK are locked at same frequency and phase.
  - Tracks low-frequencies but rejects high-frequencies.

CDR Architecture

- **Bang-bang PD → LF → VCO → Sampler**

PLL Architecture:

- Phase Detector (PD)
- Charge Pump (CP)
- Loop Filter (LF)
- Voltage-Controlled Oscillator (VCO)
- Frequency Divider

CDR Architecture:

- Phase Detector (linear or bang-bang)
- Loop filter
- VCO / DCO
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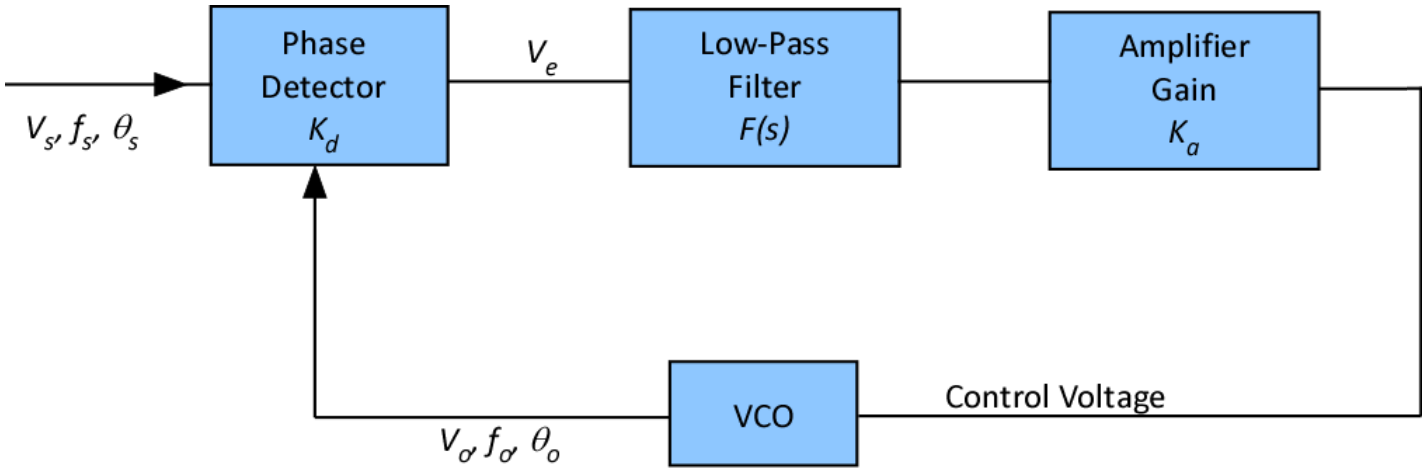
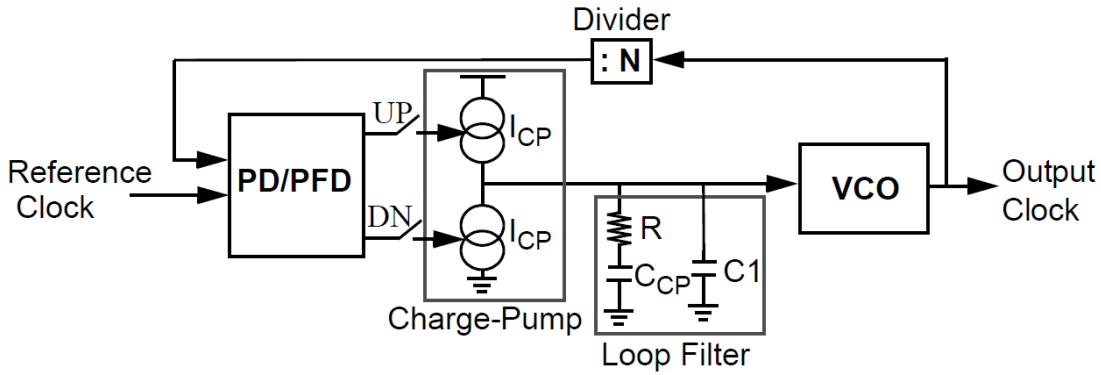
Components of PLL



- Loop is in lock when frequencies of input and VCO are identical ($f_s = f_o$)
- If input frequency changes, phase difference must change enough to produce control voltage V_d that produce equality in frequency

PLL Building Blocks

Basic PLL Components:



- PD/PFD ~ Phase/Phase+Frequency Detector
- CP ~ Charge pump circuit
- LF ~ Loop-Filter
- VCO ~ Voltage controlled oscillator
- Frequency Divider

Phase Detector

- **XOR, PFD, Bang-bang**

Types:

1. XOR detector
2. Phase-frequency detector (PFD)
3. Bang-bang detector (CDR)

Tradeoffs:

Type	Linearity	Capture Range	Complexity
XOR	Poor	Small	Low
PFD	Good	Large	Medium
Bang-bang	Nonlinear	Large	High

Phase Detector Mathematics

The phase detector is a mixer with

$$v_1(t) = V_1 \cos(\omega_{RF} t + \theta_1)$$

$$v_2(t) = V_2 \cos(\omega_{LO} t + \theta_2)$$

After mixing

$$v_p(t) = \frac{V_1 V_2}{2}\left[\begin{array}{l}\cos(\omega_{LO} t - \omega_{RF} t + \theta_2 - \theta_1) \\ +\cos(\omega_{LO} t + \omega_{RF} t + \theta_2 + \theta_1)\end{array}\right]$$

Phase Detector Mathematics

Define

$$\omega_{beat} = \omega_{LO} - \omega_{RF}$$

$$V_{pb} = \frac{V_1 V_2}{2}$$

$$\theta_e = \theta_2 - \theta_1$$ **Phase-error difference between signal 1 and signal 2**

We get

$$v_p(t) = V_{pb} \cos\left(\omega_{beat} t + \theta_e\right)$$

Phase Detector Mathematics

We have

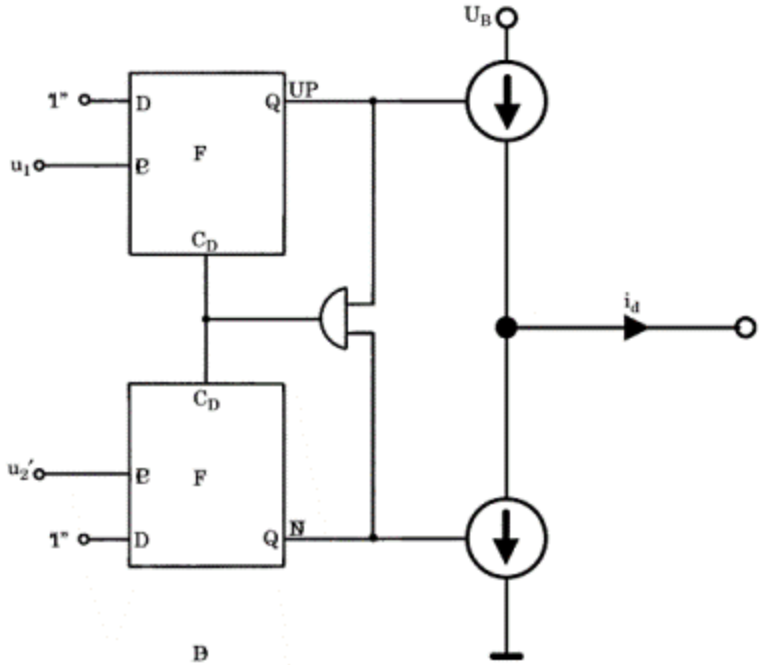
$$v_p(t) = V_{pb}\cos(\omega_{beat}t + \theta_e)$$

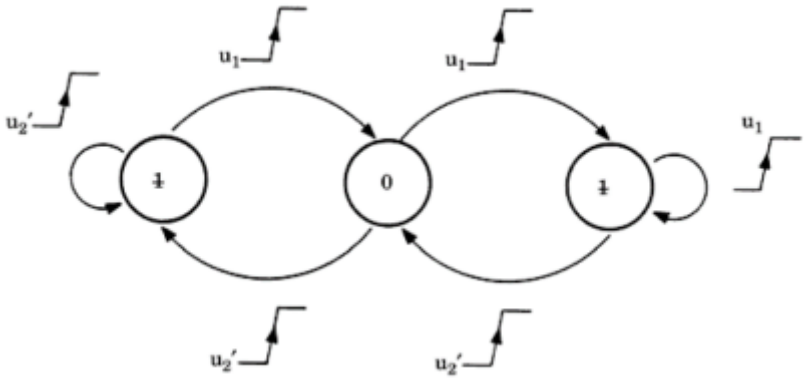
When the loop is in lock, ω_{beat}= 0 and v_p is a DC voltage. When the loop is not in lock, v_p is a voltage that tries to pull the VCO into synchronism with the input signal.

Actual process of acquiring lock is nonlinear

PFD Theory

1. PFD is needed to adjust the control voltage for VCO according to the phase difference between the VCO output and reference frequency

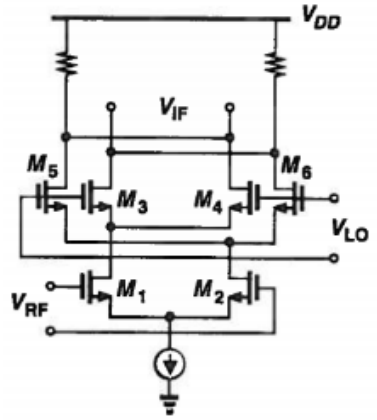




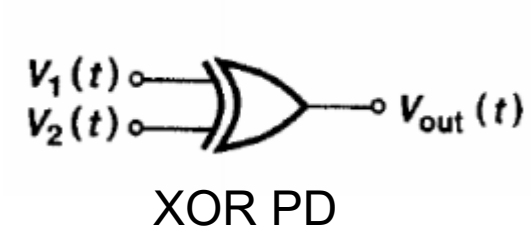
2. PFD can be seen as a state machine with three states. It will change the control voltage of VCO according to its current state and phase/frequency difference will cause state transition.

PD/PFD Circuits

Common PD Implementations:

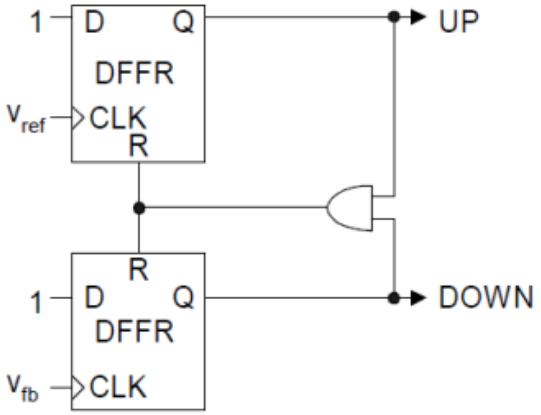


Gilbert-cell Mixer



XOR PD

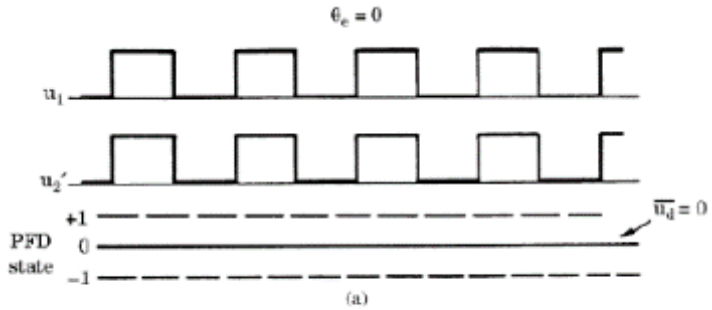
Common PFD Implementations:



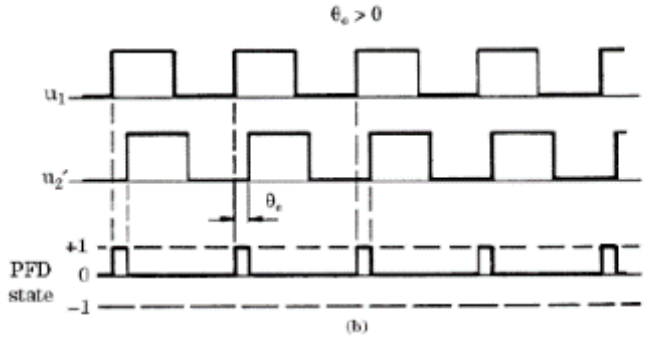
- PD/PFD are strictly digital circuits in high speed SerDes transceivers.
- Ideal PD is a "multiplier" in time-domain, ex: Mixer
- Analog PD → High Jitter, noise.
- XOR PD → sensitive to clock duty cycle
- PFD ~ best to lock phase and frequency!

PFD Analysis

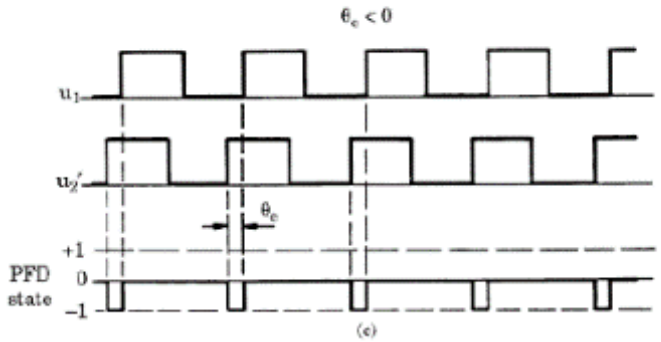
1. PFD is in state 0 with no phase difference.



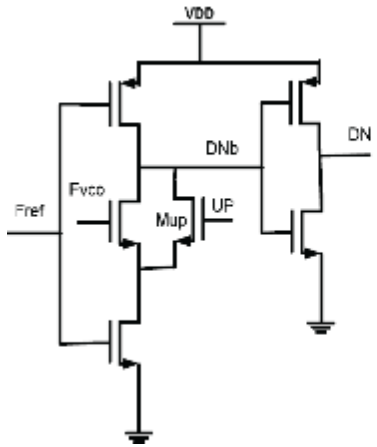
2. PFD is in state 1 with positive phase difference.



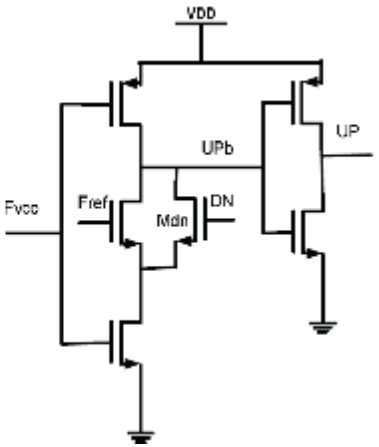
3. PFD is in state -1 with negative phase difference.



PFD Design Overview

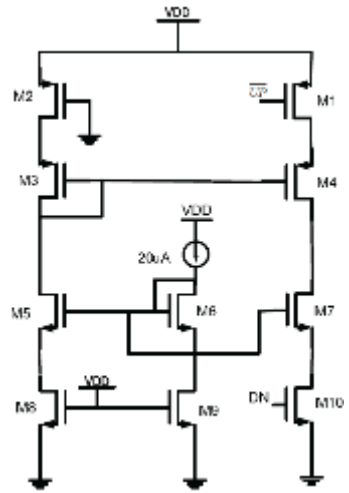


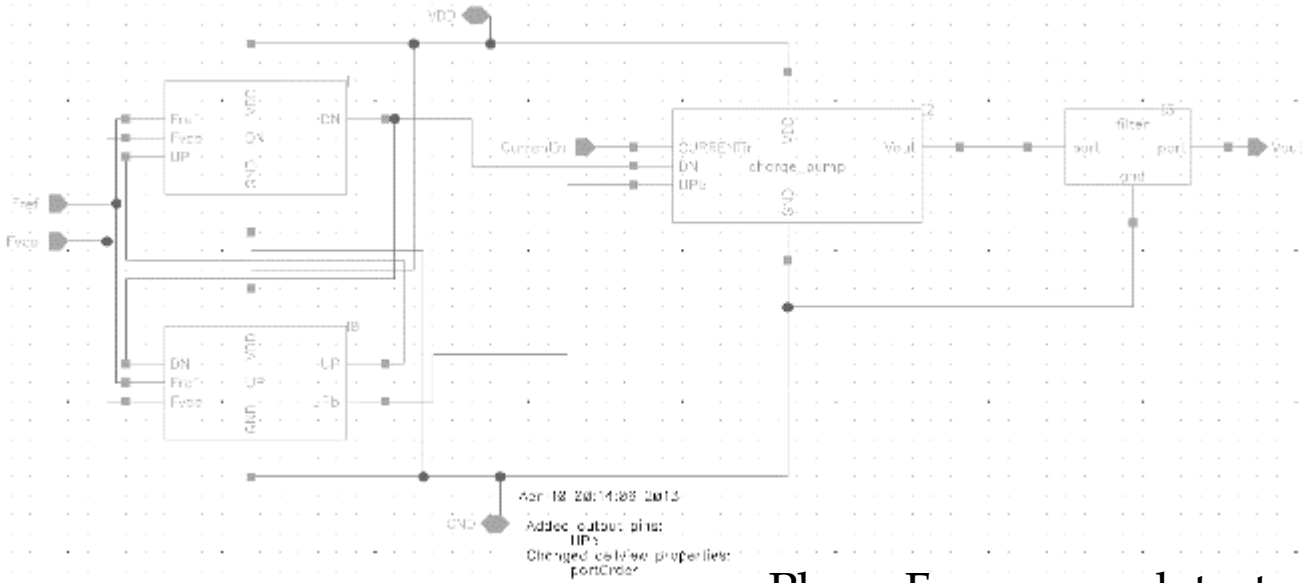
Down circuit



UP circuit

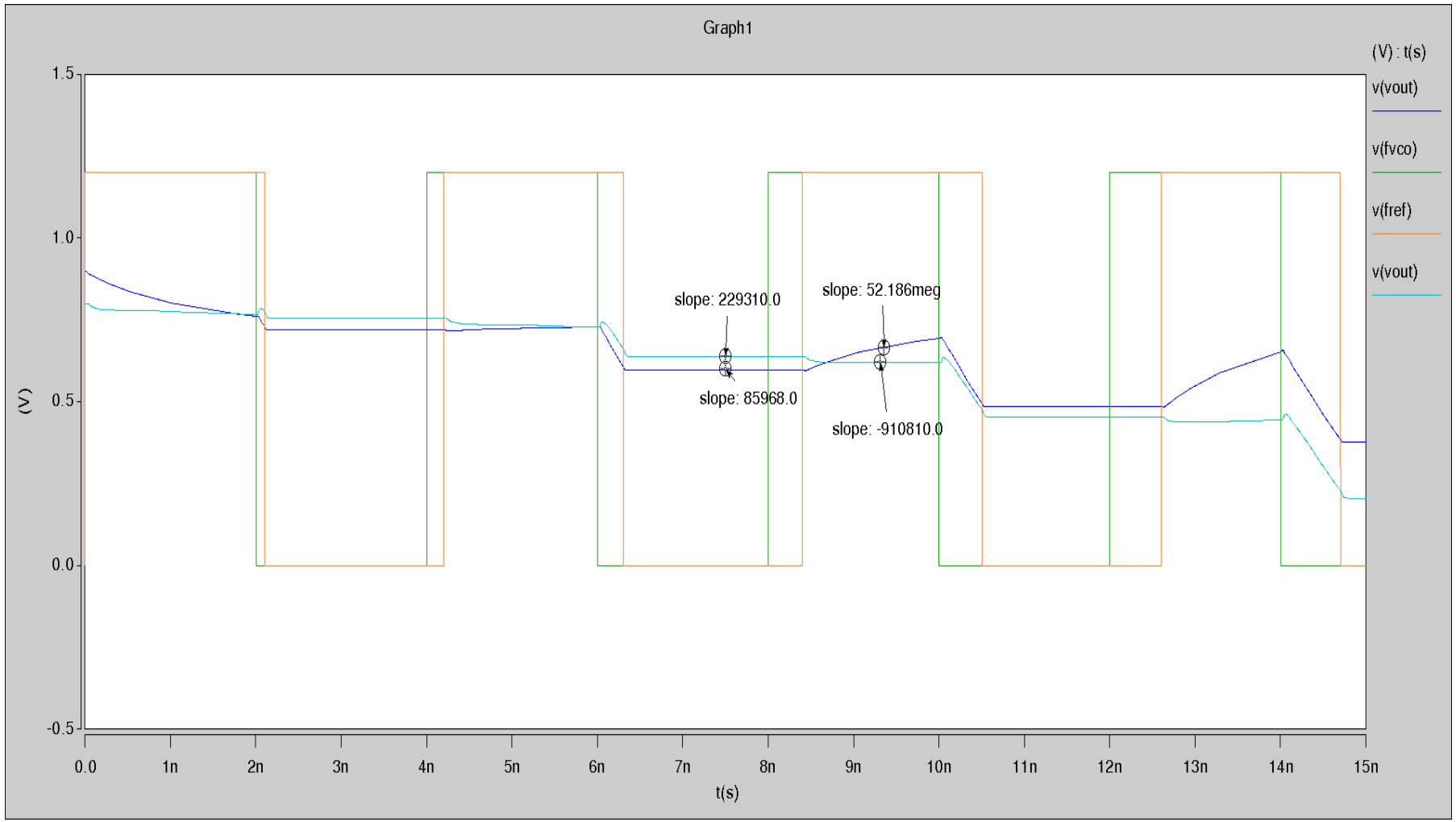
Charge pump





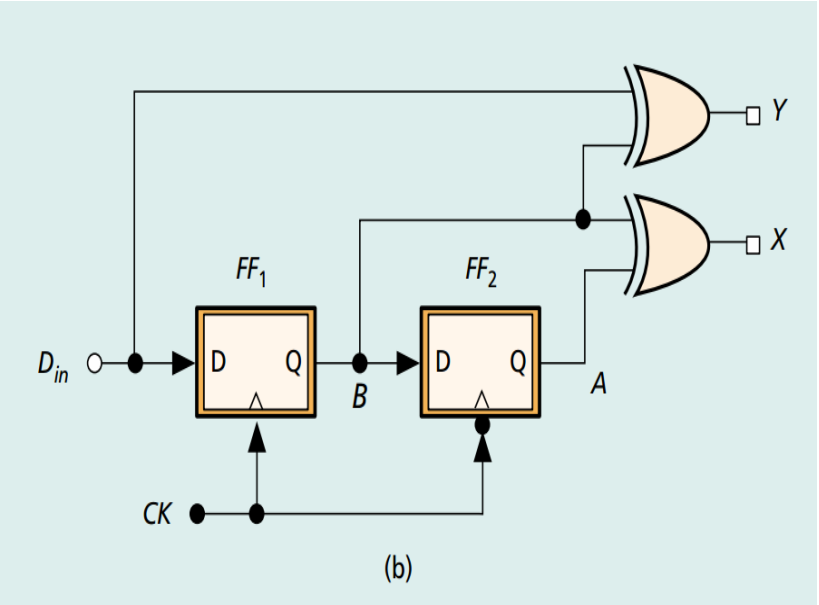
Phase Frequency detector

PFD Simulation



The Hogge Phase Detector

- Two Functions
  - Transition detection
  - Phase Detection



Charge Pump

Converts phase error to current.

Non-idealities:

- Current mismatch → static phase error
- Charge sharing
- Clock feedthrough

Design Rules:

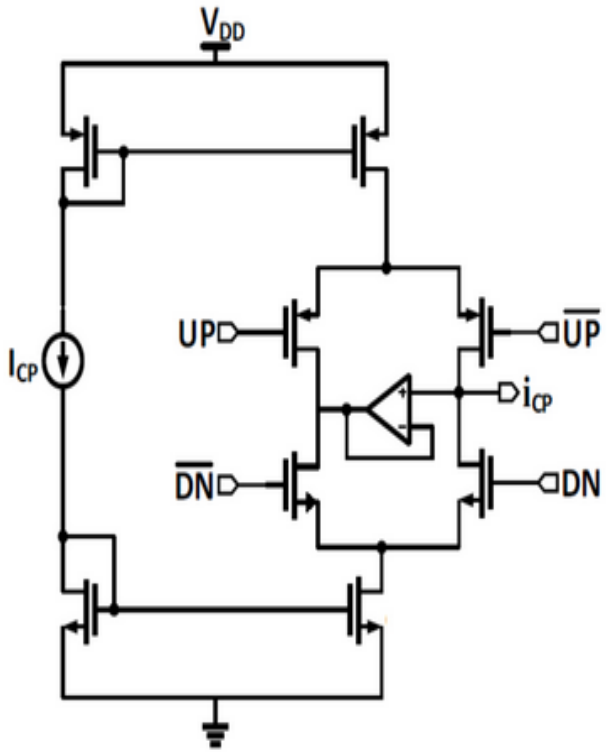
- Match up/down currents carefully
- Use cascode for output impedance
- Minimize switching transients

Current mismatch is critical

The Charge Pump

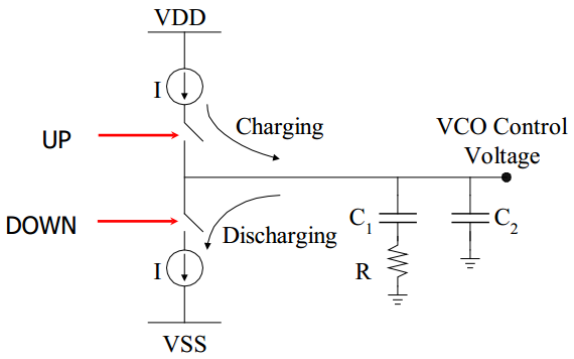
- Combination of current source and sink
- Converts PD output

UP	DN	Io
0	0	0
1	0	Icp
0	1	-Icp

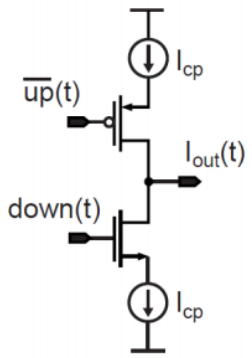


Charge-Pump Circuit

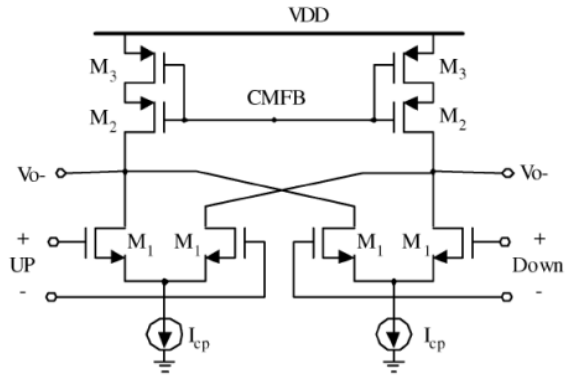
Common CP Implementations:



Single-Ended



Fully Differential



- Used in conjunction with PFD over PD+LF combo. b/c:
  - Higher capture/lock acquisition range of PLL
  - $\Delta\phi_e^{SS} = 0$ provide no device mismatch exists.
  - Provide infinite gain for a static phase-error

Loop Filter

Controls bandwidth and stability

Types:

- Passive RC
- Active filter

Function:

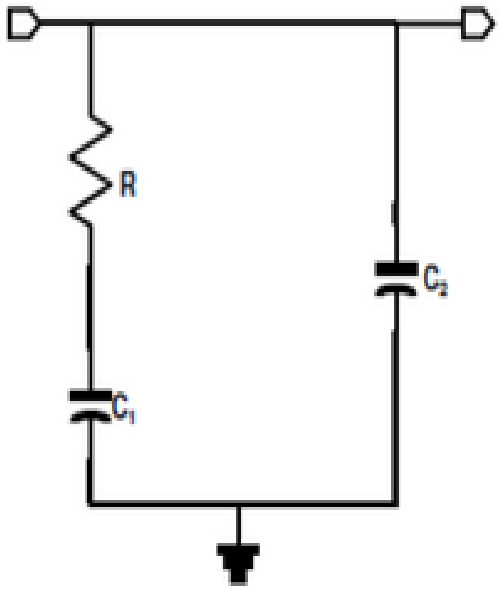
- Sets loop bandwidth
- Controls stability

Tradeoffs:

- Narrow bandwidth → low jitter, slow lock
- Wide bandwidth → fast lock, more noise

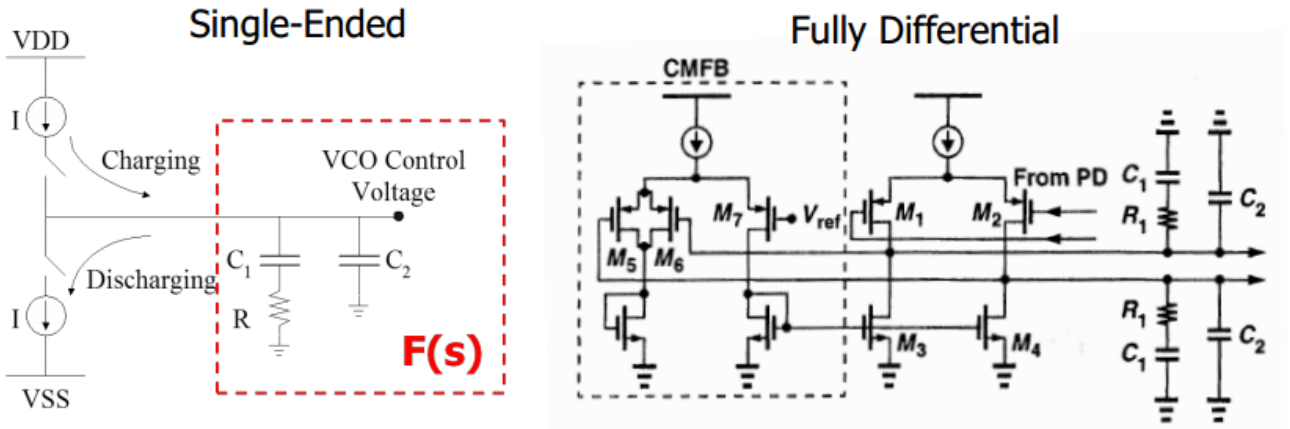
The Loop Filter

- Low-pass for rejection of high frequency noise
- Forms the control voltage of the VCO



Loop-Filter

Common LF Implementations:

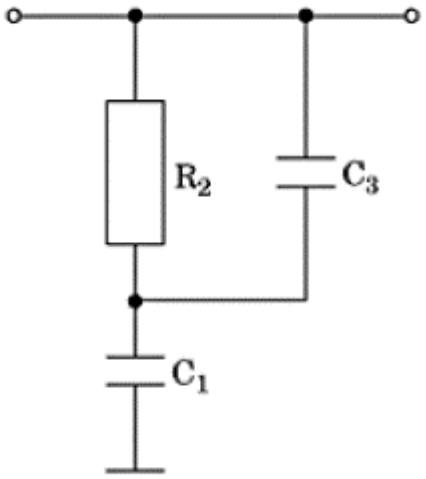


- Extracts average of PD error signals generate VCO control voltage.
- Integrates low-frequency phase-errors on C1 to set avg. freq.
- R adds thermal noise, C_1 determines loop BW, C_2 smoothens control voltage ripple.

Loop-Filter Design

1. Needed to filter out high frequency noise generated by PFD

2. Due to the superior performance of PFD, only a passive second order RC low pass filter is needed.



Low pass filter for current input

Where $R_2 = 70.18K\Omega, C_1 = 72.56\text{f}F, C_3 = 18.136\text{f}F;$

Assuming $K_0 = 4.5\,GHz/V\,;\; K_P = 3.183\mu A/rad\,, N = 8, \omega_T = 25\text{MHz}$

Voltage-Controlled Oscillator

Output frequency is expressed by:

$$\omega_o = \omega_f + K_o V_d \ (rad/s)$$

Total angle of VCO can be described by:

$$\theta(t) = \int_0^t \left(\omega_f + \Delta\omega\right) dt = \omega_f t + \theta_o(t)$$

$\Delta\omega$ is deviation from ω_f

$$\theta_o(t) = \int_0^t \Delta\omega dt$$

Ring VCO

- **Compact, noisy, wide tuning**

Structure:

- Odd number of inverters
- Frequency controlled by delay

Advantages:

- Compact
- Wide tuning range
- Fully CMOS-compatible

Disadvantages:

- High phase noise
- Supply sensitivity

Frequency:

$$f = \frac{1}{2N \cdot t_d}$$

LC VCO

- **Low phase noise, large area**

Structure:

- LC tank + cross-coupled pair

Advantages:

- Low phase noise
- High spectral purity

Disadvantages:

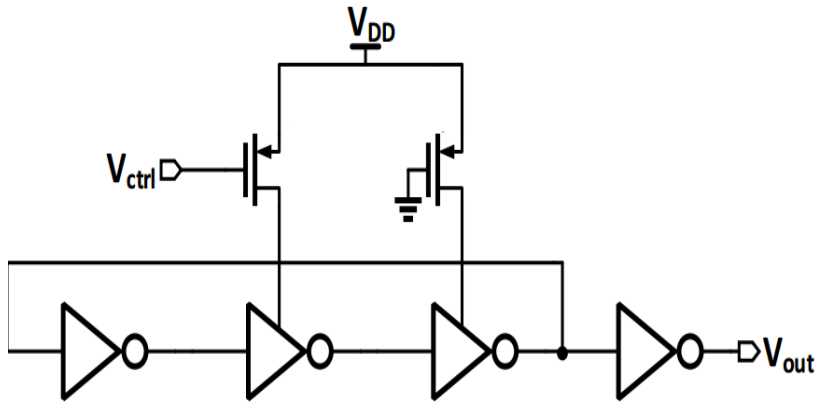
- Large area (inductor)
- Limited tuning range

Key Insight:

- Phase noise is inversely proportional to **tank Q**

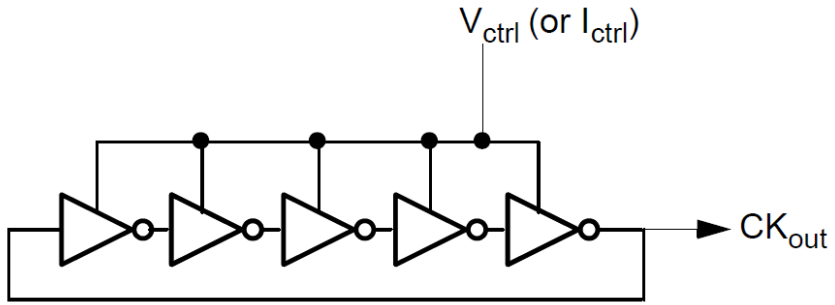
Voltage Controlled Oscillator

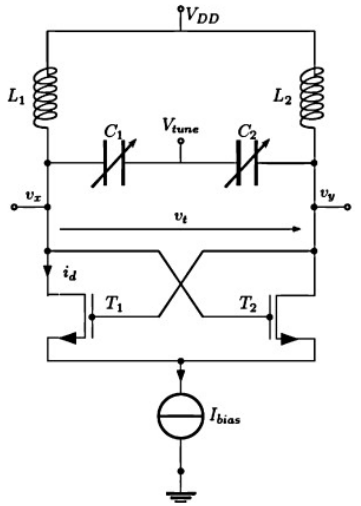
- Generates an output with oscillation frequency proportional to the control voltage
- Helps the CDR accumulate phase and achieve lock



VCO

Common VCO Implementation:

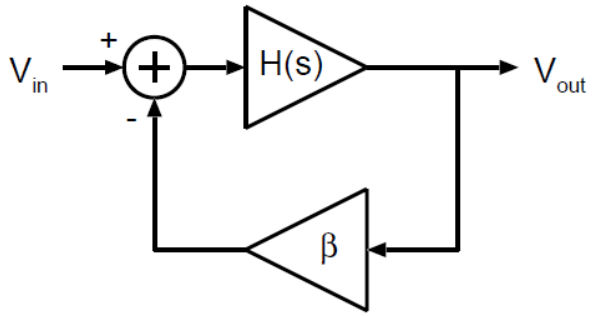




LC-Tank Oscillator

- Extracts average of PD error signals generate VCO control voltage.
- PLL acts like a High-pass filter with respect to VCO jitter.
- VCO always has one pole!

Oscillators Overview



- Closed-Loop Transfer function:

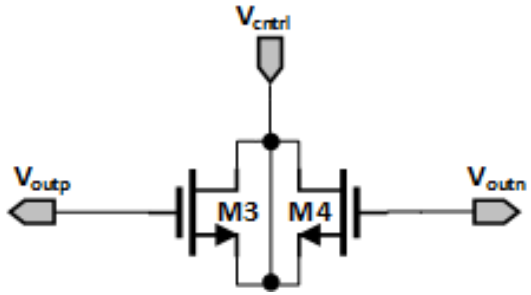
$$-\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+\beta H(s)}, where\ s = j\omega$$

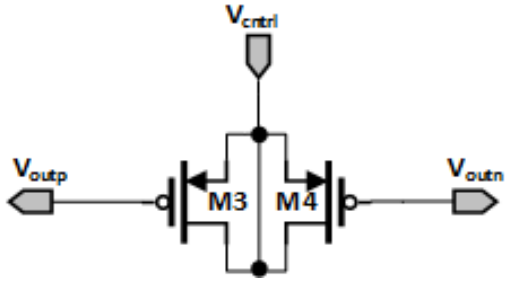
- Barkhausen's criteria for oscillation:
  - $|\beta H(j\omega_0)| = 1$
  - $\arg(\beta H(j\omega_0)) = -180^0$.
- ω_0 = oscillation-frequency.

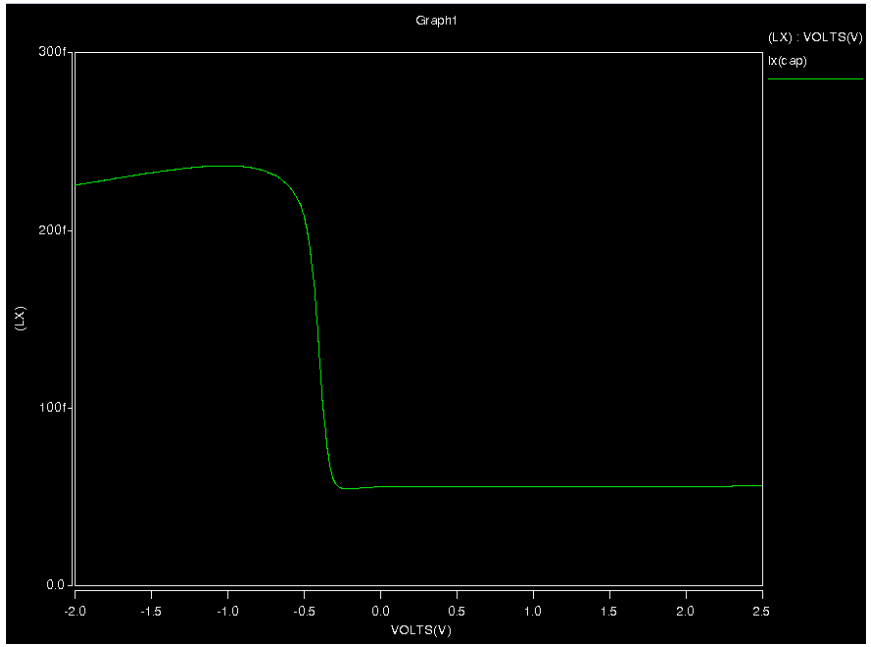
Ring v/s Tank Architecture

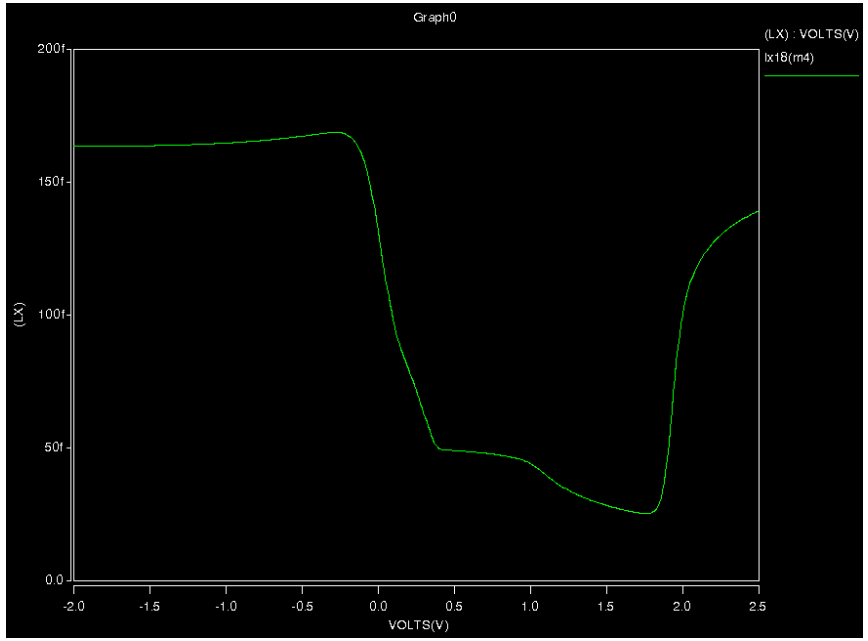
Ring Structure	LC-Tank Structure
1. Low-power, highly integrated.	1. High-power, not integrable.
2. Occupies smaller die-area.	2. Occupies large die-area.
3. Poor-performance at high-frequency due to large phase-noise + jitter.	3. Great phase-noise and jitter performance at high frequency.
4. Can only accept digital signals.	4. Can accept analog and digital signals.

MOS Varactor

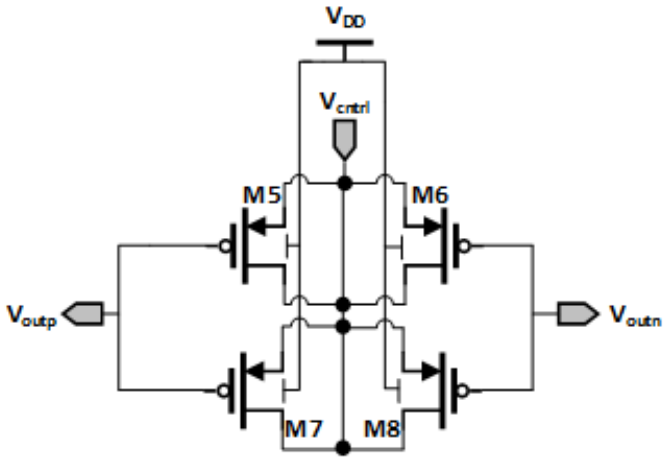


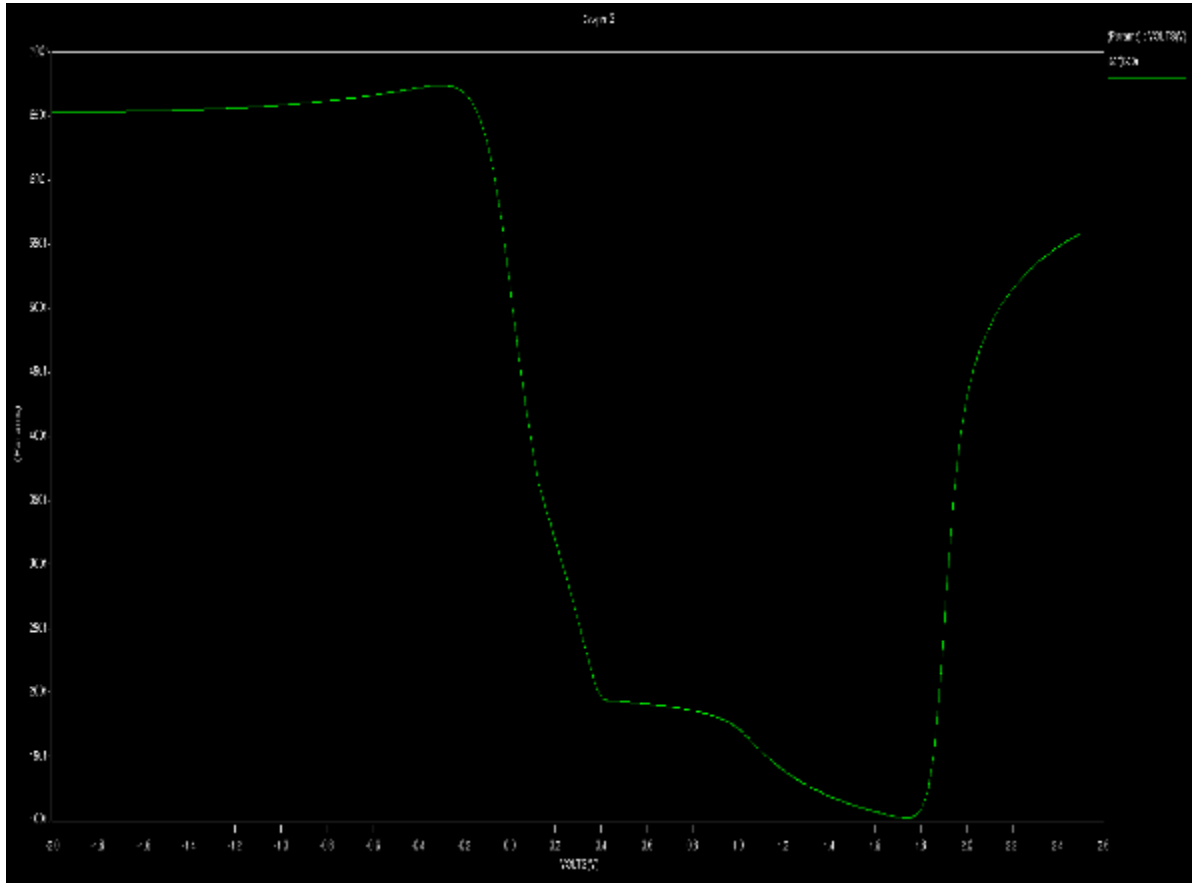




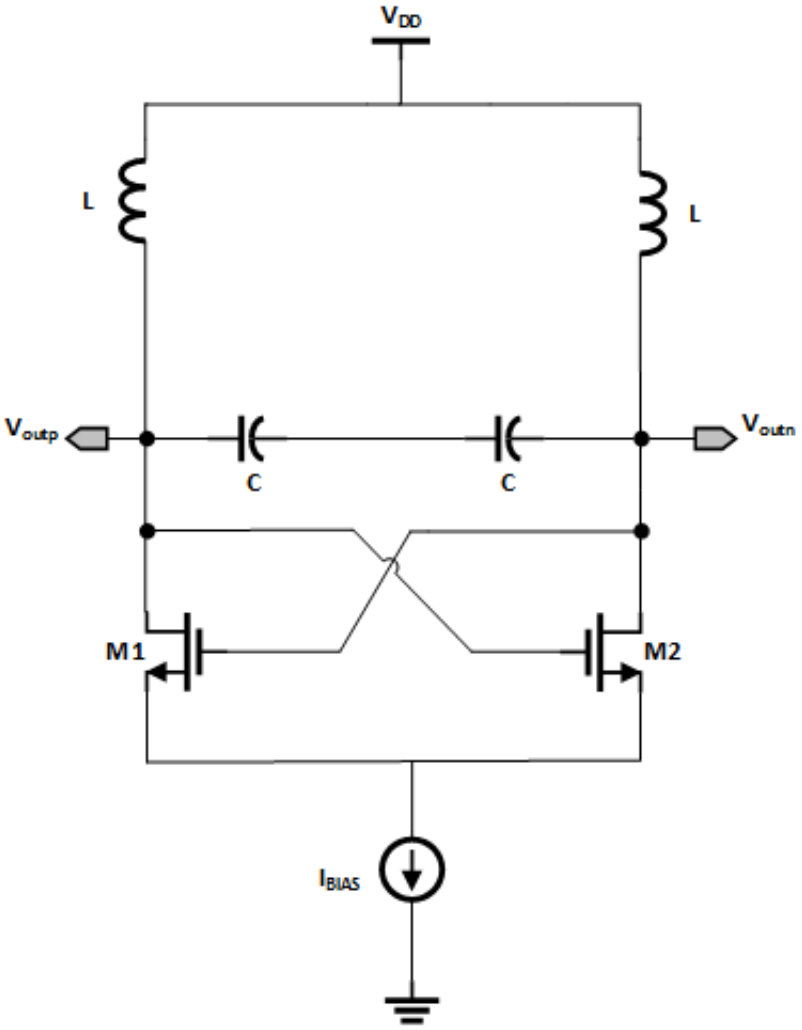


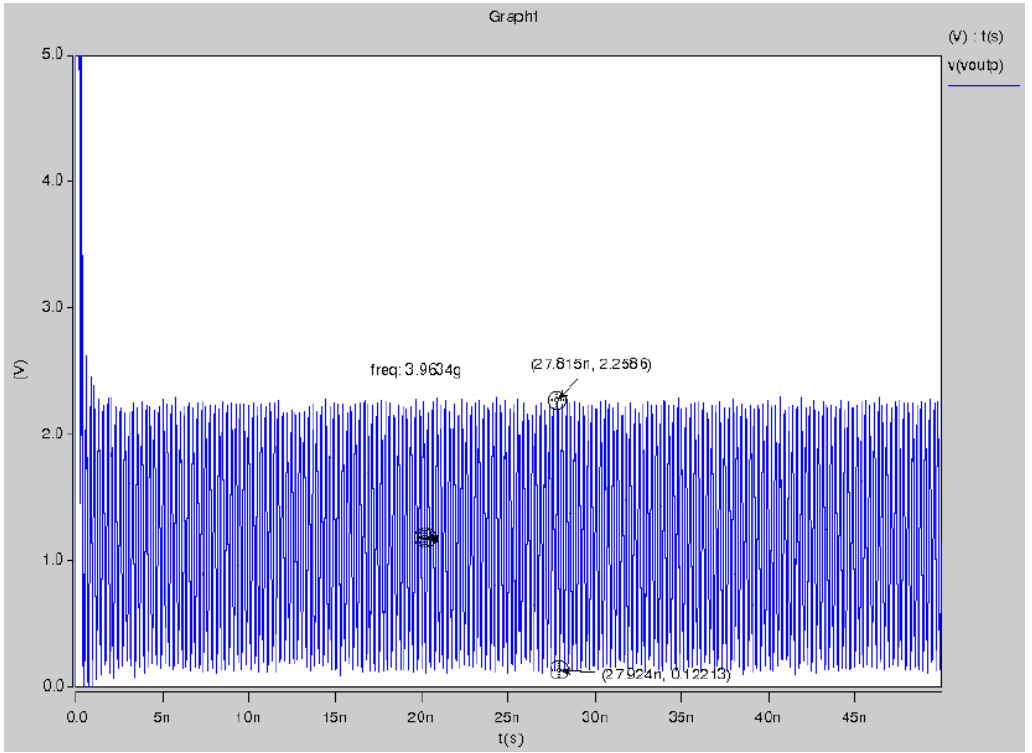
Cascode MOS Varactor



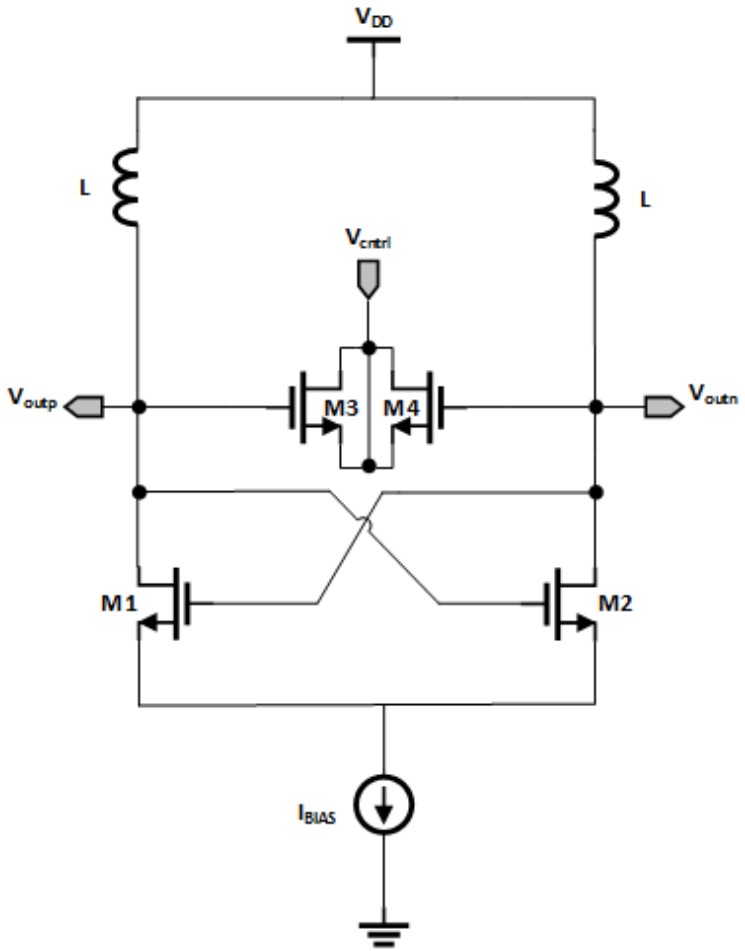


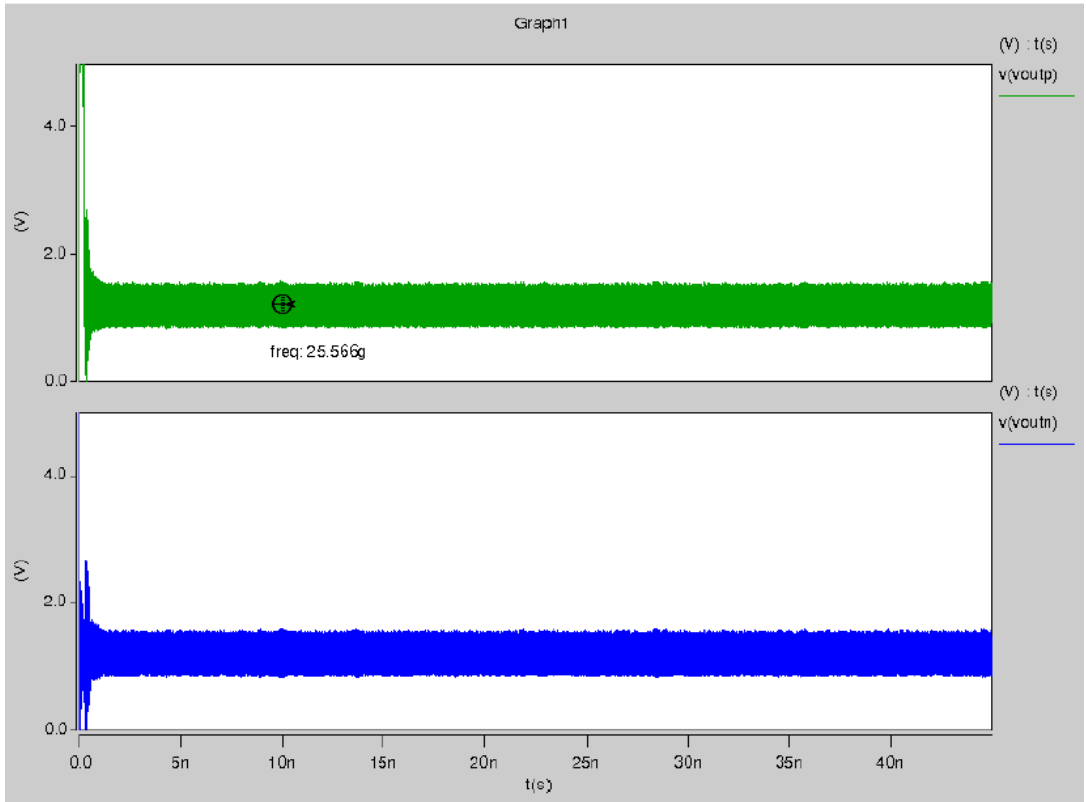
LC-Tank VCO Designs - I



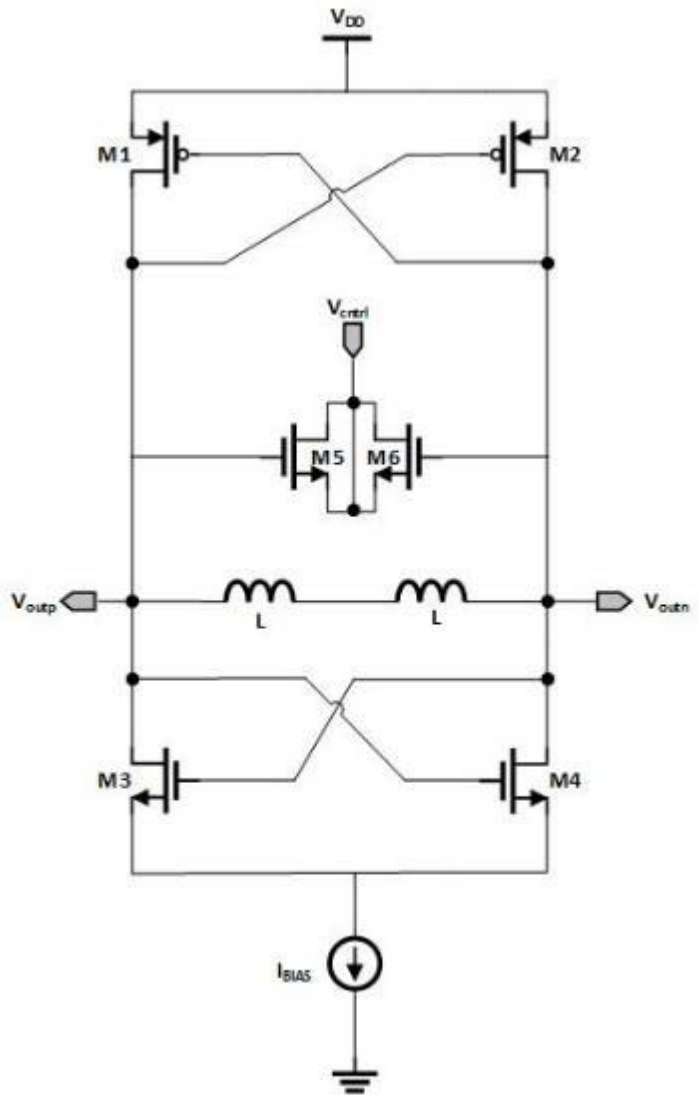


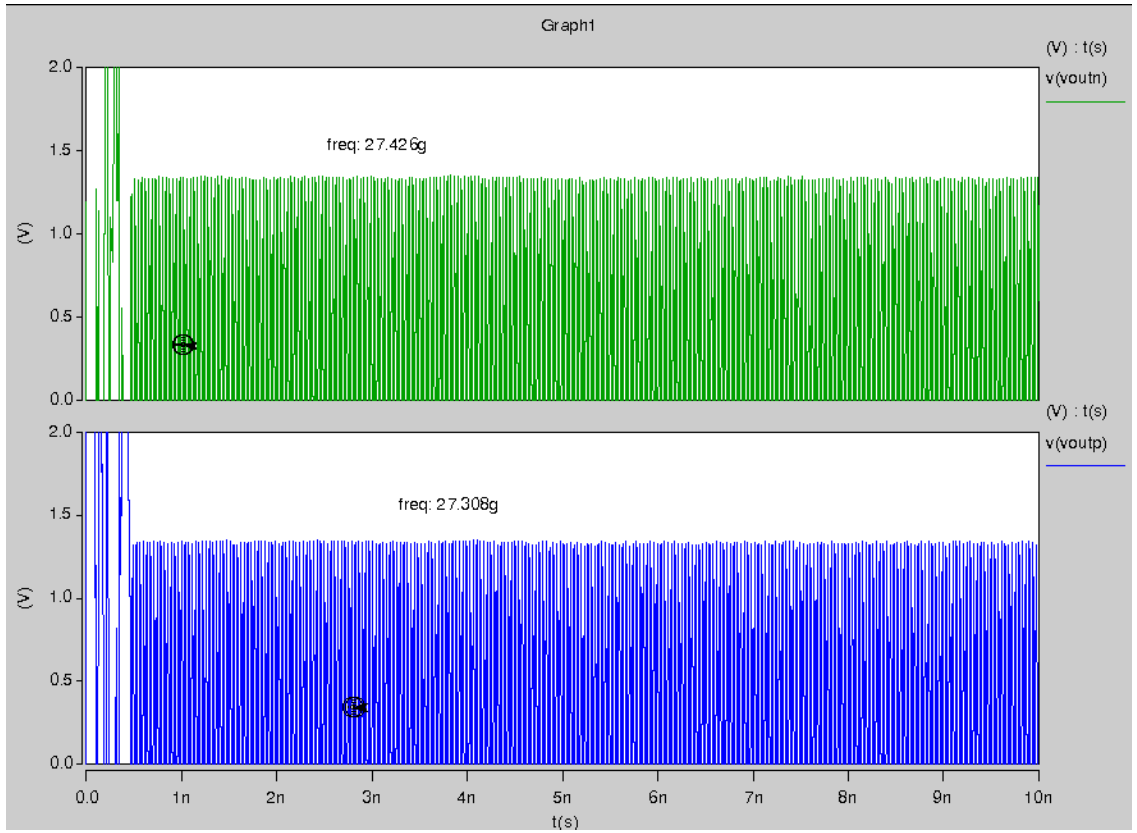
LC-Tank VCO Designs - II



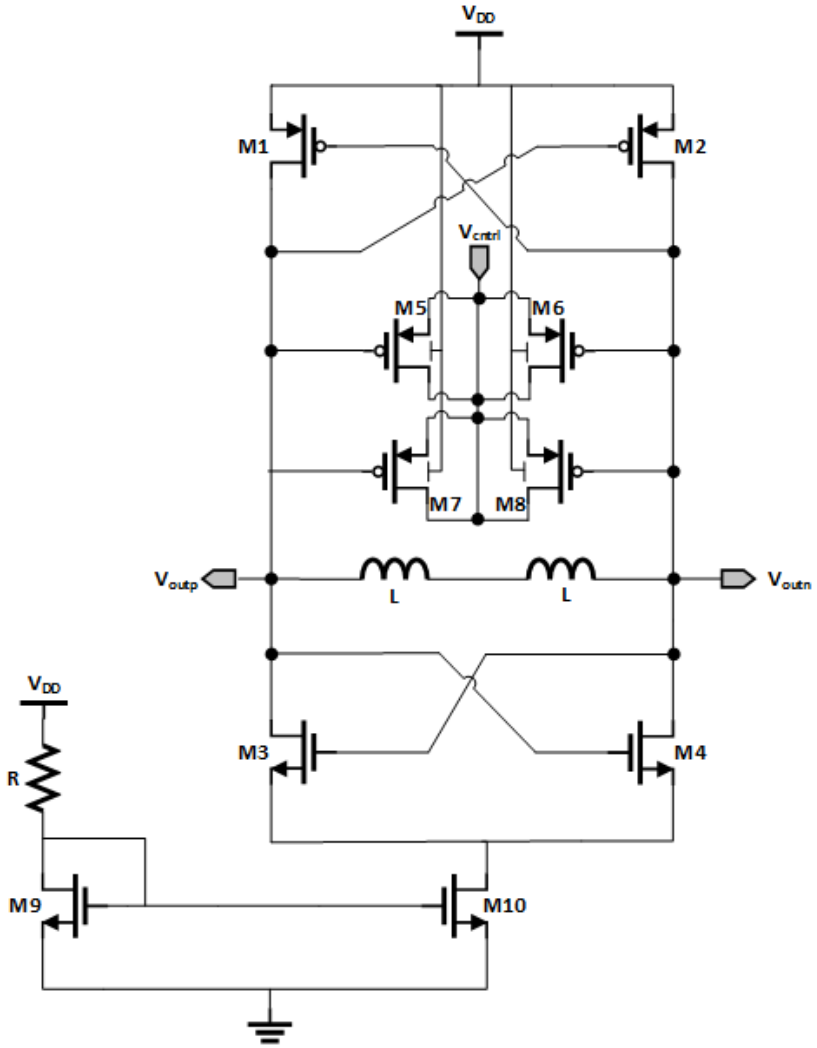


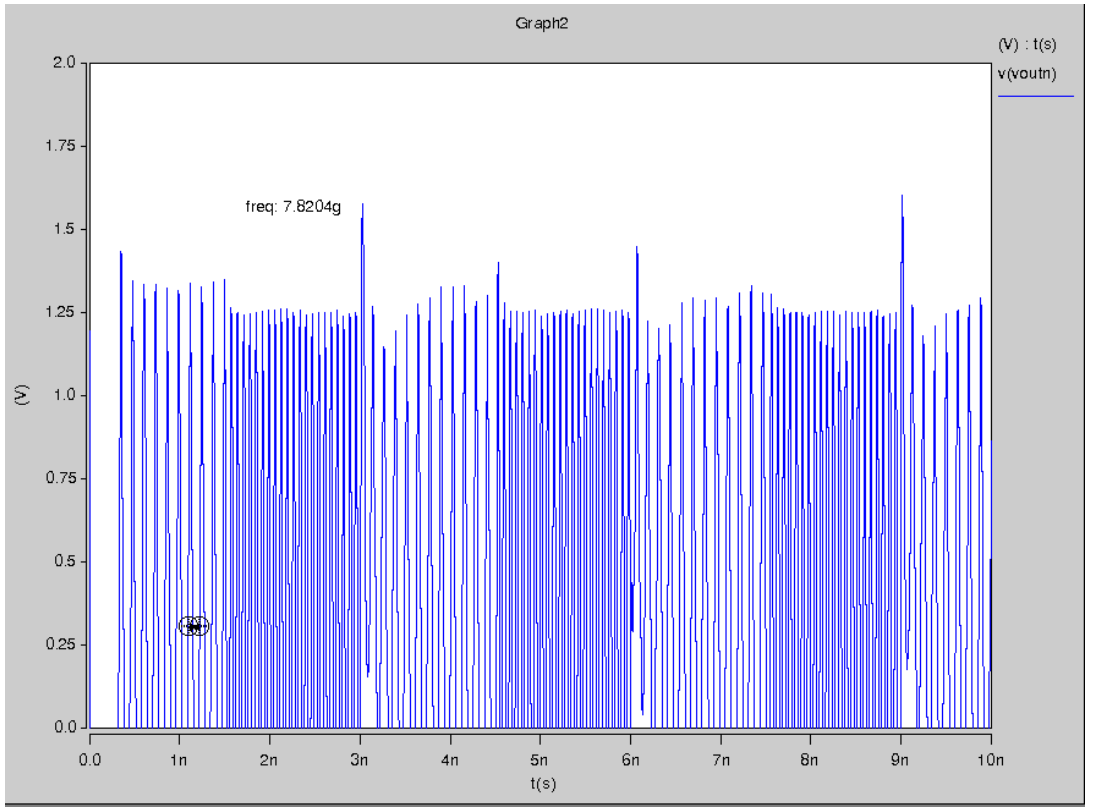
LC-Tank VCO Designs - III





LC-Tank VCO Designs - Final

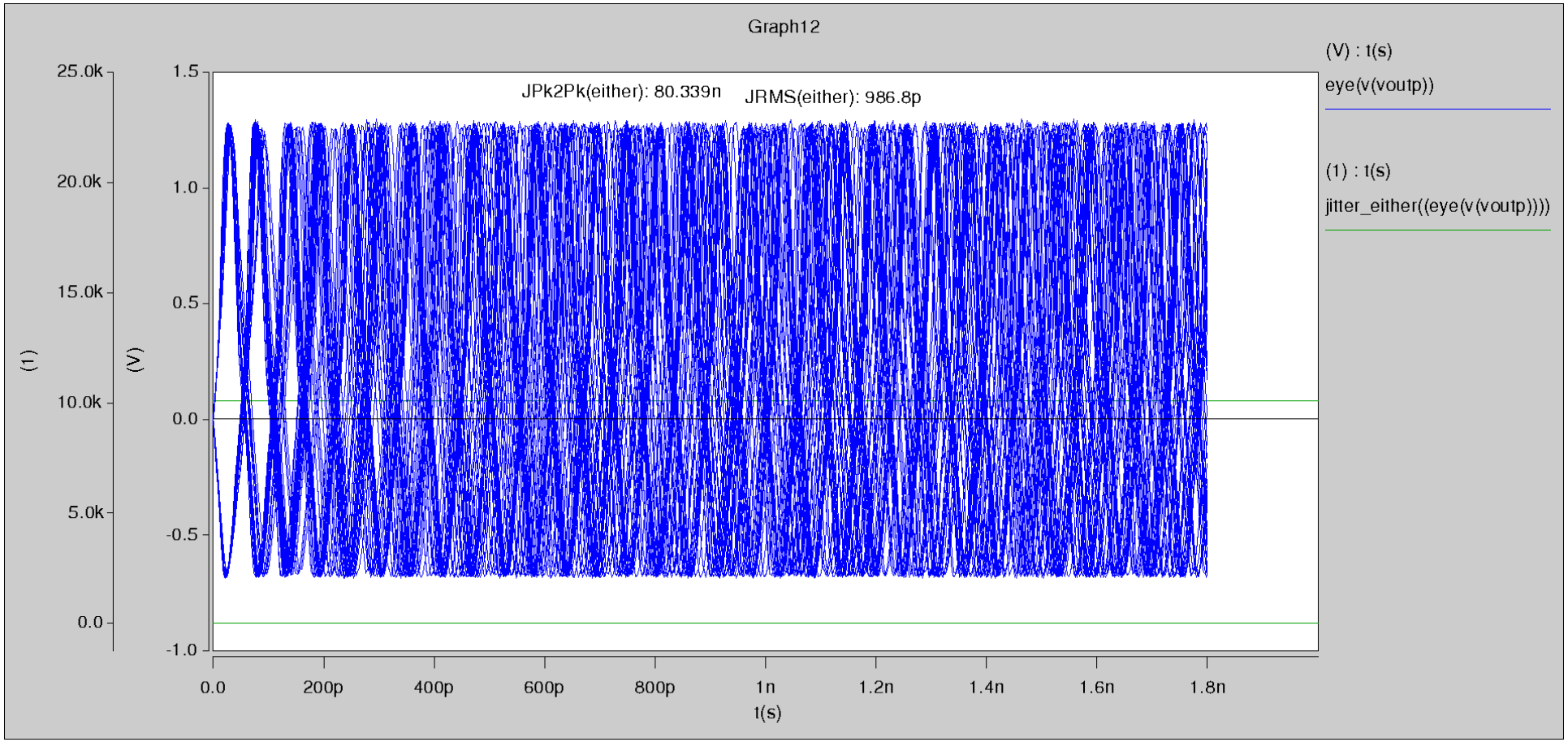




Final VCO Design Parameters

M1	L = 100n, W = 2u
M2	L = 100n, W = 2u
M3	L = 100n , W = 2u
M4	L = 100n, W = 2u
M5	L = 500n, W = 10u
M6	L = 500n, W = 10u
M7	L = 500n, W = 10u
M8	L = 500n, W = 10u
M9	L = 100n, W = 2u
M10	L = 50n, W = 2u
L	1.5nH, Q = 5
R	465 Ω

VCO Jitter Analysis



Divider

Static, dynamic, injection-locked

Used in PLL feedback.

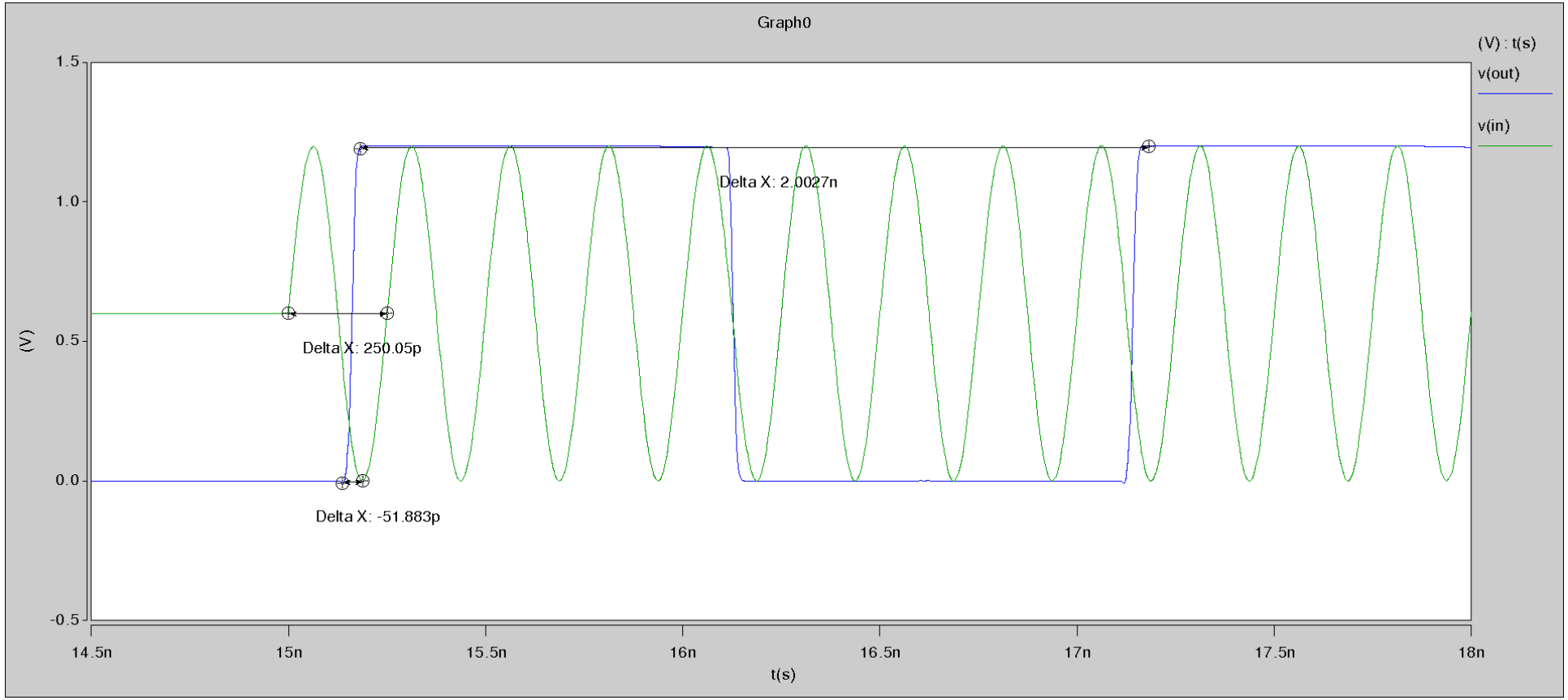
Types:

- Static CMOS divider
- Dynamic divider (TSPC)
- Injection-locked divider

Challenges:

- High-speed operation
- Power consumption
- Metastability

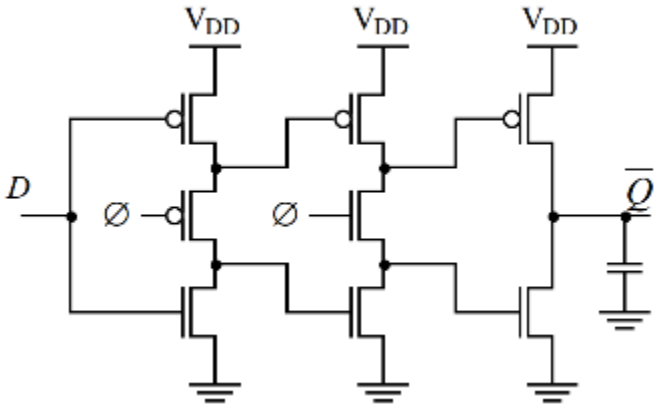
Fractional N-Divider Simulation



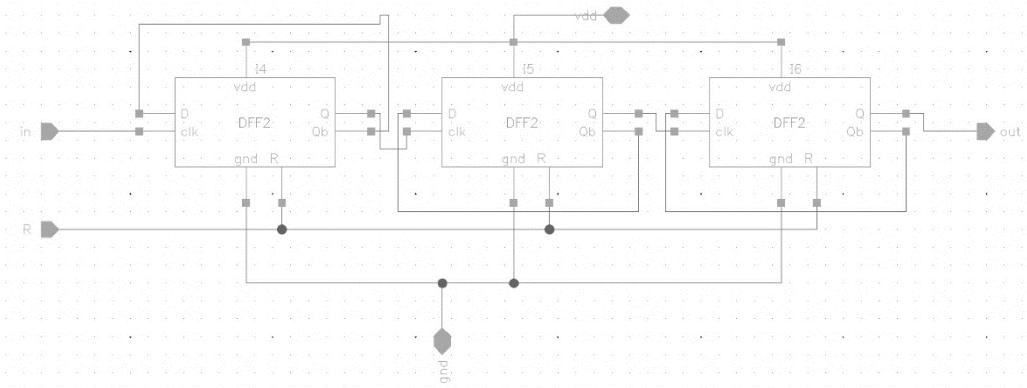
Fractional N-Divider Circuit

1. Needed to slow down the VCO's output so that PFD can compare it with reference frequency.

2. N D-FlipFlops cascaded together to achieve 2^N divider.



Positive edge-triggered DFF using split-output latches

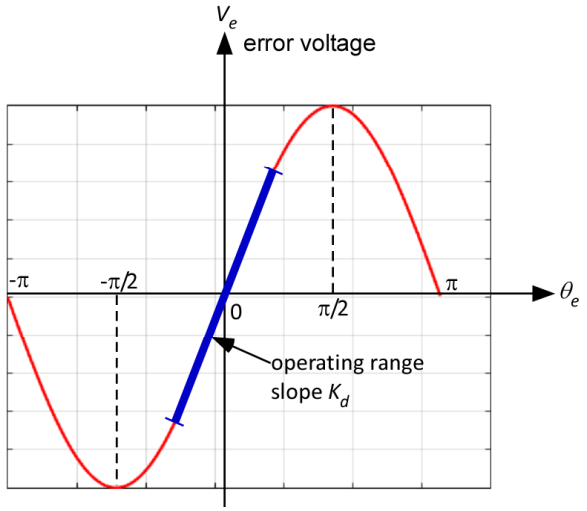


Fractional 8 Divider

Hold in Range

Range over which we can change f_s and still have the loop remain in lock.

For sinusoidal phase detector



$$V_e = K_d \sin\theta_e$$

$$\sin\theta_e = \frac{V_e}{K_d} = \frac{V_e K_a K_o}{K_v} = \frac{\Delta\omega}{K_v}$$

Since sin θ_e cannot exceed ± 1 as θ_e approaches $\pm\pi/2$

The hold-in range is equal to the DC loop gain

Sinusoidal detector:

Max V_e is A and $A=V_d$

$$\pm\Delta\omega_H = \pm K_v$$

Lock in Range

Range of frequencies over which the loop will come into lock without slipping cycles.

- **If the frequency difference $|\omega_s - \omega_f|$ is less than the 3-dB bandwidth of the closed-loop transfer function $H(s)$, the loop will lock up without slipping cycles.**

$$\Delta\omega_L \approx \pm 2\varsigma\omega_n$$ ⟵ **Maximum lock-in range**

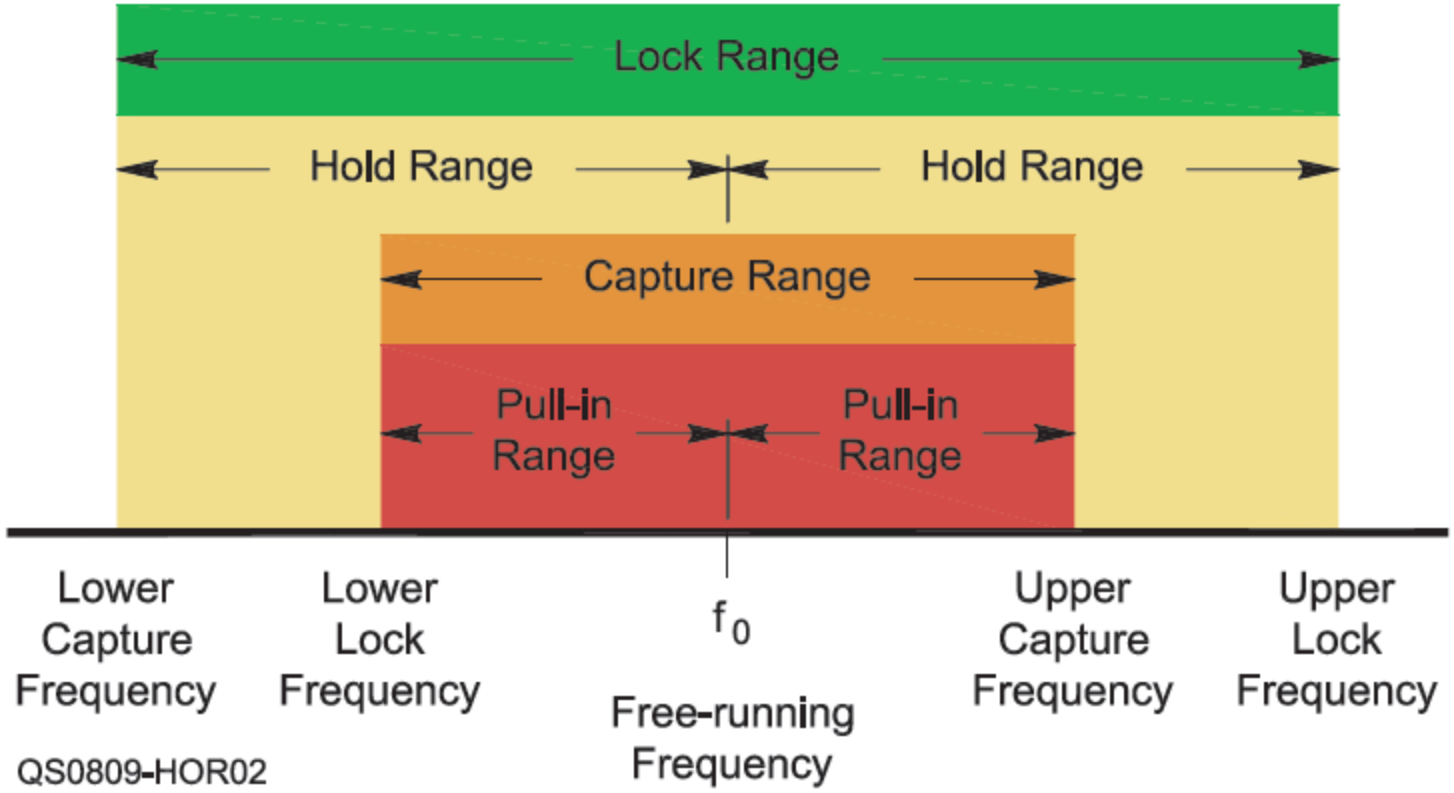
Pull in Range

Range of frequencies over which the loop will eventually lock

- Once loop is in lock, small loop bandwidth is desirable to minimize noise transmission
- If initial frequency difference is outside lock-in range but inside pull-in range, difference-frequency waveshape is nonlinear and contains DC component that gradually shifts VCO frequency until lock up occurs

$$\Delta\omega_p \approx \pm\sqrt{2}\left(2\zeta\omega_n K_v - \omega_n^2\right)^{1/2}$$

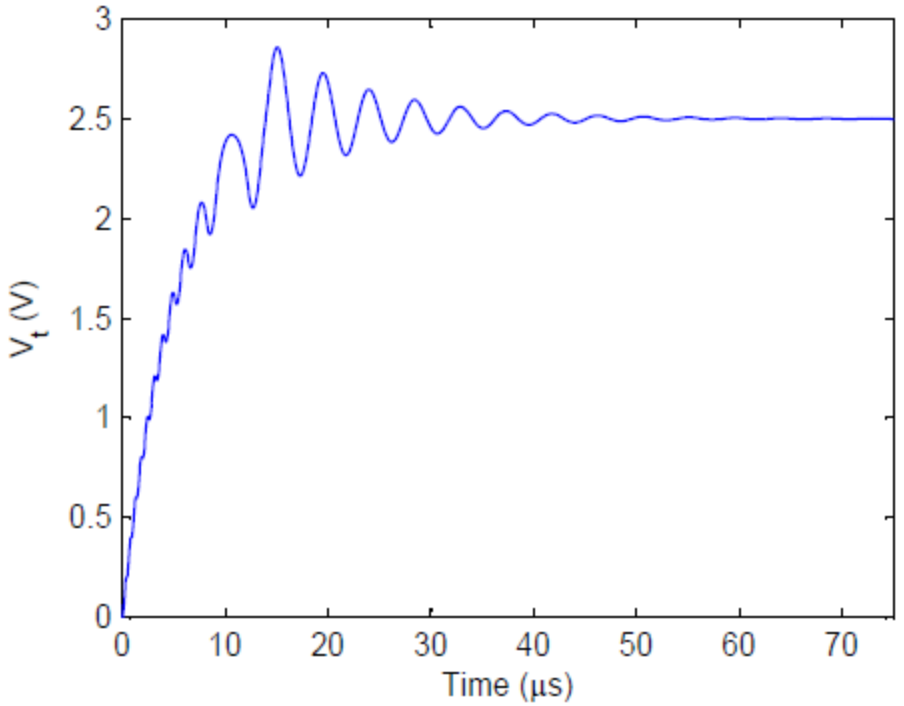
Frequency Ranges of PLL



Source: N0ax Hands-On Radio

PLL Operation – Acquisition

Tuning Voltage
During acquisition

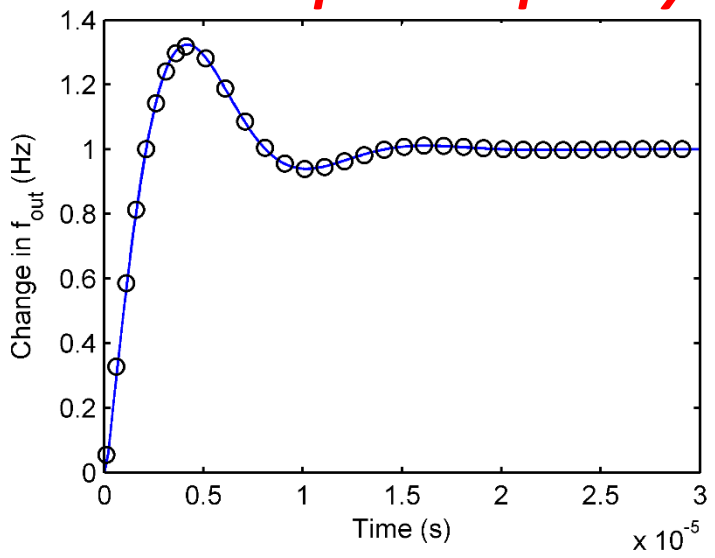


PLL Operation – Lock-In

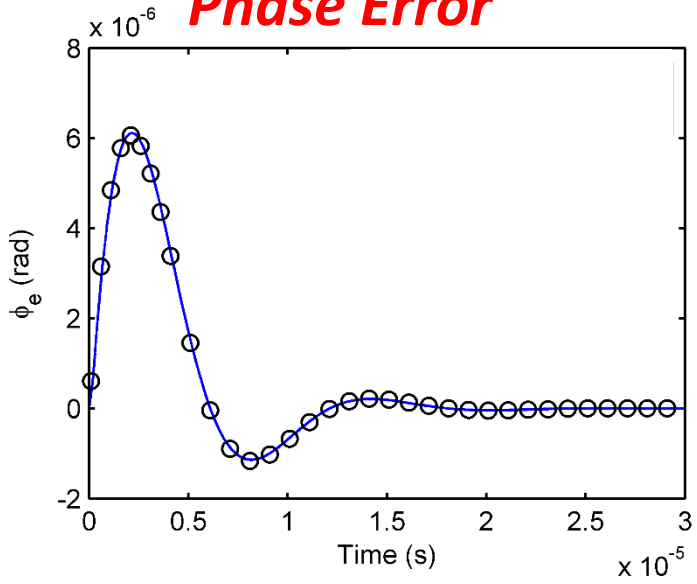
- PLL characteristics
  - $K_D = 5/(2\pi)$ V/rad, $K_V = 2\pi\,(3\times10^5)$ rad/V, $\tau_1 = 4.385\times10^{-6}$ s, $\tau_2 = 1.592\times10^{-6}$ s
- Small unit step change in $f_{in.}$
- PLL operates in the linear region:

$$\sin\phi_e(t) \approx \phi_e(t)$$

Output Frequency



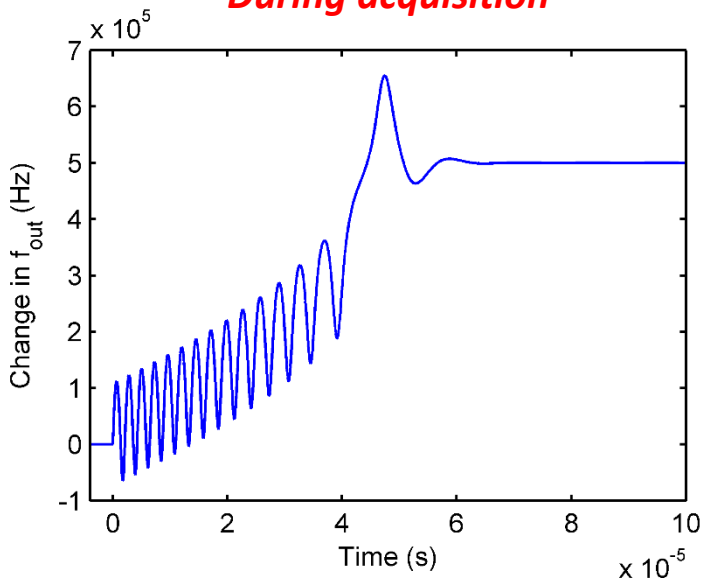
Phase Error



PLL Operation – Acquisition

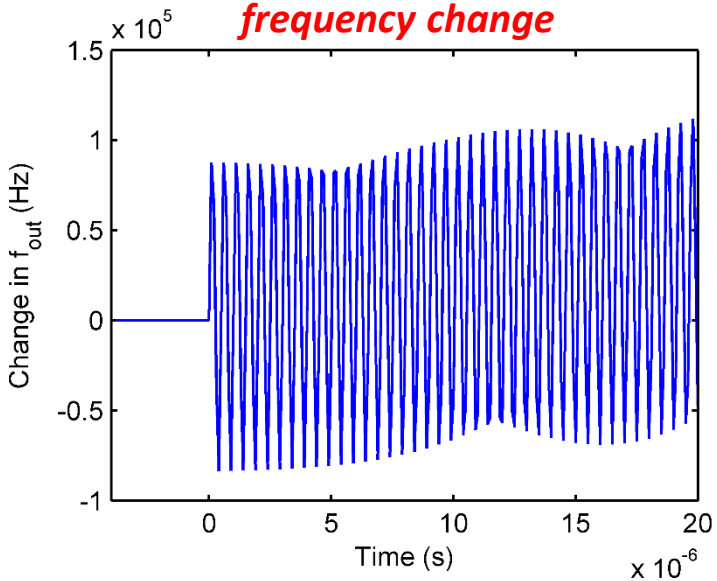
- Large change in $f_{in.}$
- PLL exhibits non-linear behavior:

Output Frequency During acquisition



5 kHz change in f_{in}. Pull-in/acquisition process.

Output Frequency For large step in frequency change

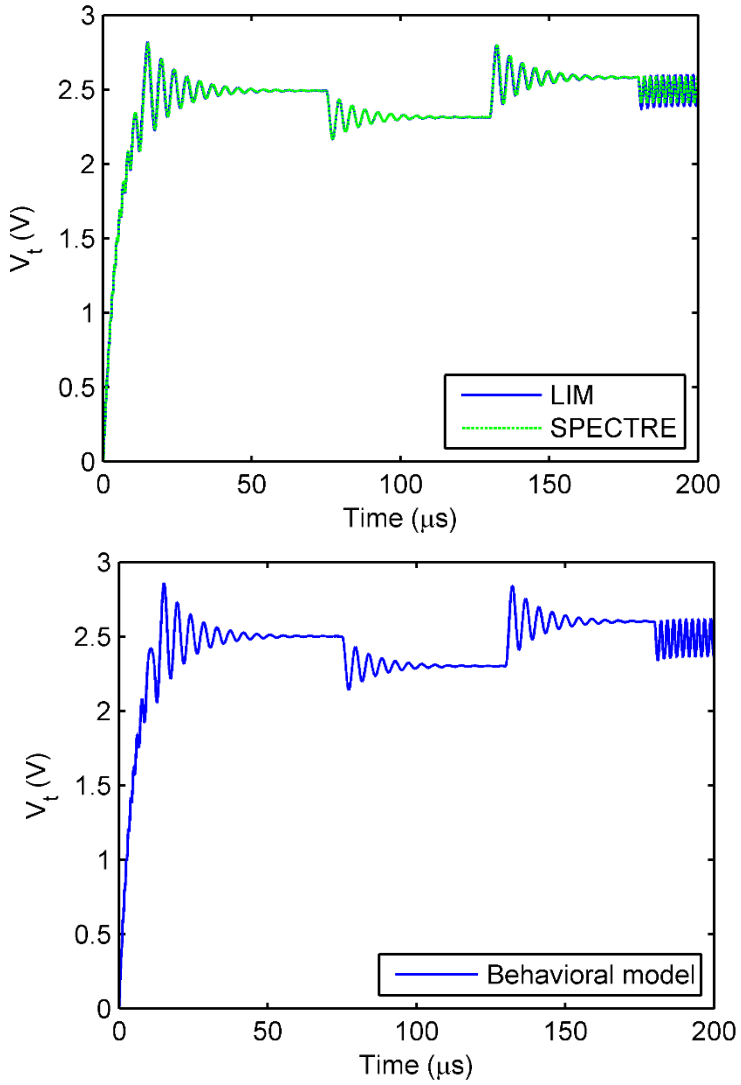


2 MHz change in f_{in}. Pull-out process. PLL no longer locks.

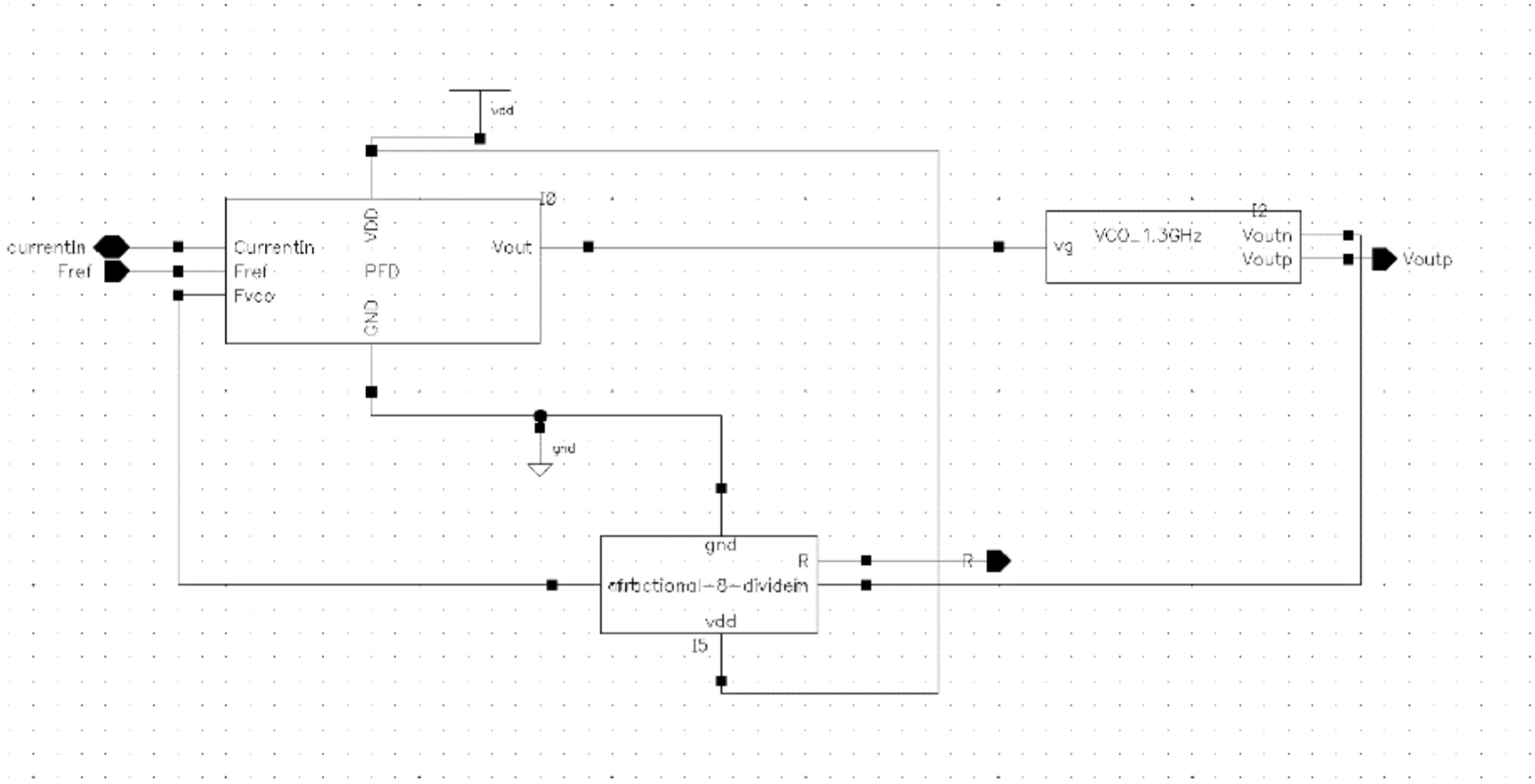
PLL Operation – Long Simulation

- Another example:
  - Long simulation (200 µs)

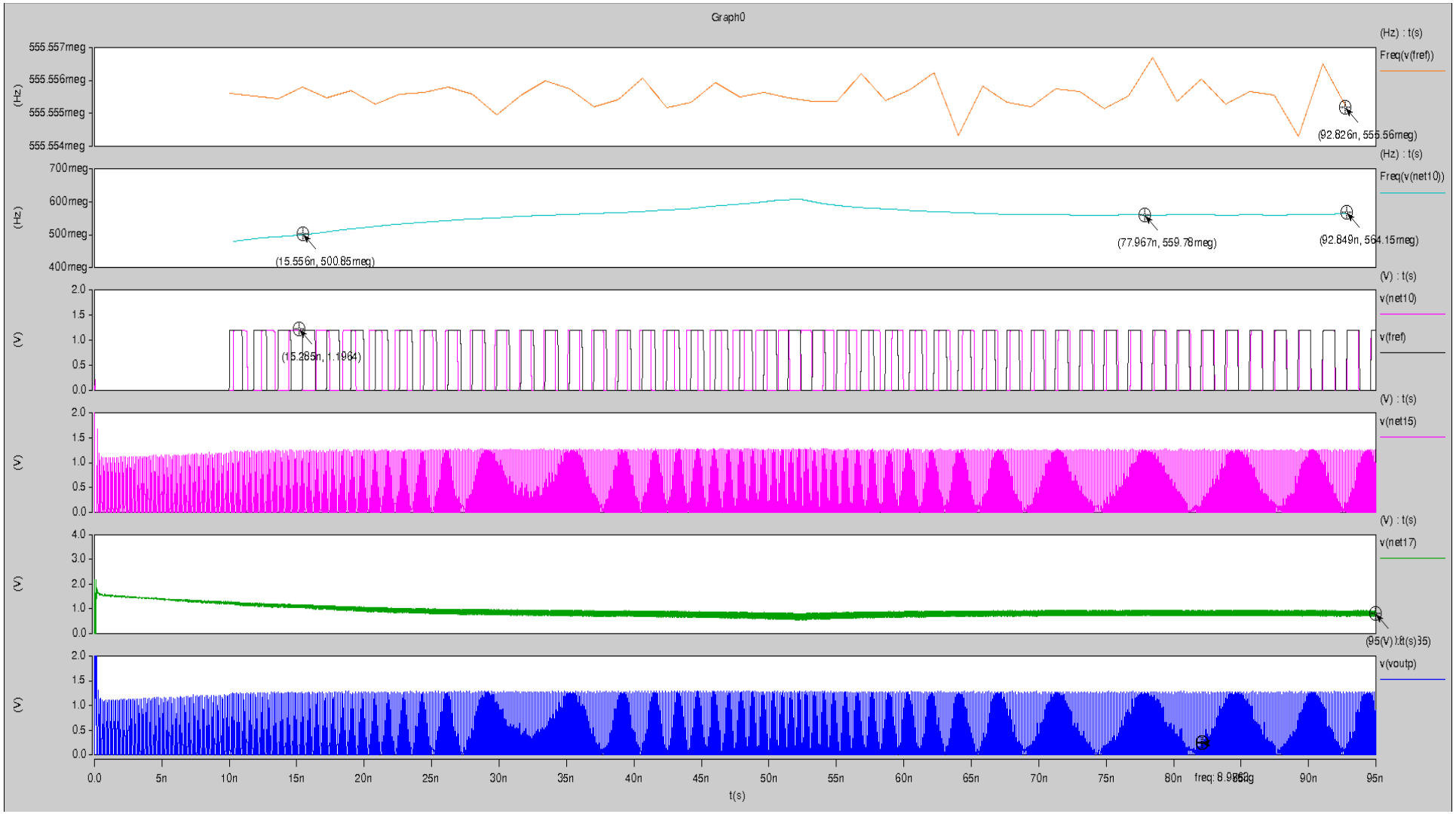
- Input:
  - 0 – 75 µs : 38.5 MHz
  - 75 µs – 130 µs : 38.3 MHz
  - 130 µs – 180 µs : 38.6 MHz
  - 180 µs – 200 µs : 38 MHz



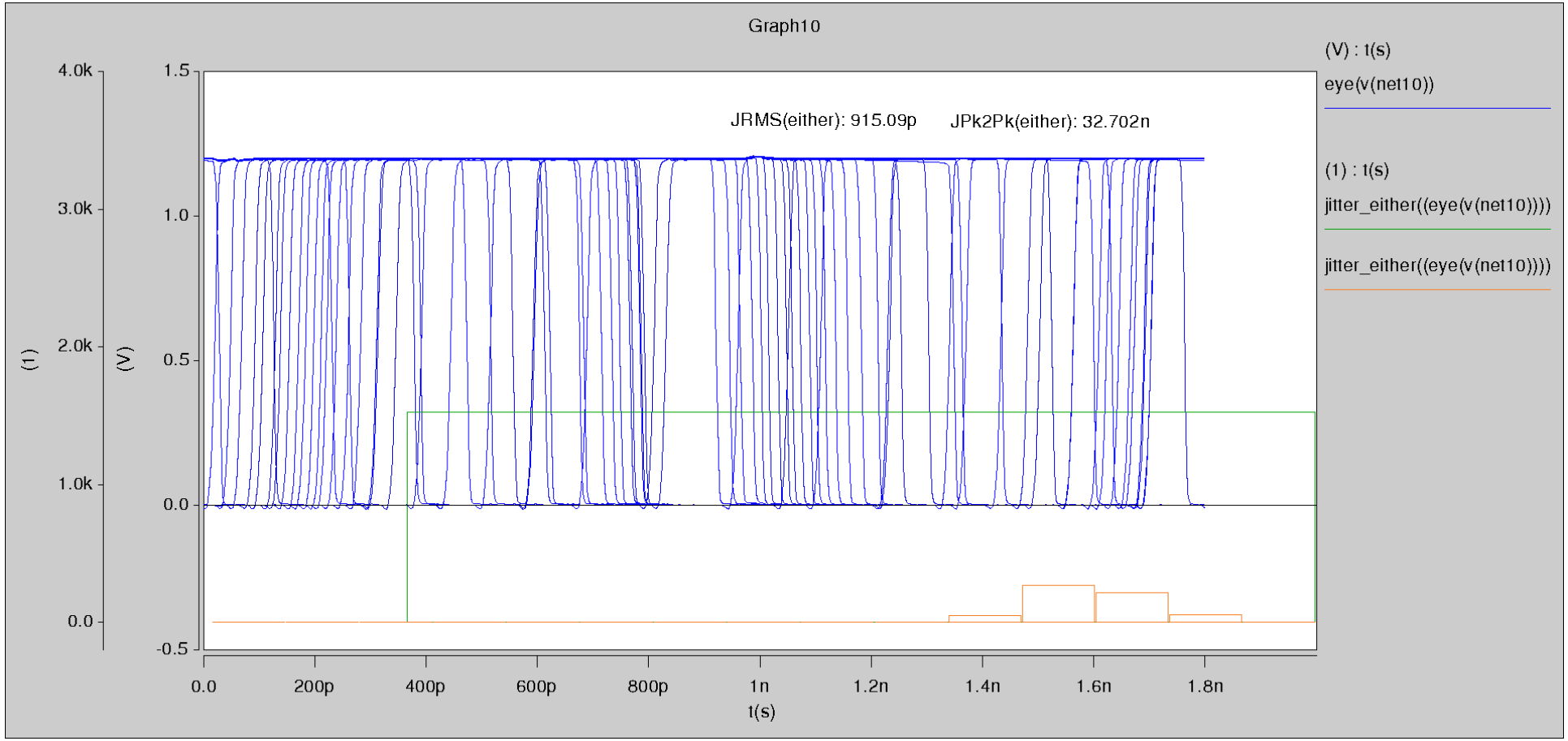
Complete PLL Circuit



Complete PLL Simulation



Complete PLL Jitter Analysis



PLL vs CDR

- **PLL: frequency synthesis**
- **CDR: timing recovery**

PLL:

- Generates a clean, frequency-multiplied clock
- Filters noise from reference
- Synchronizes internal clocks

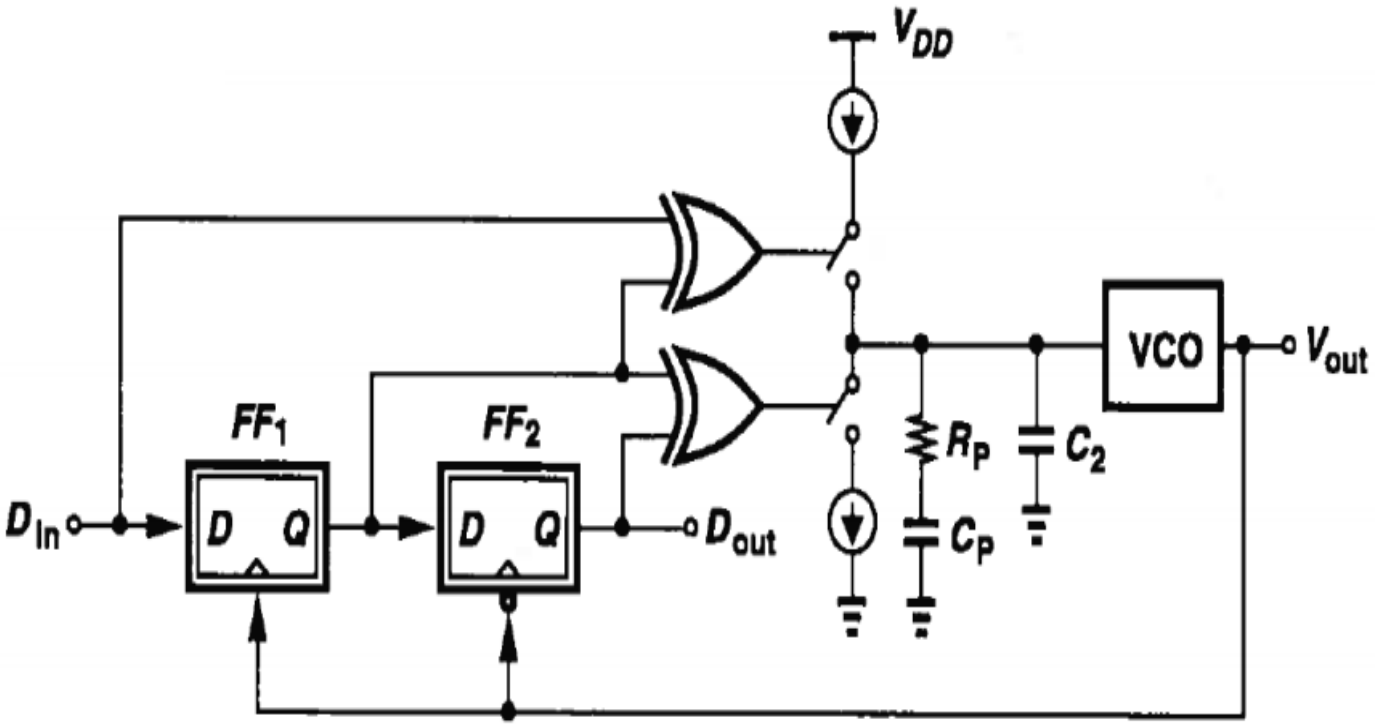
CDR:

- Extracts timing from incoming data stream
- Must track phase variations dynamically

Key Difference:

- PLL → **frequency synthesis**
- CDR → **timing extraction + tracking**

The CDR Circuit



CDR Circuit Overview

- Monitor data signal transitions and select optimal sampling phase for the data at midpoint between edges.
- Extracts clock information from incoming data stream and uses this regenerated clock to resample the data waveform and recover the data.
- Non-linear circuit and key block to limit jitter, noise within the SERDES circuit.