ECE 546 HOMEWORK No 10 Due Wednesday, April 24, 2024

In this homework you will exercise the DC analysis features of Virtuoso and use them to properly size the inverter transistors in order to achieve a 50-ohm match.

1. DC analysis tutorial

To enable DC analysis, simply choose 'dc' from the analysis setup in the ADE environment (see Figure 1).

Analysis	 dc sens sp pstb qpss qpsp 	 ac dcmatch envlp pnoise qpac hb 	 noise stb pss pxf qpnoise
 xf pz pac psp qpxf hbnoi Save DC Operating P Hysteresis Sweep Sweep Variable Temperature Design Variable Component Parar 	 sens sp pstb qpss qpsp 	 dcmatch envlp pnoise qpac hb 	 stb pss pxf qpnoise
 pz pac psp qpxf hbnoi Save DC Operating P Hysteresis Sweep Sweep Variable Temperature Design Variable Component Parar 	 sp pstb qpss qpsp 	 envlp pnoise qpac hb 	 pss pxf qpnoise
 pac psp qpxf hbnoi Save DC Operating P Hysteresis Sweep Sweep Variable Temperature Design Variable Component Parar 	 pstb qpss qpsp 	 pnoise qpac hb 	○ pxf○ qpnoise
 psp qpxf hbnoi Save DC Operating P Hysteresis Sweep Sweep Variable Temperature Design Variable Component Parar 	 qpss qpsp 	O qpac O hb	o qpnoise
 qpxf hbnoi Save DC Operating P Hysteresis Sweep Sweep Variable Temperature Design Variable Component Parar 	🔾 qpsp	🔾 hb	
 hbnoi Save DC Operating P Hysteresis Sweep Sweep Variable Temperature Design Variable Component Parar 			🔾 hbac
Save DC Operating P Hysteresis Sweep Sweep Variable Temperature Design Variable Component Parar	se 🔾 hbsp		
Sweep Variable Temperature Design Variable Component Parar	oint 🗹		
🔲 Component Paran			
🔲 Model Parameter	otor		
Enabled 🕑	letei		

Figure 1. ADE L Analysis dialog box

In order to measure the on-resistance of the transistor, the voltage drop across the transistor, V and the current through it, I will also need to be measured. The resistance is simply the ratio V/I. This can be evaluated using the built-in calculator. You can enter the calculator mode by clicking the '**open**' button from the "**output setup**" dialog box within the ADE environment.

Design Varlables Name Value	Analysis 7.8 x	
	Outputs Or #puts Or #puts	
Sature Culmute	Status Baady Tu27 C Similator sharts	
AV count contain	Setting Outputs ADE L (1)	
	i Output Table Of Outputs	e Ontre
Selected		

Figure 2. ADE L – Outputs settings dialog box

Next, click 'vdc' from the upper row of the new window, the schematic will automatically come to the foreground. Click the node for which you want to measure the dc voltage. An expression VDC("/NOTE_NAME") will appear in the text box. This will measure the DC voltage of the node. Similarly, clicking on 'idc' will measure the DC current, 'vf' and 'if' will measure the frequency-domain voltage and current respectively, 'vt' and 'it' will measure the time domain voltage and current respectively. You can also select functions from the 'Function Panel' button to perform advanced mathematical manipulations of the signal.

Wirtuoso (R) Visualization & Analysis XL calculator	_ 0 X
Eile Iools View Options Constants Help	cādence
In Context Results DB: none specified	
vt vt vt vt vt vt vt vt vs vs vs var vn sp vswr v it vf Select schematic signal. Create DC voltage expression yp	hp 🔾 zm gd 🔾 data
📗 Off 🔾 Family 🔾 Wave 🗹 Clip 🦏 🚛 Append 🔽 Rectangular 🕇) 🎯 🛛 »
Key B X 7 8 9 / 4 5 6 *	
1237 - 7 B. & B. B. B. B. B. M. B. B. A. B. A. B. A. B. A. B.	5 ¢
Stack	8×
Function Panel	ē x
Special Functions	
PN handwidth compression/PL dPm dthh aumOnak faurEuch gainBu	Brod barmon
a2d clip convolve delay dnl eyeDiagram freq gainMa	rgin harmon
average compression d2a dft evmQAM flip frequency groupD	elay iinteg
	×.
5	

Figure 3. ADE L – Visualization and analysis calculator.

The expression for calculating the on-resistance of the transistor will be 'abs((VDC(source) – VDC(drain))/IDC(drain))'. Once you finished editing the expression, go back to the output setup window and click 'get expression', the expression will be automatically copied. A proper name should be given to the expression and then click 'add'.

Selected Output Name (opt) Ron Expression >dd*) > VDC (*/out*)) / IDC (Calculator Open Get Expression Clo Will be ✓ Pioted/Evaluated Clo Clo	Table Of Outputs Table Of Outputs Table Of Outputs Table Of Outputs Term Schematic se	× Virtuoso (R) Visualization & Analysis XL calculator _ _ × F Options Elle Tools ½ev Options Constants Help Cādence Image: Second and the second a
Add Delete Change Next Ne ADE L (Launch Sgssion Setup Analyses Variables	W Expression OK Cancel Apply L) - ece546 inv schematic – Quiputs Simulation Besuits Tools Help cād	Image: Control of Con
Design Variables	Analyses 7 6 Type Enable Arguments g dc v t Outputs 6 6 Name/Signal/Expr Value Hot Save Save Option	All Tix bif delay freq_iller grcupCelay ipn normalOG pp PN clip deriv frequercy gt ipn/RI overshoot pr PN clip deriv frequercy gt ipn/RI overshoot pr PN clip deriv frequercy gt ipn/RI overshoot pr acd compression with gac_gain harmonicFreq acd compression/RI del gac_gain harmonic kf peak pr abs_tifter conjugate dutyCycle gainBurFrod histogram2D loadpul period_iller pr action const evenOprk getAsciWave in test phaseDeg interpaseDeg interpase action cost evenOprk getAsciWave in test phaseDeg interpaseRad re pr atam 4Ca faiTime gram gram inter c.freq phaseRed re phaseRadUrwrapped ris average dE20 fourEval gpc_freq integ rd phaseRed re phaseRadUrwrapped ris Control test and the second
 (4) Choose Analyses 	Plot after simulation: Auto Plotting mode; Replace	status area S

Figure 4. ADE L – Implementing mathematical expressions

2. Transistor model

The transistor in the inverter-based transmitter can be modeled as an ideal switch and a series resistor as shown in Figure 5.

Draw a similar model for the differential transmitter, channel and termination from homework

9. Comment on the target on-resistance of each transistor.



Figure 5. CMOS inverter and switch equivalent-circuit.

3. Sizing the transistor

Note that the on-resistance of the transistor not only depends on the voltage drop across it but also on the absolute voltage of both the source and the drain.

Calculate the source and drain voltages needed to measure the on-resistance of each transistor.

4. Simulation

In Cadence virtuoso, implement the DC analysis and extract the width of each transistor to ensure a 50-ohm match. Run the same step function as in homework 8 for at least 60 ns and comment on the results (input waveform of TX, input waveform of channel and output waveform of the channel).