In this homework you will extract the pulse response of the given channel, extract the decision feedback equalization (DFE) coefficients to equalize the channel and examine the equalization result by using a behavioral implementation of DFE in VerilogAMS.

1. **Extract pulse response of the channel**
   You should generate a pulse input with a 400ps pulse width, a 20 ps rise and fall time, and a period of at least 60 ns. The input and output of the channel should be matched to 50 ohms.

2. **Find the post cursers**
   Plot the pulse response of the channel, comment on the result, note the main post curser(s) and determine your DFE coefficients.

3. **VerilogAMS tutorial**
   3.1. Create a new CellView and choose the `VerilogAMSText` as the type. Note that the cell name should be exactly the same as the module name of the Verilog block.

   ![New File](Image)

   3.2. Now you can copy and paste the given dfe sampler Verilog code ([http://emlab.uiuc.edu/ece546/tools/verilog.vams](http://emlab.uiuc.edu/ece546/tools/verilog.vams)) into the text editor. When you close it the code will be automatically compile and virtuoso will ask you whether or not to generate a symbol for it. Please click `yes`. If there is no symbol generated, it is usually due to the code not being compiled. Please make sure the code is the **last** file to be saved and closed. You can close all the text editor sessions and re-open the code, make any change then close it again to force compilation. If there is any error, please go back to CIW window to debug.
3.3. Next, create the test bench for the DFE sampler. An example schematic that shows how to integrate the DFE sampler with the existing system is included below.

3.4. You can right click the DFE block and choose ‘property’ -> ‘CDF Parameter of view’ -> ‘verilogams’ to change the DFE coefficients. The DFE block has the following inputs: \text{in} and \text{inbar} are the differential channel input; \text{rst} is the reset signal to initialize the block; \text{clk} is the clock signal to sample the incoming waveform (\text{eyeopen} \geq 400mV). The outputs are as follows: \text{out} and \text{outbar} are the differential outputs after equalization; \text{Dout} is the digital decision of the input waveform.
3.5. After the testbench schematic, a testbench config view is needed to co-simulate the VerilogAMS blocks with transistor blocks. To create the config view, highlight your testbench, create a new view, choose the ‘config’ as the type. Then on the newly popped window choose ‘Use Template’ -> ‘Name’ -> ‘AMS’, ‘View’->’schematic’.
3.6. In the Hierarchy editor make sure all the cells are resolved and right views are used for the simulation. Then click ‘Open’ to open the config view. You can start ADE as usual.

3.7. In the ADE environment, the simulator should be changed to ‘ams’, the view name of the design to be simulated should be ‘config’. In ‘Simulation’ -> ‘Netlist and Run Options’, choose ‘OSS-ased netlister with irun’ as the run mode. In ‘Setup’ -> ‘Connect Rules’ make sure the built-in ‘ConnRules_18V_full_fast’ is chosen.
Use the DFE coefficients you determined earlier, set the input of the TX to PRBS31 with bit period of 400 ps with 20 ps rise and fall time, plot the eye diagram of the output of the channel and the output of the DFE block. Comment on the results.
**Note1**: a PRBS31 source can be created by using ‘vsourse’ from ‘analogLib’

![Add Instance Dialog](image)

**Note2**: A differential PRBS31 source can be created from ‘vsourse’ and ‘vcvs’ (voltage controlled voltage source) from ‘analogLib’
Note 3: To create the eye diagram, go to ‘Visualization & Analysis’, choose ‘Measurements’ -> ‘Eye diagram’, Choose the signal you want to plot on the left column and specify the start/end time (the sequence should be long enough), period (> 2 bit period) on the right column.

Note 4: Open the VerilogAMS file to understand the algorithm. For VerilogAMS syntax please go to http://www.designers-guide.org/VerilogAMS/