ECE 546 HOMEWORK No 10 Due Friday, May 1, 2026

PART I

In this part of the homework you will exercise the DC analysis features of Virtuoso and use them to properly size the inverter transistors in order to achieve a 50-ohm match.

1. DC analysis tutorial

To enable DC analysis, simply choose '**dc**' from the analysis setup in the ADE environment (see Figure 1).

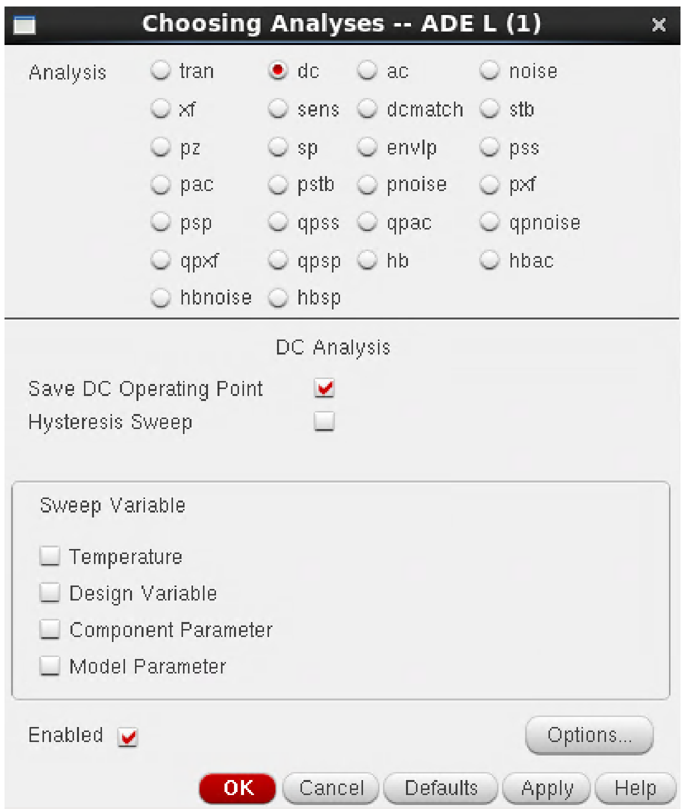


Figure 1. ADE L Analysis dialog box

In order to measure the on-resistance of the transistor, the voltage drop across the transistor, *V* and the current through it, *I* will also need to be measured. The resistance is simply the ratio *V/I*. This can be evaluated using the built-in calculator. You can enter the calculator mode by clicking the '**open**' button from the "**output setup**" dialog box within the ADE environment.

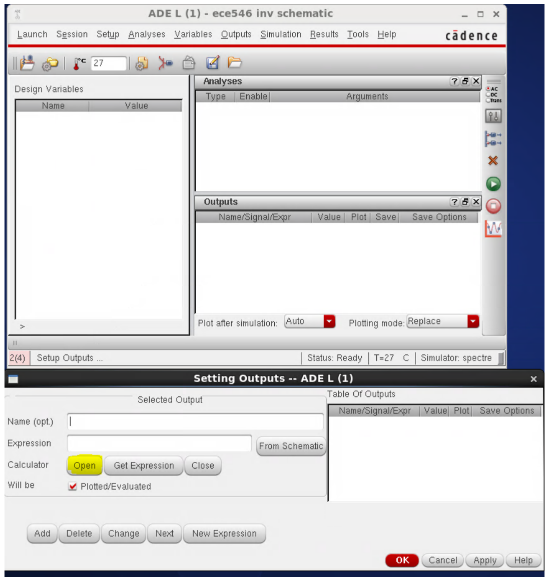


Figure 2. ADE L – Outputs settings dialog box

Next, click ‘**vdc**’ from the upper row of the new window, the schematic will automatically come to the foreground. Click the node for which you want to measure the dc voltage. An expression **VDC(“/NOTE_NAME”)** will appear in the text box. This will measure the DC voltage of the node. Similarly, clicking on ‘**idc**’ will measure the DC current, ‘**vf**’ and ‘**if**’ will measure the frequency-domain voltage and current respectively, ‘**vt**’ and ‘**it**’ will measure the time domain voltage and current respectively. You can also select functions from the ‘**Function Panel**’ button to perform advanced mathematical manipulations of the signal.

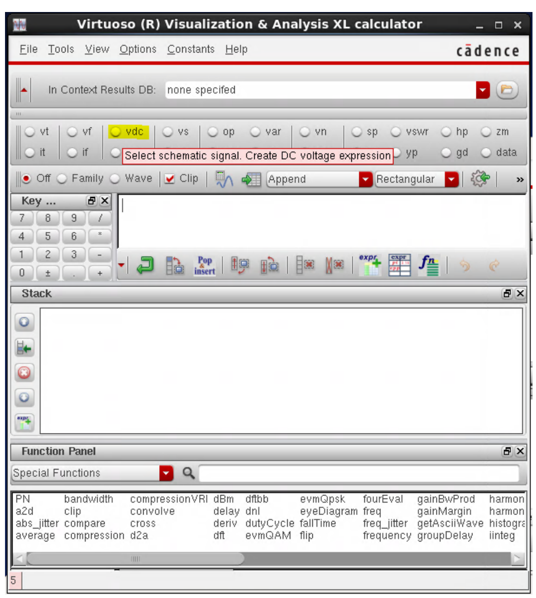


Figure 3. ADE L – Visualization and analysis calculator.

The expression for calculating the on-resistance of the transistor will be '**abs((VDC(source) – VDC(drain))/IDC(drain))**'. Once you finished editing the expression, go back to the output setup window and click '**get expression**', the expression will be automatically copied. A proper name should be given to the expression and then click '**add**'.

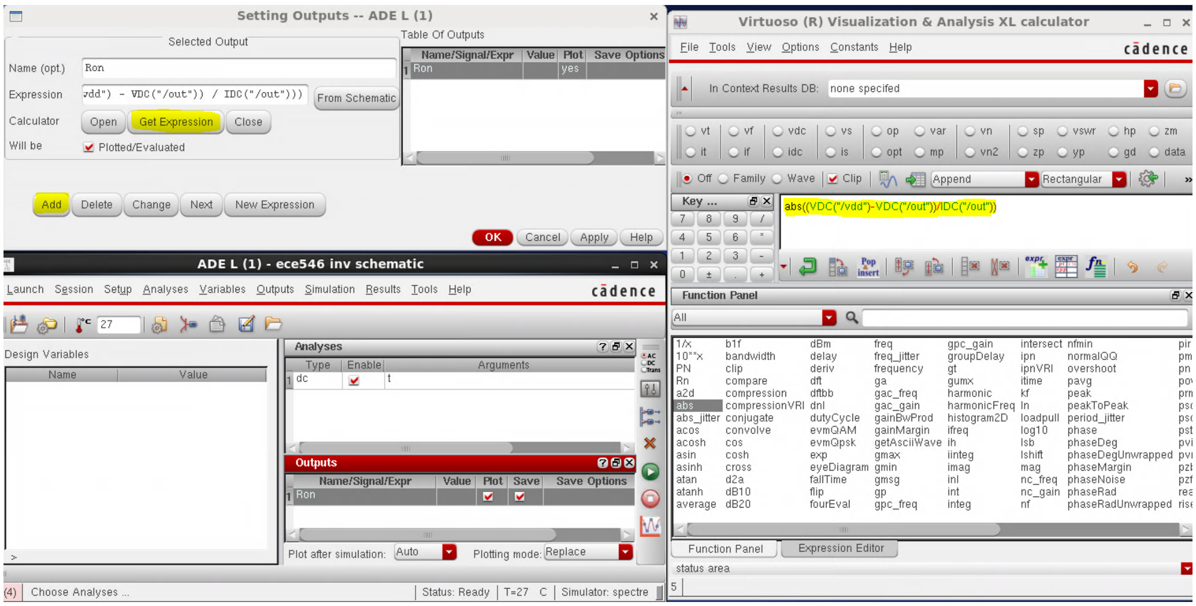


Figure 4. ADE L – Implementing mathematical expressions

2.Transistor model

The transistor in the inverter-based transmitter can be modeled as an ideal switch and a series resistor as shown in Figure 5.

Draw a similar model for the differential transmitter, channel and termination from homework 9. Comment on the target on-resistance of each transistor.

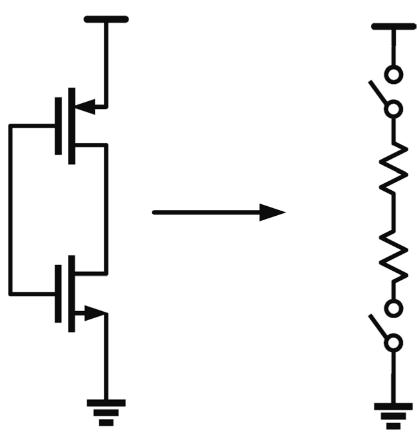


Figure 5. CMOS inverter and switch equivalent-circuit.

3. Sizing the transistor

Note that the on-resistance of the transistor not only depends on the voltage drop across it but also on the absolute voltage of both the source and the drain.

Calculate the source and drain voltages needed to measure the on-resistance of each transistor.

4. Simulation

In Cadence virtuoso, implement the DC analysis and extract the width of each transistor to ensure a 50-ohm match. Run the same step function as in homework 8 for at least 60 ns and comment on the results (input waveform of TX, input waveform of channel and output waveform of the channel).

PART II

In this part, you will extract the pulse response of the given channel, extract the decision feedback equalization (DFE) coefficients to equalize the channel and examine the equalization result by using a behavioral implementation of DFE in VerilogAMS.

1. 1. Extract pulse response of the channel

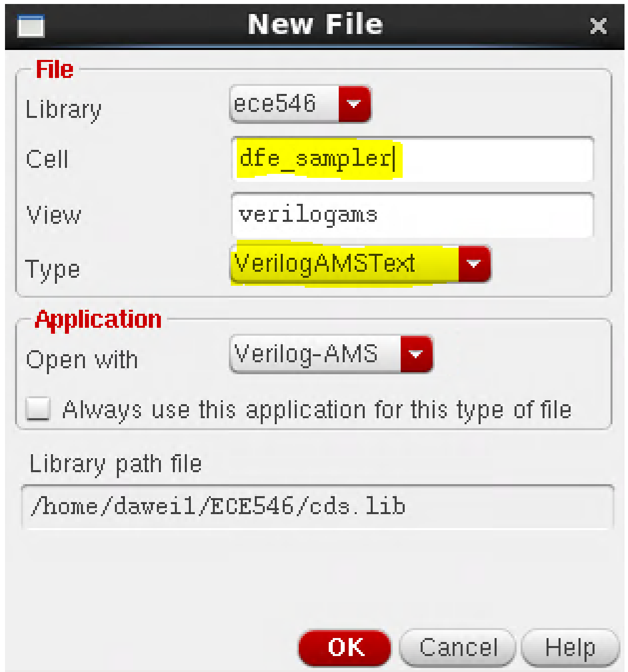
You should generate a pulse input with a 400ps pulse width, a 20 ps rise and fall time, and a period of at least 60 ns. The input and output of the channel should be matched to 50 ohms.

2. 2. Find the post cursers

Plot the pulse response of the channel, comment on the result, note the main post curser(s) and determine your DFE coefficients.

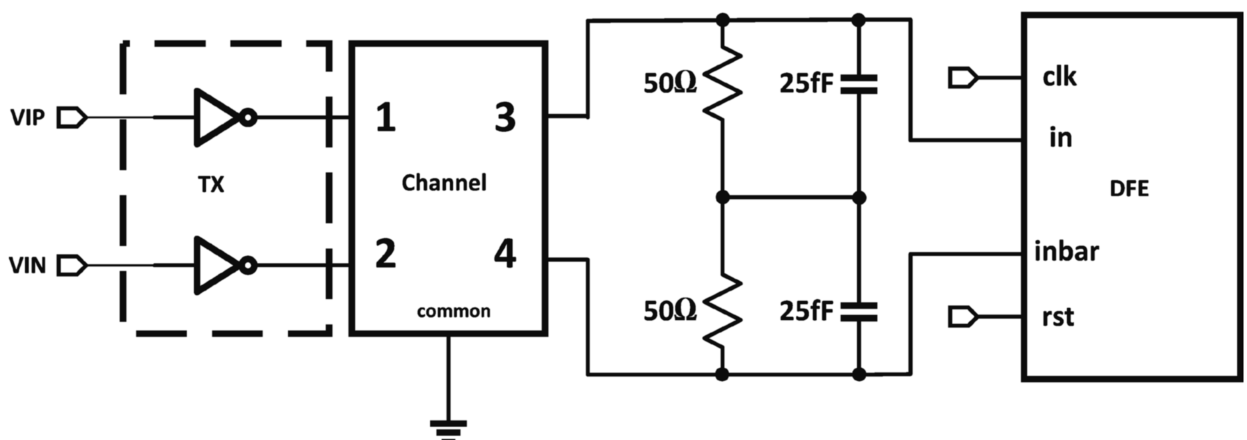
3. 3. VerilogAMS tutorial

3.1. Create a new CellView and choose the **'VerilogAMSText'** as the type. Note that the cell name should be exactly the same as the module name of the Verilog block.



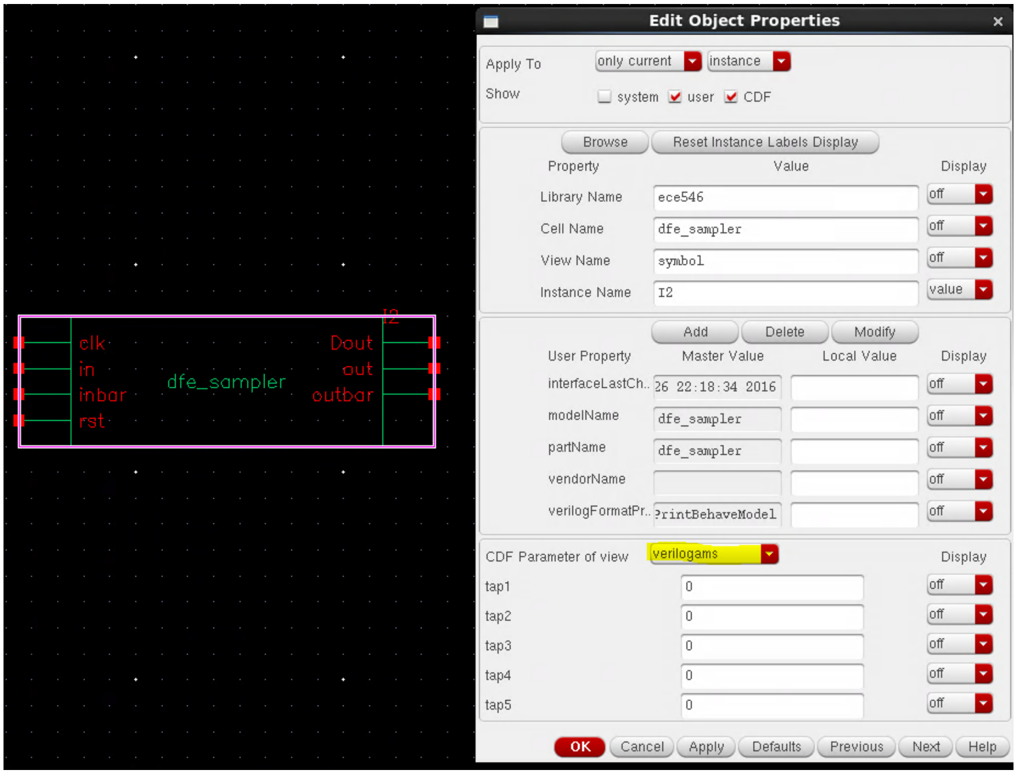
3.2. Now you can copy and paste the given dfe sampler Verilog code (http://emlab.uiuc.edu/ece546/tools/verilog.vams) into the text editor. When you close it the code will be automatically compile and virtuoso will ask you whether or not to generate a symbol for it. Please click '**yes**'. If there is no symbol generated, it is usually due to the code not being compiled. Please make sure the code is the **last** file to be saved and closed. You can close all the text editor sessions and re-open the code, make any change then close it again to force compilation. If there is any error, please go back to CIW window to debug.

3.3. Next, create the text bench for the DFE sampler. An example schematic that shows how to integrate the DFE sampler with the existing system is included below.

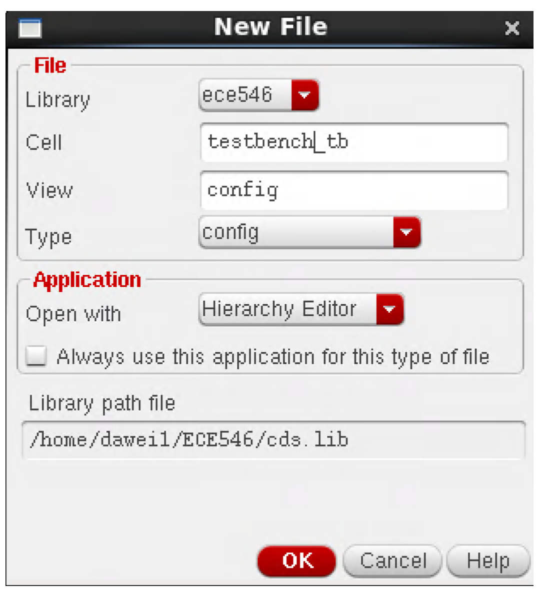


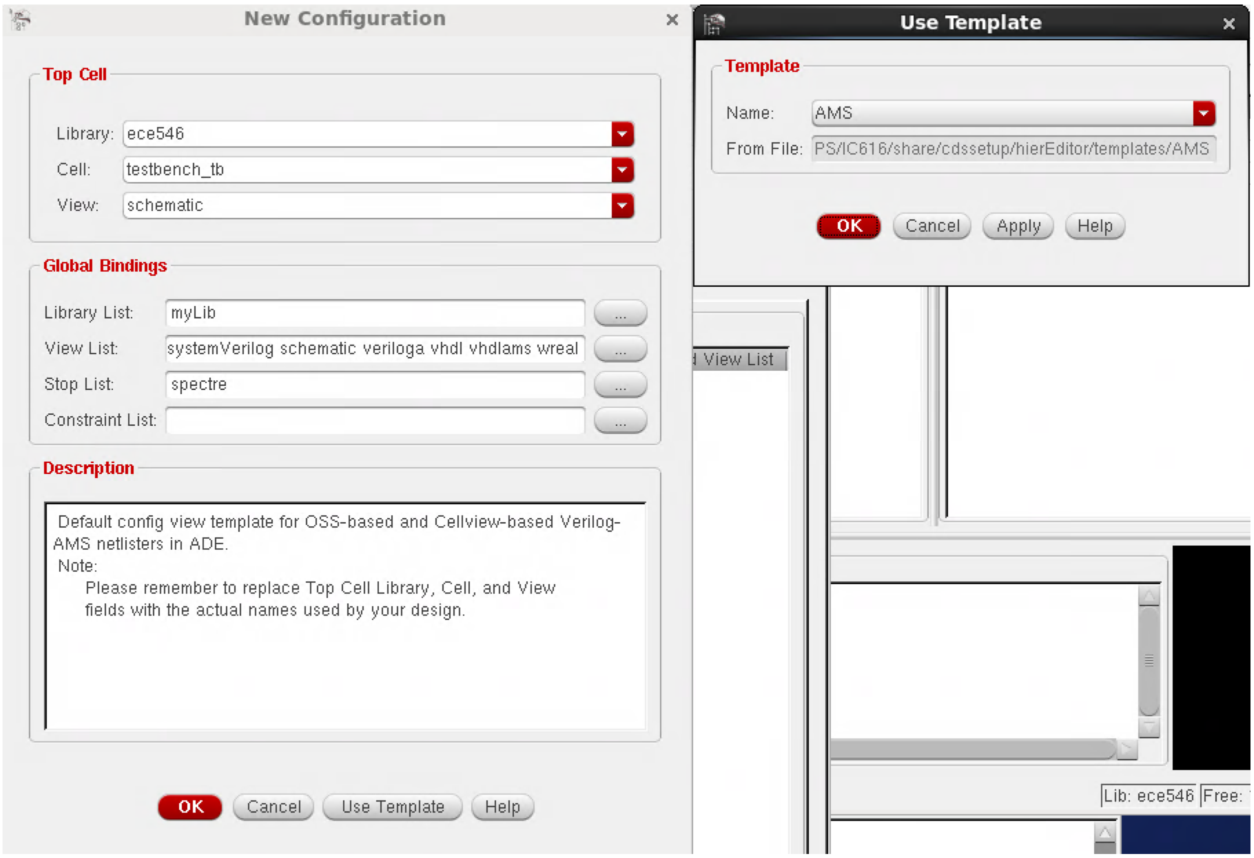
3.4. You can right click the DFE block and choose '**property**' -> '**CDF Parameter of view**' -> '**verilogams**' to change the DFE coefficients. The DFE block has the following inputs: **in** and **inbar** are the differential channel input; **rst** is the reset signal to initialize the block; **clk** is the clock signal to sample the incoming waveform (eyeopen >= 400mV). The outputs are as follows:

out and **outbar** are the differential outputs after equalization; **Dout** is the digital decision of the input waveform.

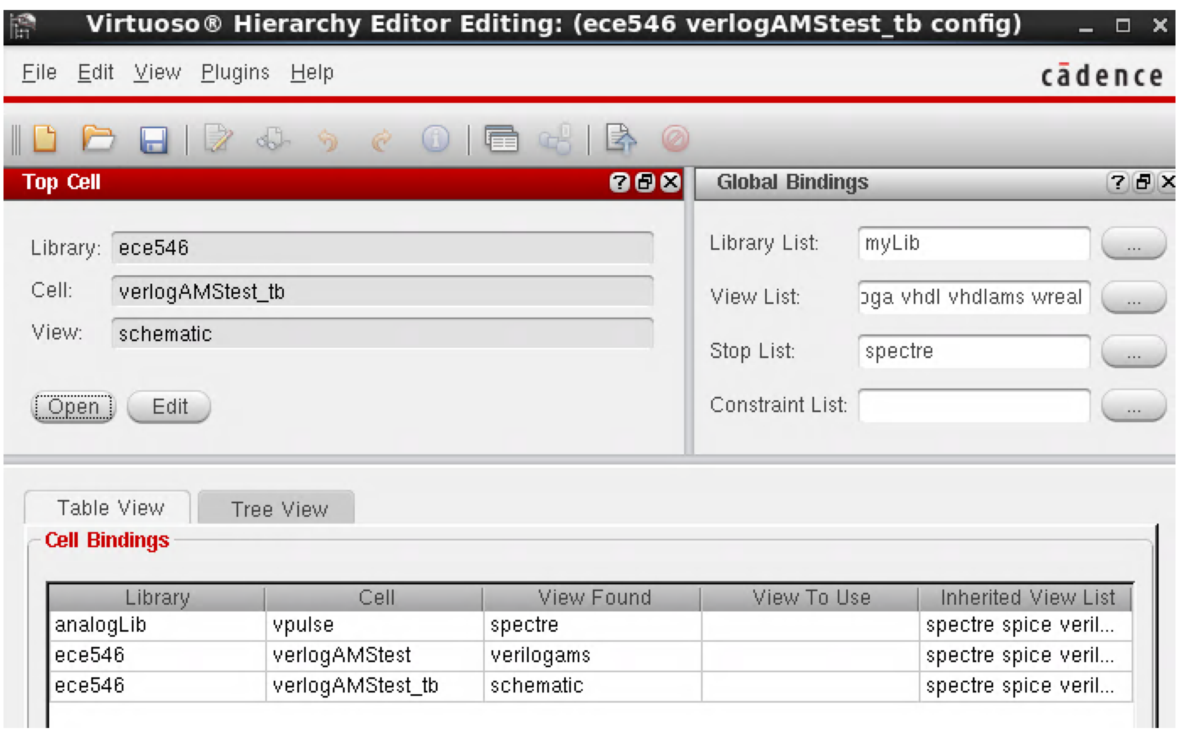


3.5. After the testbench schematic, a testbench config view is needed to co-simulate the VerilogAMS blocks with transistor blocks. To create the config view, highlight your testbench, create a new view, choose the '**config**' as the type. Then on the newly popped window choose '**Use Template**' -> '**Name**' -> '**AMS**', '**View**'->'**schematic**'.

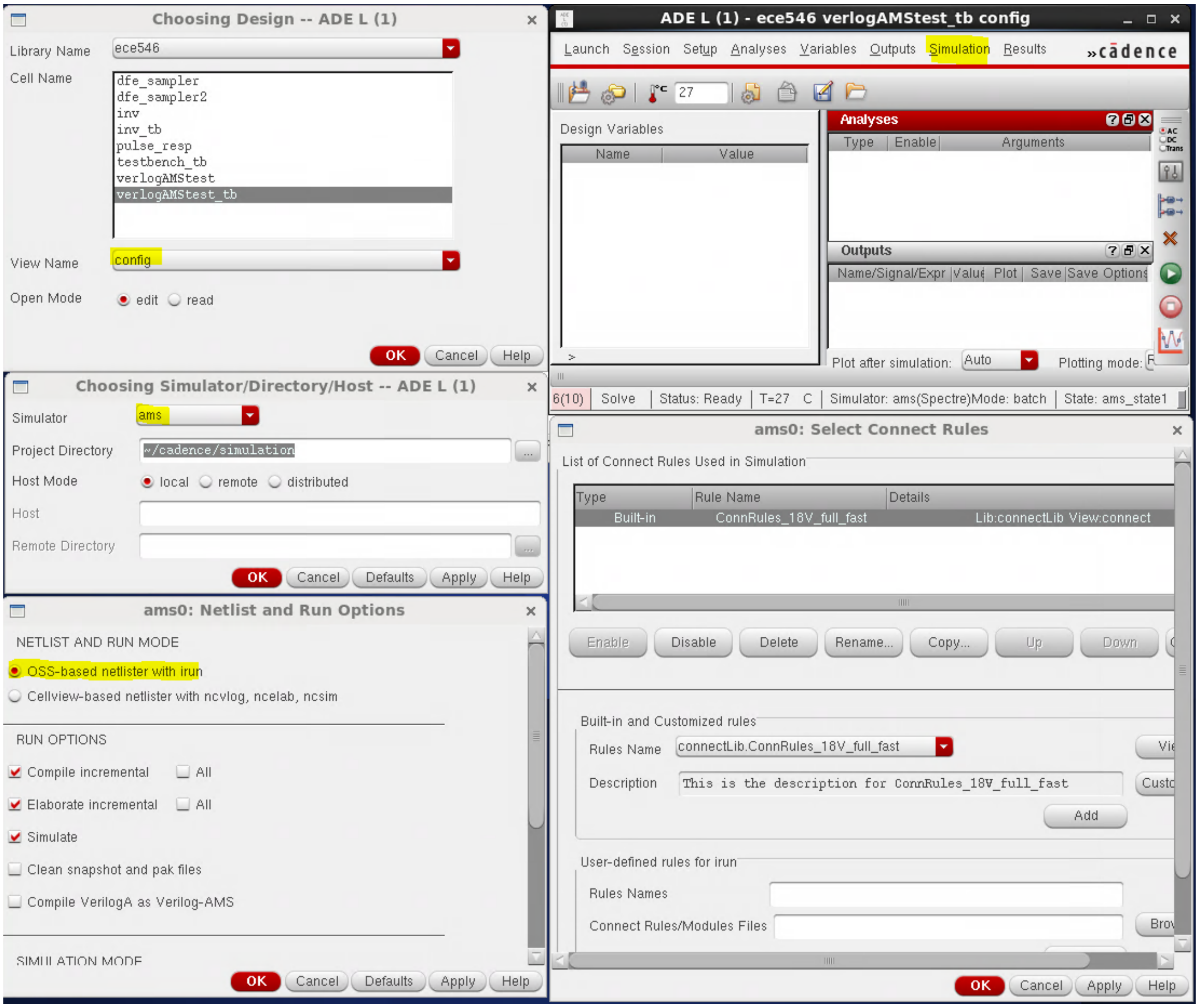




3.6. In the Hierarchy editor make sure all the cells are resolved and right views are used for the simulation. Then click '**Open**' to open the config view. You can start ADE as usual.

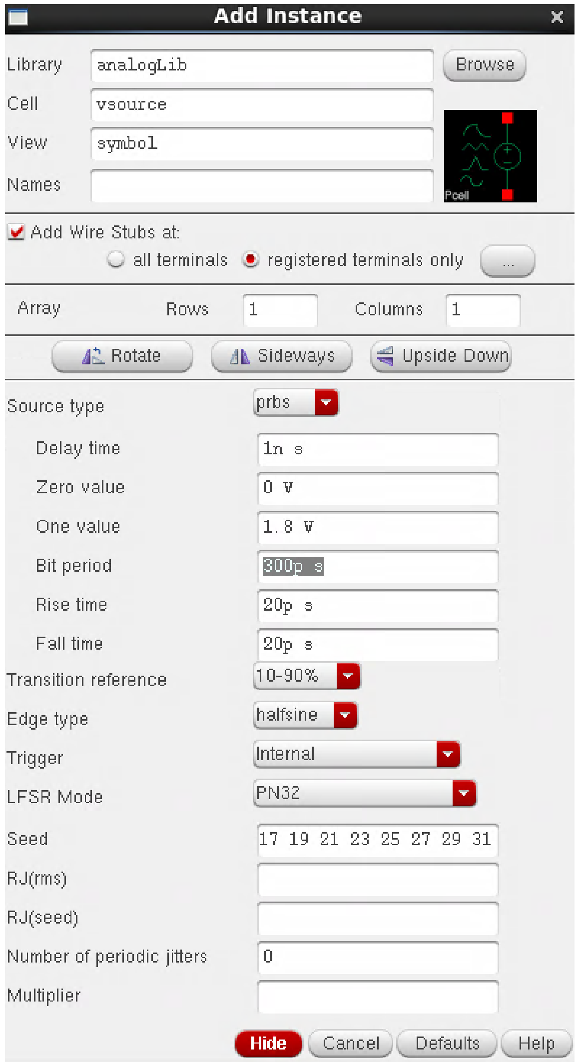


3.7. In the ADE environment, the simulator should be changed to ‘**ams**’, the view name of the design to be simulated should be ‘**config**’. In ‘**Simulation**’ -> ‘**Netlist and Run Options**’, choose ‘**OSS-ased netlister with irun**’ as the run mode. In ‘**Setup**’ -> ‘**Connect Rules**’ make sure the built-in ‘**ConnRules_18V_full_fast**’ is chosen.

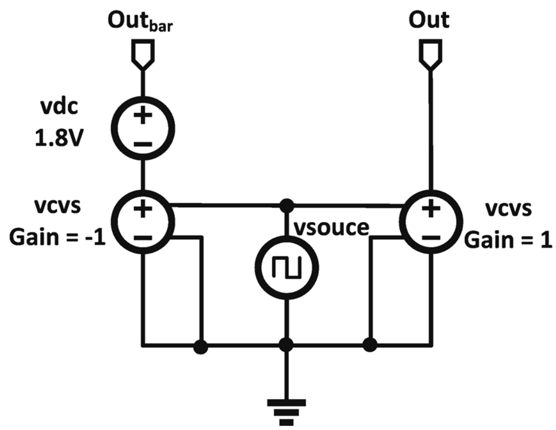


Use the DFE coefficients you determined earlier, set the input of the TX to PRBS31 with bit period of 400 ps with 20 ps rise and fall time, plot the eye diagram of the output of the channel and the output of the DFE block. Comment on the results.

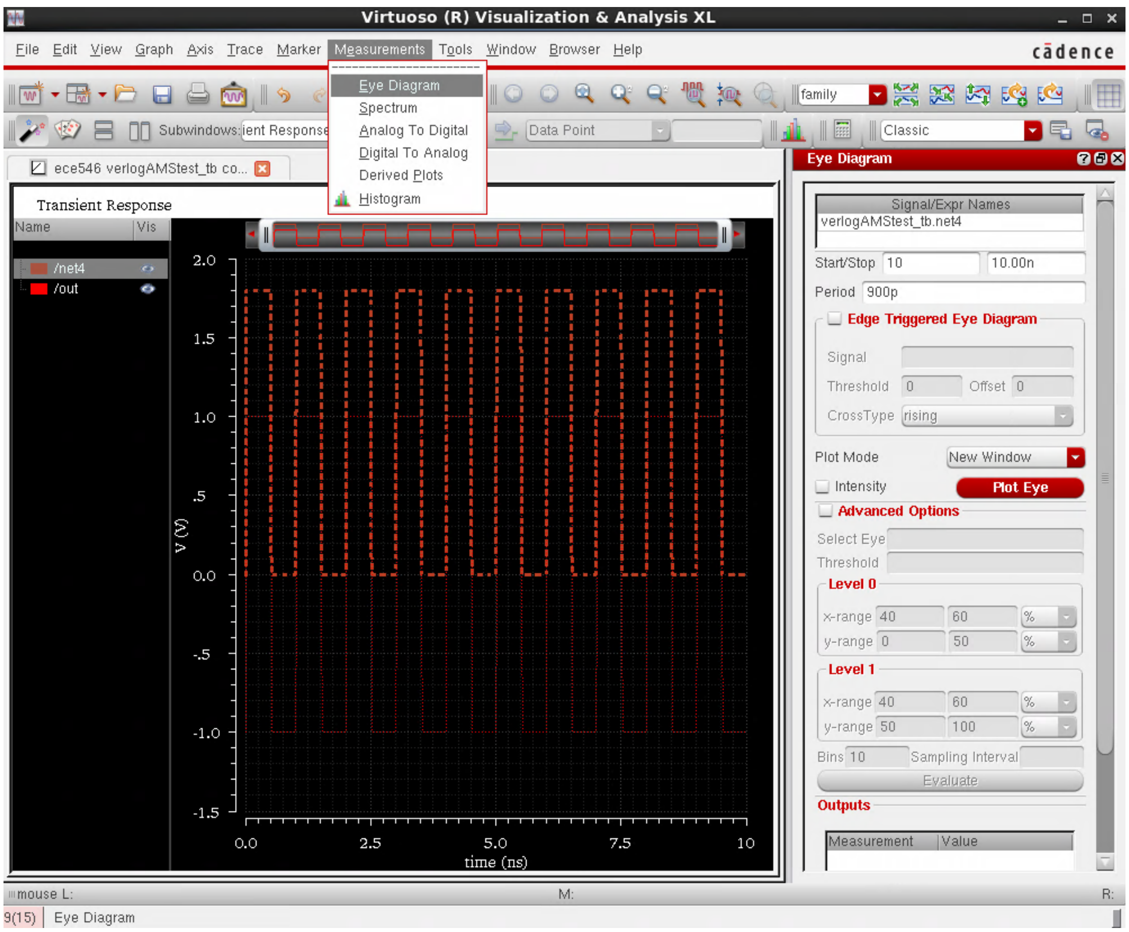
Note1: a PRBS31 source can be created by using '**vsource**' from '**analogLib**'



Note2: A differential PRBS31 source can be created from '**vsource**' and '**vcvs**' (voltage controlled voltage source) from '**analogLib**'



Note 3: To create the eye diagram, go to '**Visualization & Analysis**', choose '**Measurements**' -> '**Eye diagram**', Choose the signal you want to plot on the left column and specify the start/end time (the sequence should be long enough), period (> 2 bit period) on the right column.



Note 4: Open the VerilogAMS file to understand the algorithm. For VerilogAMS syntax please go to http://www.designers-guide.org/VerilogAMS/