ECE 546 HOMEWORK No 9 Due Wednesday, April 17, 2024

In this homework you are going to build a simple inverter based transmitter, simulate it with the provided channel s4p file and analyze its response.

1. Get a ***FastX*** client (version 1) from webstore and follow the installation instruction to login to your designated server.

2. After login, go to the **ECE546** folder in your home directory from a terminal and type **'virtuoso &'**. Then Cadence Virtuoso will start. Notice that the top window in Figure 1 will be referred to as '**Library manager**' and the bottom window will be referred as '**CIW**'

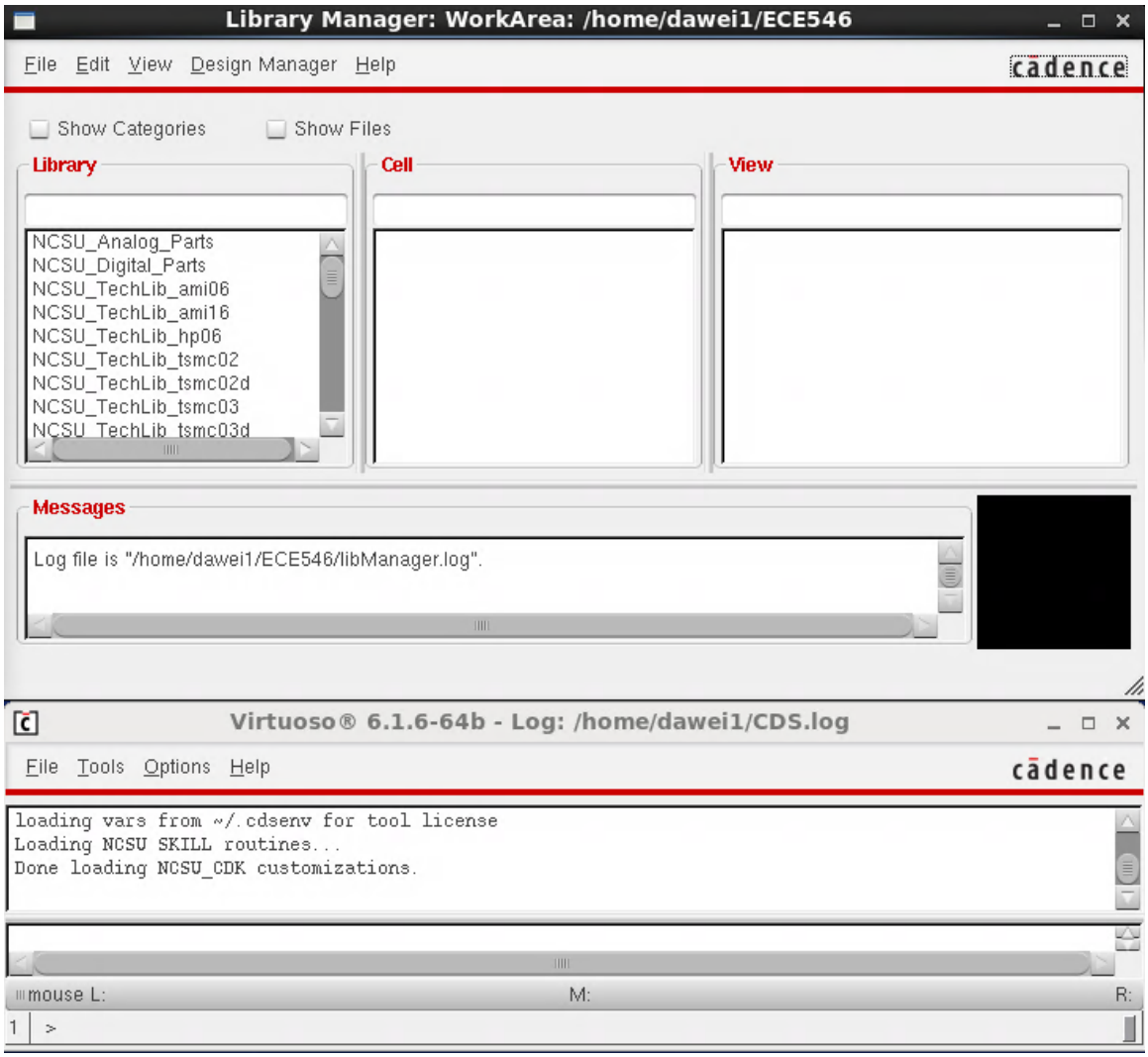

Figure 1. Window view for steps 1 and 2

3. Now you are going to create a library. First, identify the CIW window shown in Figure 1, then go to **'Tools->library manager'** a new window will pop up as shown in Figure 2.

4. In the library manager window go to **'file->new->library'** and type **'ECE546'** in the '**name**' field and click the "**OK**" button.

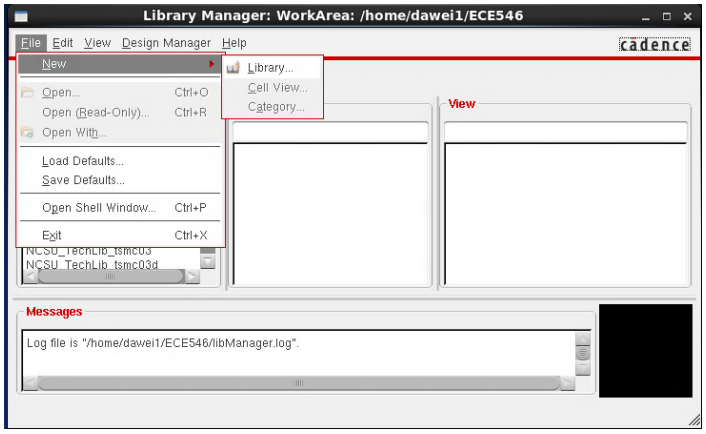

Figure 2. Window view for step 4.

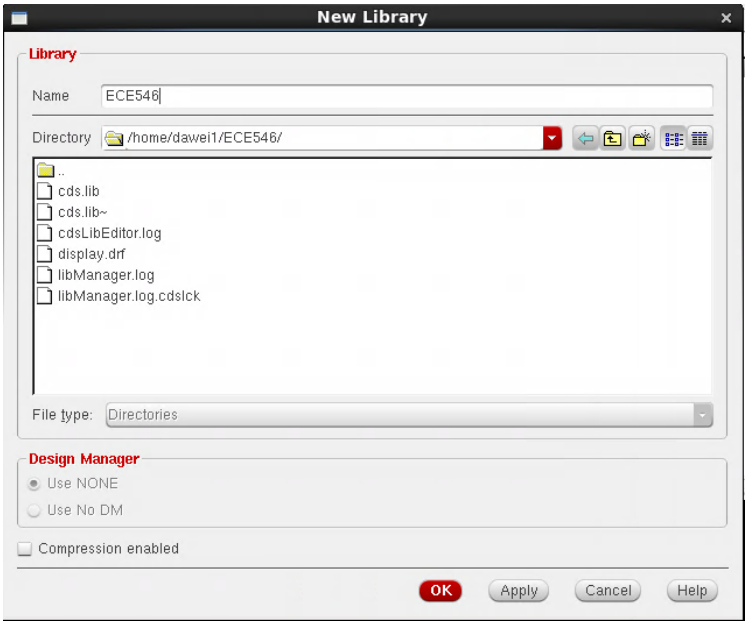

Figure 3. Window view for step 4.

5. A new pop up window as in Figure 5 **'attach to an existing technology library**'. Choose **'NCSU_TechLib_tsmc02d'.**

6. Go back to the library manager and choose library ECE546 (you just created it), when it is highlighted, go to **'File->new->Cell View'** a new window like figure will pop up. Type **'Inv'** in the '**Cell**' field and click '**OK**'. The cell named '**Inv**' is created and the schematics editor will open it in editing mode automatically.

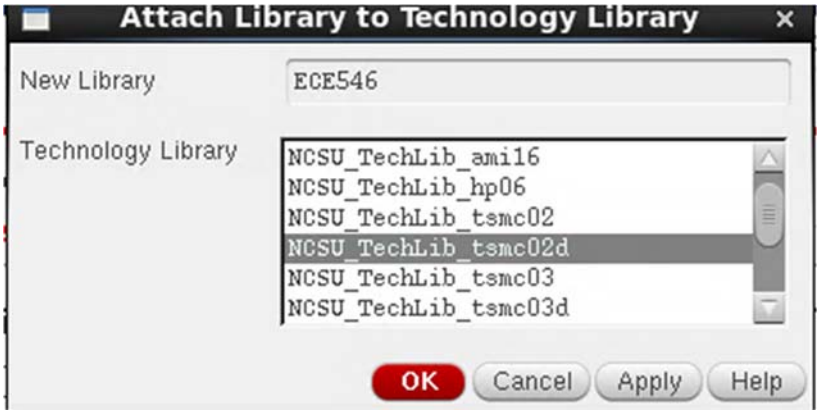

Figure 4. Window view for step 5

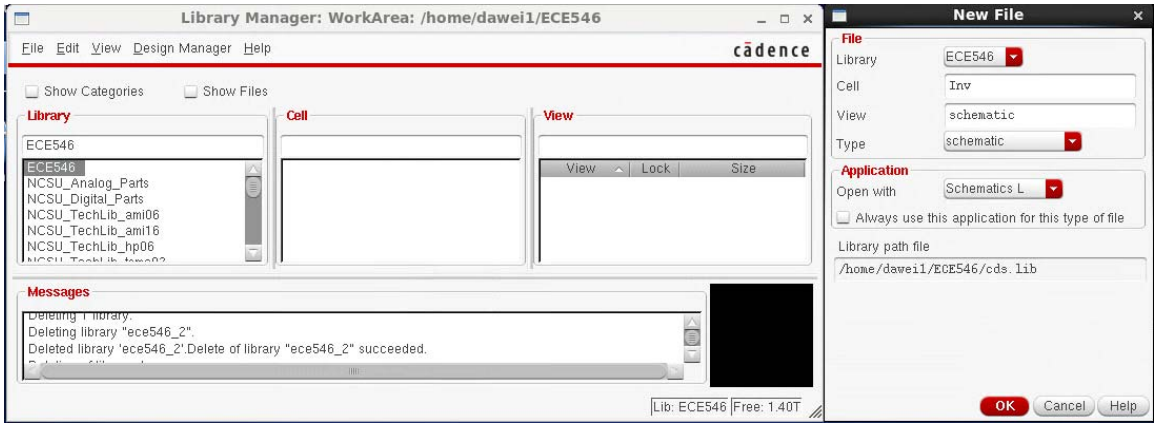

Figure 5. Window view for step 6.

7. Now you are going to add transistors to the schematic. Press the key '**I**' and the **'add instance**' window will pop up. You can also go to the pull-down menu **'Create->Instance'** from the schematic editor to create an instance in the schematic.

8. On the '**Add Instance**' window, click '**Browse**' and a new window will pop up as shown in Figure 6. Choose "**NCSU_Analog_Parts**" as the library and '**nmos**' as the cell, '**symbol**' as the view. Next, go back to the schematic window and click anywhere of the empty space; an nmos transistor symbol will be added. You can press '**ESC**' to cancel the add instance command. Please use the same method to add a pmos transistor with minimal length and width.

9. Now you are going to make some connections. In the schematic editor press '**w**'. This will allow you to add wires. You can alternatively go to the pull-down menu **'Create->wire(narrow)'** from the schematic editor. Single click will define a start point

and double click will define the end point of the connection. Next, connect the pmos and nmos devices created in step 8 to build an inverter circuit.

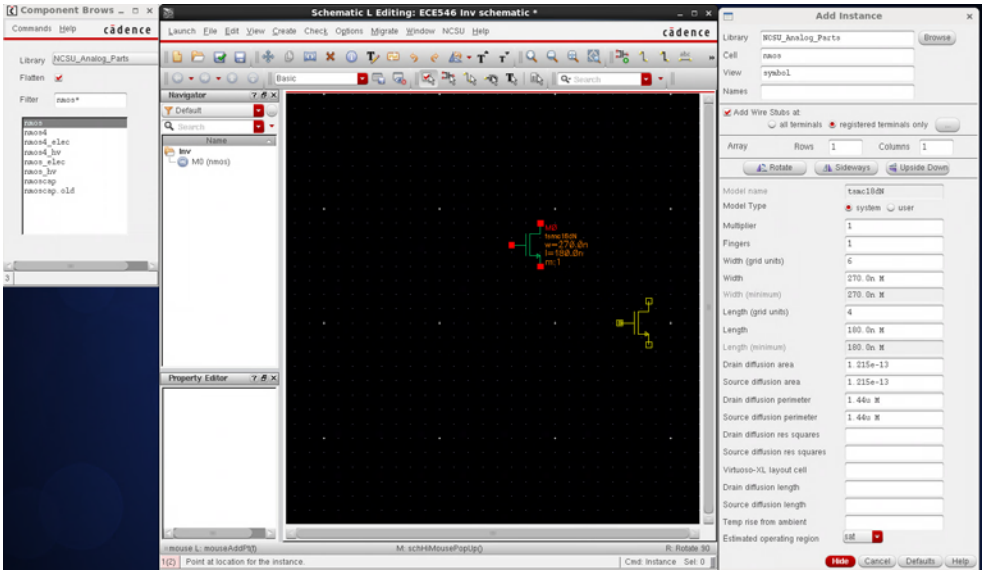

Figure 6. Window view for step 8

10. You will now create the I/O ports. Press '**p**' and enter the pin creation window as shown in the figure. You can also enter this mode by going to **'Create->pin'**. Type '**in**' in the '**name**' text box and choose '**input**' as the direction. Then click on any empty space in the schematic editor to place a port '**in**'. Create port '**out**' as output, '**VDD**' and '**gnd**' as **InputOutput** and connect them to the inverter you just built. The final circuit is shown in Figure 7.

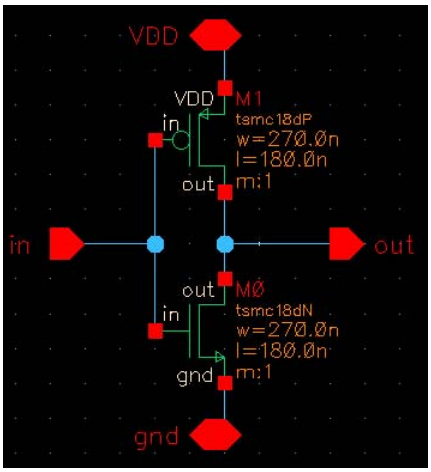

Figure 7. Window view for step 10.

11. The last step is to create a symbol for the inverter so that you can instantiate it in other blocks. Before that, you need to check and save the schematic. Please go to **'File->Check and Save'**.

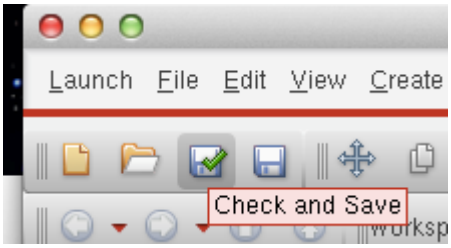

Figure 8. Window view for step 11.

There should be no warning nor error. If there is one, go to the CIW window for the logs and information to debug your schematic. Once the schematic is clean, go to **'Create->cellview->from cellview'**, keep the default setting and click '**OK**'. Next, you need to define the pin locations. Usually we want '**VDD**' on top, '**gnd**' at the bottom, inputs on the left and outputs on the right.

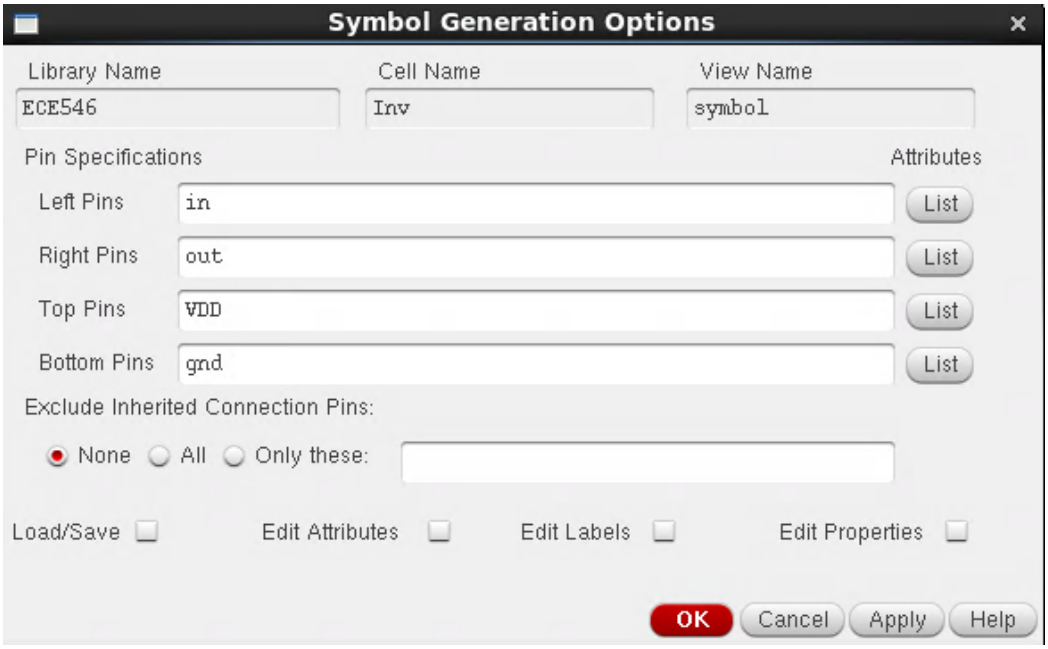

Figure 9. Window view for step 11.

Once you have adjusted your pin locations click the '**OK**' button, the symbol editor with the automatically created symbol for your inverter will appear. Check and save the symbol and the inverter is successfully created.

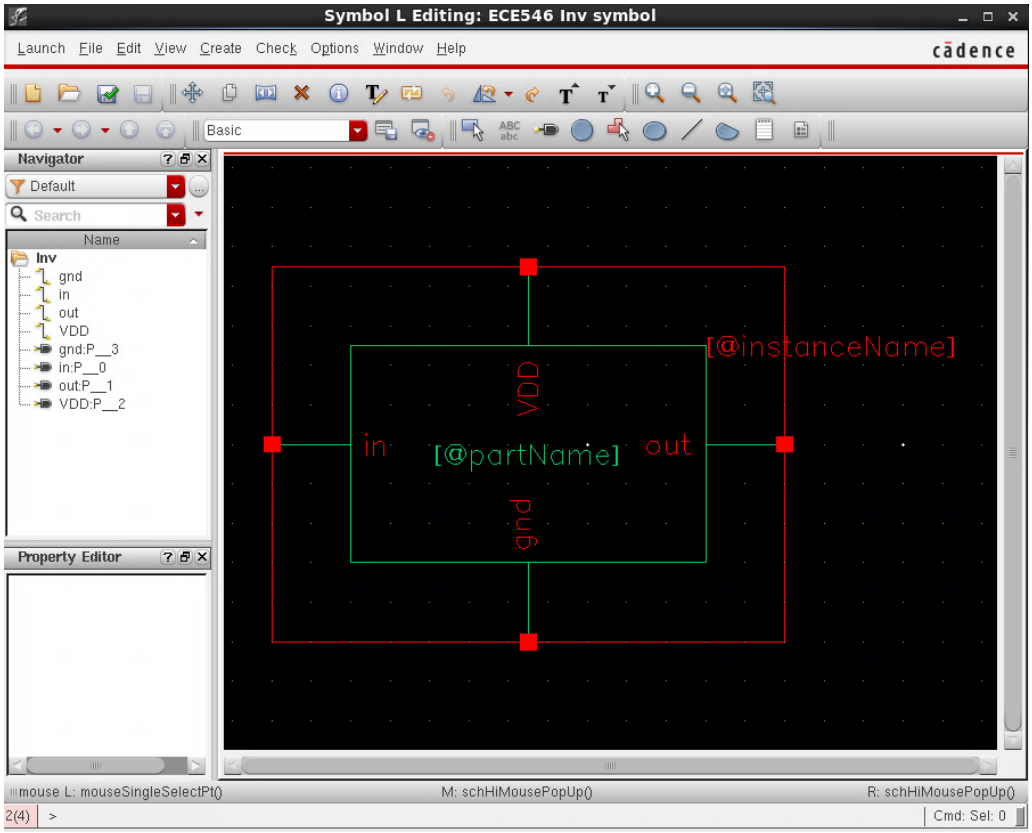

Figure 10. Window view for step 11.

12. Now you are going to create the testbench for your inverter. Create a new cellview in the ECE546 library and instantiate the inverter from library **'ECE 546'** just as you instantiated the pmos and nmos transistors. Then from library **'analogLib'** instantiate the dc source **vdc** and set the DC voltage to 1.8V. Connect the positive port of the DC voltage source to the VDD port of the inverter. Connect the ground port, '**gnd**' to the global ground. Next, from library **'analogLib'** instantiate the voltage step generator **vpwl.** This will be your input. Please set the **'number of voltage time pair'** to 3 and enter the following voltage/time pair information:

Time	voltage
0	0
10n	0
10.02n	1.8

This will create a unit step function *u(t-10n)* with rising time 0f and 20ps. Add a capacitor of 10fF from analogLib (part name: cap) between the output and ground and create an output pin, then check and save your testbench. The final circuit should be as shown in Figure 11.

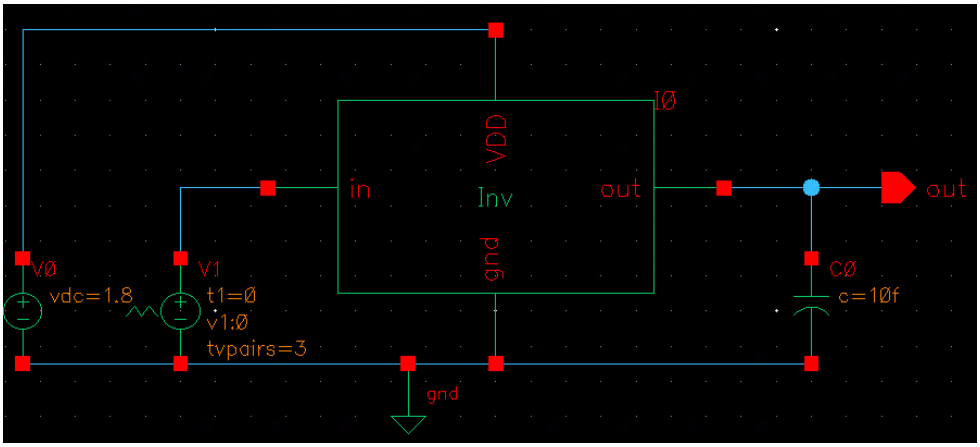

Figure 11. Window view for step 12.

13. The next step is to run a transient simulation with the newly built testbench. From the schematic of the testbench, go to **'Launch->ADE L'**. The ADE L window will appear as shown in Figure 12.

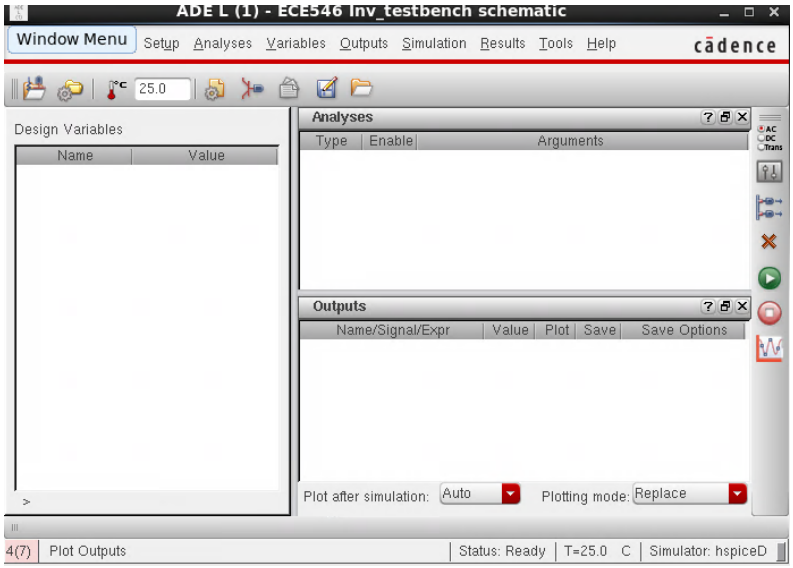

Figure 12. Window view for step 13.

14. First go to **'setup->Simulator/Directory/Host'**, on the newly popped window. Change Simulator from '**hspiceD**' to '**spectre**'. You can also specify the simulation file folder in the '**Project Directory**' field. Next, click the **'Choose Analysis'** icon to choose the simulation type.

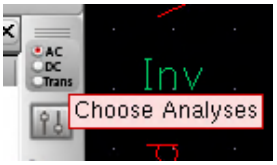

Figure 13. Window view for step 14.

There, you need to choose '**tran**' with a stop time '**20n**', and '**conservative**' as the accuracy. You can also click '**option**' to fine tune the simulation parameters but the defaults are good enough for this homework. Click '**OK**' when you are done.

15. You will next add the signals to be displayed after simulation. Click the '**Setup Output**' icon.

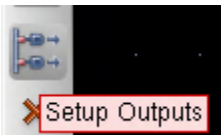

Figure 14. Window view for step 15

The signal selection window will pop up. Click **'From Schematic'** and click on the testbench schematic to select the signals you want. Here we want the output and the input of the inverter. After choosing all the signals, press '**ESC**' to quit command mode and get back to the ADE window.

16. Go back to the ADE L window and choose **'output->Save all'**. In the field **'Select signal to output(save)'** choose '**selected**'. This is important since the default selection will save all the signals (most of which are useless for our purpose), which would generate too large a dataset and would dramatically reduce HDD performance.

17. On the ADE L window, choose '**Setup-> Model Libraries**', in '**Model Library Setup**' window add the pmos and nmos model files as shown in Figure 15.

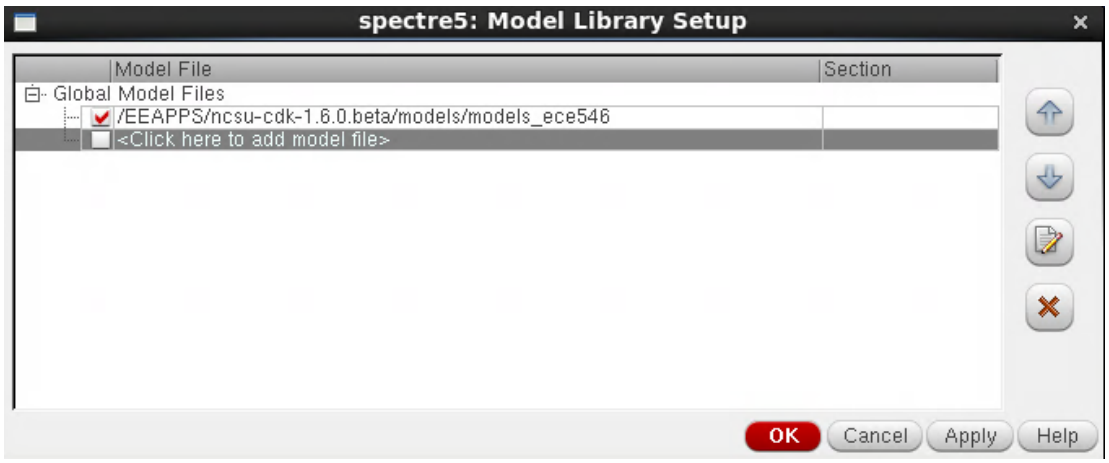

Figure 15. Window view for step 17.

17. Click the "**Run**" green button to start simulation. The program will run and generate some plots. Include the results and provide your comments.

Figure 16. Window view for step 17

18. Change the load capacitor to 100fF and re-run the simulation. Include the resulting plot and compare with the plot from step 17.

19. Use '**nport**' from '**analogLib**' (detailed setup on next page, Figure 18) to simulate the inverter based transmitter with the four-port channel from the S-parameter file TYCO.s4p (http://emlab.illinois.edu/ece546/tools/TYCO.s4p). You need to add another inverter to generate a differential input of the channel. The channel needs to be terminated as shown in Figure 17. Plot the results of the differential input of the inverter based transmitter, differential input of the channel and differential output of the channel. Comment on the results.

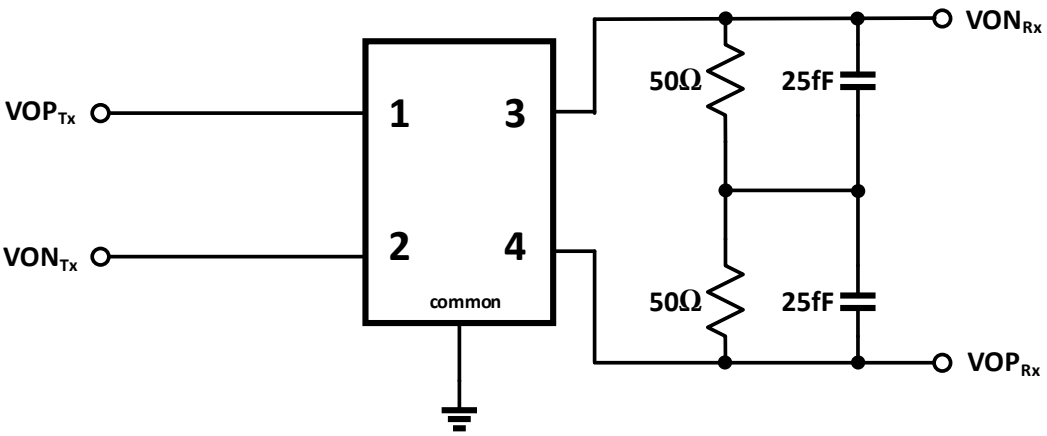

Figure 17. Channel termination diagram

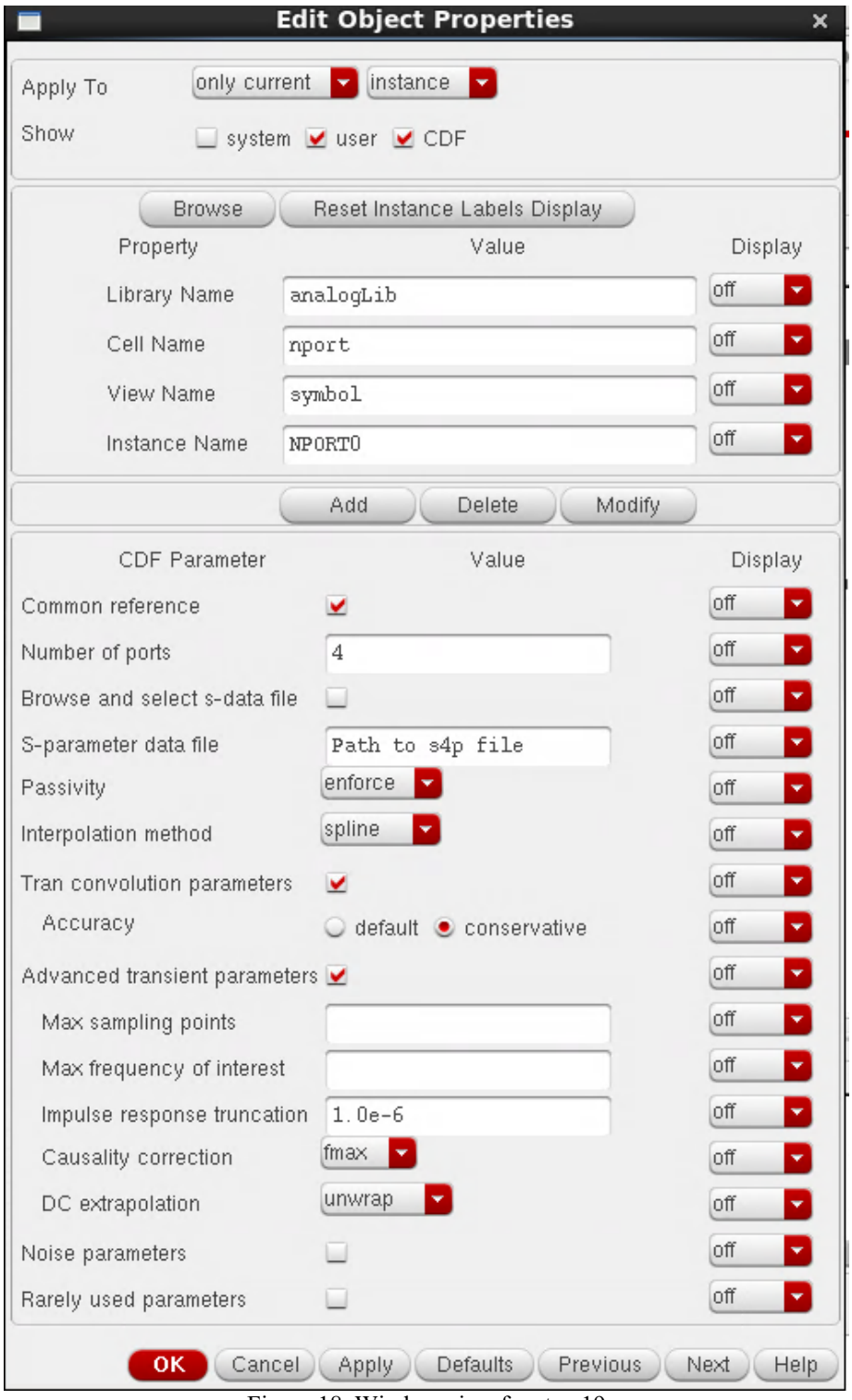

Figure 18. Window view for step 19