ECE 546: Advanced Signal Integrity

High-Speed Serial Link (HSSL) Design Project

1 Overview

Technology scaling and unprecedented growth in demand for ubiquitous fast, robust computing. With the rise of heavy duty data centers to handheld mobile devices, the desire for faster, low-power integrated inter-IC communication protocols is at an all-time high and has led the roadmap of the semiconductor industry, making it one of the fastest growing yet fiercely competitive industry. With the growing needs for ultra-low power yet multi-Gbps signaling in both wired as well as wireline applications, integrated systems on chip (SoCs) have become mainstream critical components in modern computing systems. Ability to process and access 'big-data' are the fundamental demands in modern society where every second saved in prompt communication as well as computation of information is critical. In order to meet these needs of fast, robust signaling over the same old "lossy" channels, the clock-frequencies need to scale accordingly and clever I/O links need to be developed. Figure 1 shows a typical Serial Link that consists of a Transmitter (TX) with an externally provided TX_CLK, channel, Receiver (RX) with a forwarded clock and optional equalization schemes.
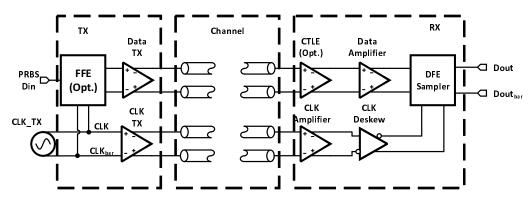

Figure 1: Basic Link High-Level Description

In this design-project you (in a team of 2) will explore the signal integrity issues experienced by High-Speed Link Designers on both a system-architecture level as well as the circuit level. The TX_CLK signal will be provided to you and and clk_deskew can be implemented by the ideal delay cell found in analogLib library. Your task would be to implement the TX and RX at transistor level; that channel in HFSS and equalization blocks if necessary in VerilogAMS. The final integration and simulation should be done by using Cadence Virtuoso. It may also be helpful to use tools like MATLAB and Agilent ADS during the design and verification process to meet the provided specifications.
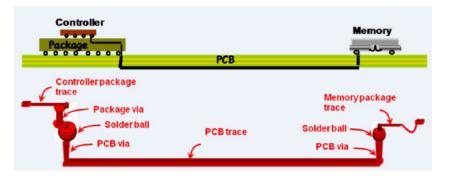

Figure 2: A typical controller and memory interface, forming a channel; consider the controller as transmitter and memory as reciever

To validate your design you will need to perform the following analyses:

1. **Timing Budget:** Calculate all contributions to timing uncertainty and compute the net timing margin.

2. **Noise Budget:** Calculate all contributions to noise and interference and compute the net noise-margin, SNR and BER.

3. **Channel Design and Modeling:** The channel connects chip through package to board as shown in Figure 2. Design a complete channel that includes wire bonding, package trace, package via, solder bump, PCB via, and PCB trace. Define appropriate ports and generate S-parameters using HFSS. The PCB trace(s) should be at least 20 inches in length.

   Build an accurate SPICE model of your channel from the obtained S-parameters and characterize it using a simulated TDR response. Additionally, simulate your timing and signaling conventions on this channel using a PRBS-31 sequence to generate an eye-diagram. Compare the simulated eye opening with your computed voltage, timing margins and characterize the 'worst-case' eye.

4. **Circuit Simulation:** Perform transistor-level simulation of your design using Cadence Virtuoso using the NCSU 180nm PDK provided in the class server or any other PDK you have access to through your research group.

2   Design Specifications

The following design specifications should be met by your design:

1. $V_{Supply} < 1.8V$

2. Data-Rate $\geq 3Gbps$

3. $BER < 10^{-12}$

4. Receiver eye opening $> 400mV$.

5. PCB trace(s) length $> 20\ inches$.

3   Grading

Your project will be graded according to the following criteria:

1. Completeness of design and analysis (60pts)

2. Robustness of design (20pts)

3. Creativity and elegance of design, i.e. "style-points" (10pts)

4. Low-power and High-Speed metric (10pts)

A detailed project report is required along with your design files by the project due-date, **May 13, 2022** before **midnight**. Few minimum requirements for the report are listed below:

1. Overall Design Approach: Describe your complete design at a system level and include a narrative, system-level block diagram.

2. Details of your signaling approach (i.e. Differential or Single-Ended).

3. Details of your timing and synchronization approach with timing budget that includes a list of all bounded as well as statistical sources of jitter.

4. A detailed design and implementation guideline for your equalization scheme.

5. Analysis of your signaling convention giving a noise-budget and calculation of worst-case ISI, cross-talk effects.