Cadence Virtuoso IC 6.16 Schematic Capture Tutorial

ECE 546 - Advanced Signal Integrity

Contents

1 Introduction

The motivation for this manual is to provide a step-by-step tutorial to design and simulate circuits using Cadence IC 6.16 Virtuoso Design Environment. In this short-tutorial students are exposed to the steps involved in remotely connecting to the EWS servers and launch the Virtuoso simulator engine from the terminal window followed by a detailed guide to create their own custom circuits and simulate them using the Cadence Spectre circuit simulator.

Cadence is an Electronic Design Automation (EDA) environment that integrates various circuit design and verifications applications and tools (both in-house proprietary as well as external third party vendor tools) in a single framework allowing unified IC design and verification in a single environment. The tools are generic and allow the designer to configure the environment depending on the fabrication technology of choice by installing the appropriate PDK (Process-Design Kit).

This tutorial document is not intended to be a one-stop reference for all the features available in Cadence Virtuoso Design Environment. Instead, it's only meant to be a quick-start guide for circuit designers to be able to use the EDA tool to effectively simulate their designs for quick prototyping and verification of their designs.

2 Environment Setup

In order to remotely login to the EWS Linux Servers follow the instructions provided below:

1. Windows OS Users:
   (a) Install **PuTTy**[`www.chiark.greenend.org.uk/~sgtatham/putty/download.html`], or another such SSH client **MobaXterm**[`http://mobaxterm.mobatek.net/download-home-edition.html`] depending on your preference.
   (b) Install **Xming X Server** [`http://sourceforge.net/projects/xming/`] for Windows to allow X-forwarding during the SSH session. Also, install **Xming-fonts** from [`http://sourceforge.net/projects/xming/files/Xming-fonts/`]
   Note: Without installing Xming you will not be able to open Virtuoso or for that matter any application with a GUI.
   (c) Launch your SSH client, type **ssh -X yourNetId@remlnx.ews.illinois.edu**, hit 'Enter'. You will be prompted to type in a password so type in your 'AD Password' and again hit 'Enter'. Now you can follow the steps outlined in Figure 1.
2. Mac OSX Users:
   (a) Install **XQuartz 2.7.5** for Mac OSX if you are using OSX Mountain Lion or later. If you have an older OS then you will already have X11 pre-installed in your system. Check your 'System Preferences' to check whether X11 is turned on.
   Note: Without installing XQuartz or enabling X11 (depending upon your OSX version) you will not be able to open Virtuoso or for that matter any application with a GUI.
   (b) Launch your SSH client and type **ssh -X yourNetId@remlnx.ews.illinois.edu**, hit 'Enter'. You will be prompted to type in a password so type in your 'AD Password' and again hit 'Enter'. Now you can follow the steps outlined in Figure 1.
3. Linux OS Users:
   (a) Launch **Terminal** and type **ssh -X yourNetId@remlnx.ews.illinois.edu**, hit 'Enter'. You will be prompted to type in a password so type in your 'AD Password' and again hit 'Enter'. Now you can follow the steps outlined in Figure 1.

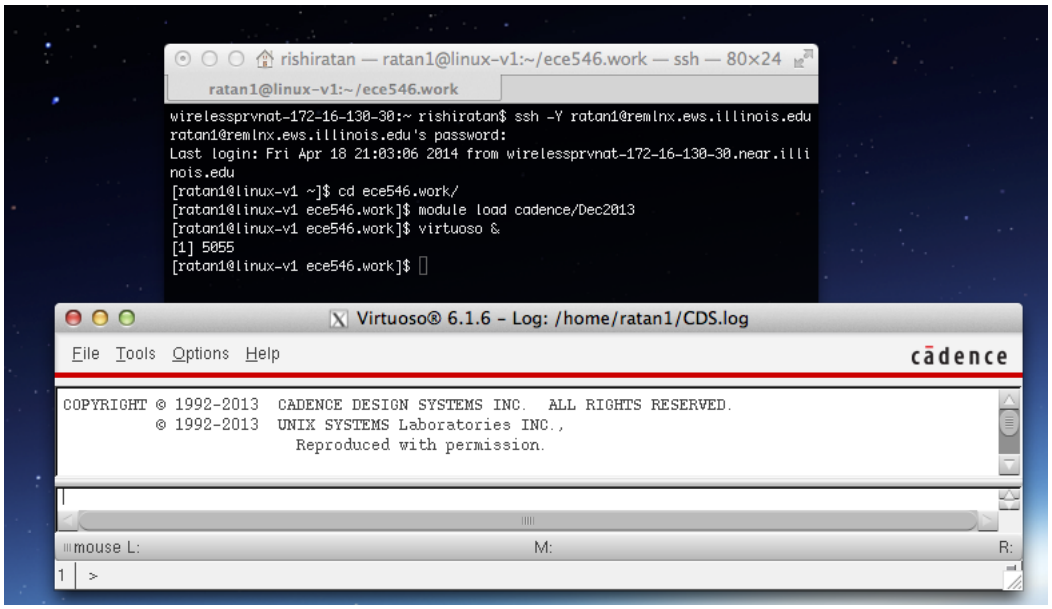


Figure 1: Launch Instructions for Virtuoso

If connecting directly from the EWS Machines, just directy follow the steps outlined in Figure 1. When prompted by the error message shown in Figure 1 select 'Yes'.

3 Schematic Capture

3.1 Creating a New Schematic

1. To view all the libraries in the current work directory click on *Tools* → *LibraryManager* as outlined in Figure 2. and the Library Manager window will pop up as shown in Figure 3.

   Note: If you want to manually add a library that you copied from an external source into your Cadence work directory you would need to edit the *cds.lib* file found in your work directory folder by opening it in a text-editor.

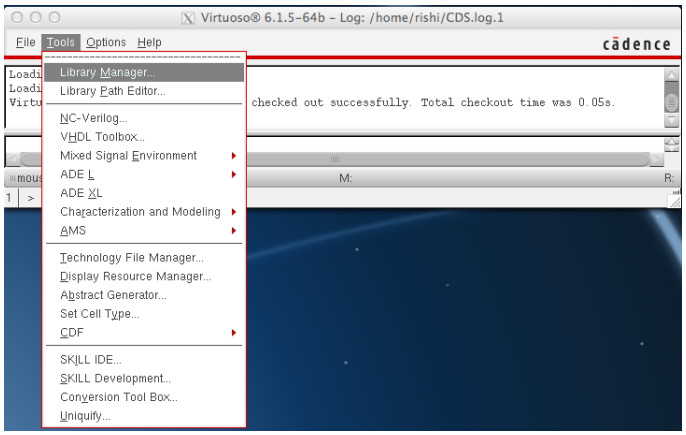


Figure 2: Launch Instructions for Library Manager

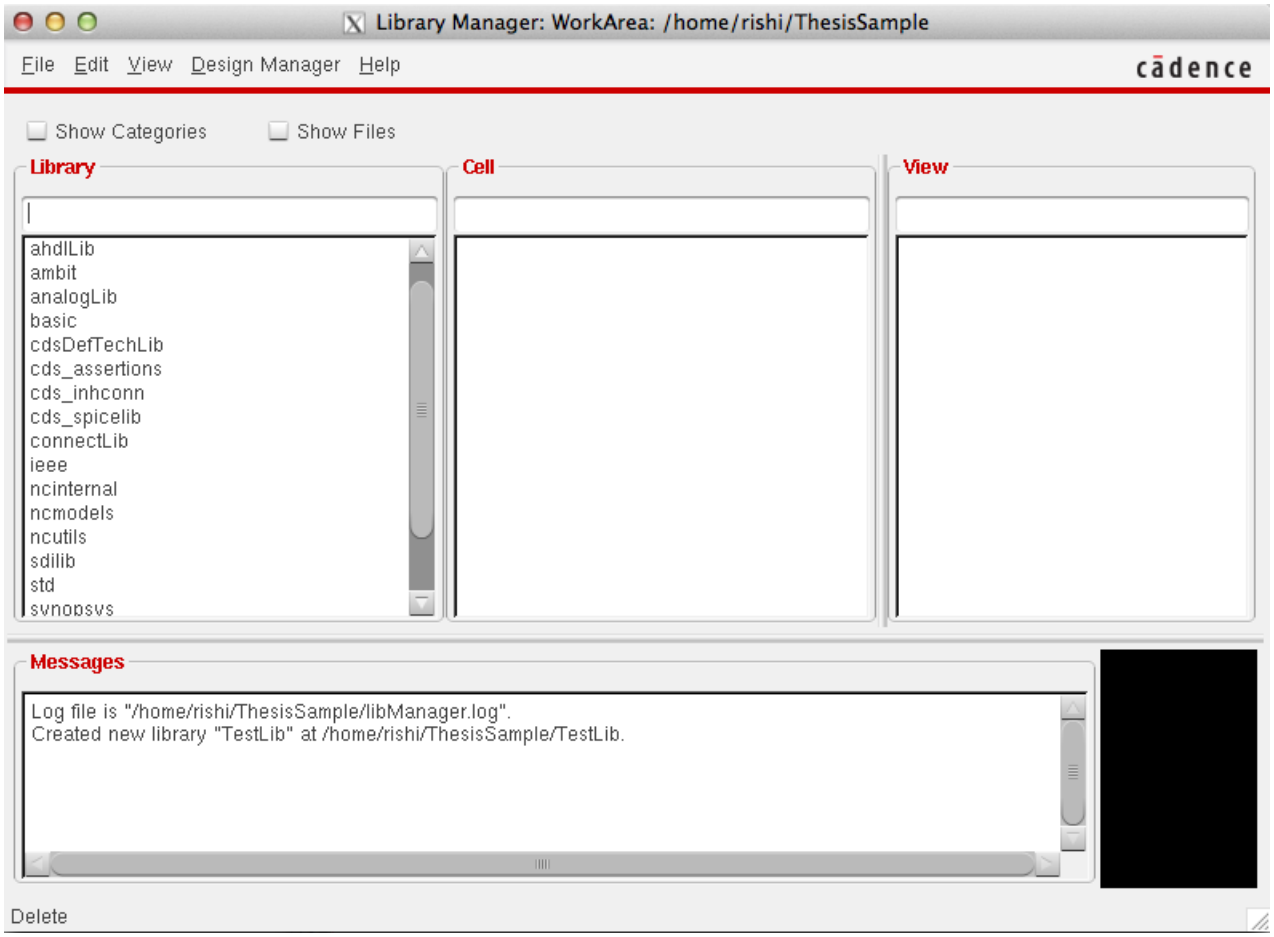
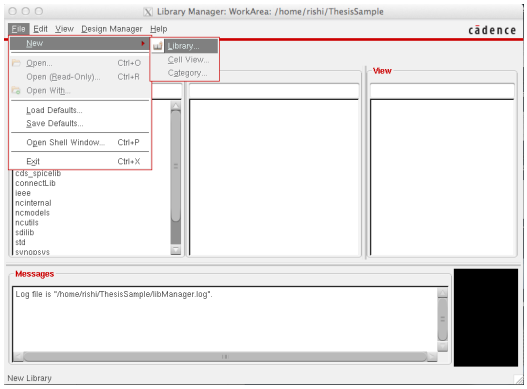
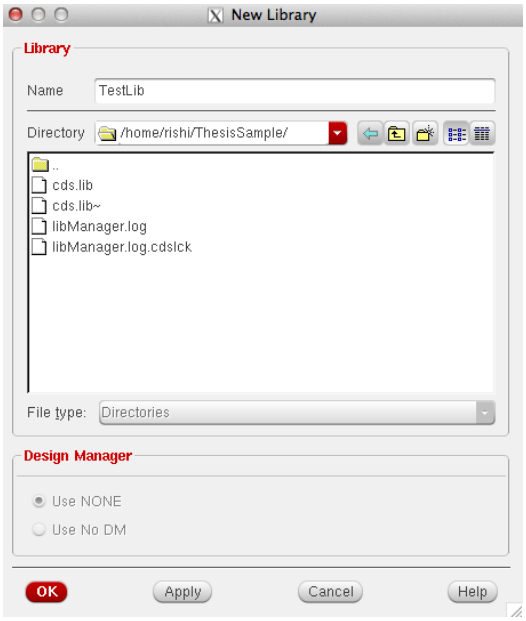


Figure 3: Library Manager Window

2. To create a new library click on *File* → *New* → *Library* and name the library as *TestLib* as highlighted in Figure 4. After creating the new library you need to specify the Technology File to be used in your respective PDK. In our case we will 'Attach an existing technology library', specifically the 'NCSU_TechLib_tsmc02d' which corresponds to 180nm CMOS process. Figure 5 shows the steps involved in attaching the appropriate technology file to a new library.

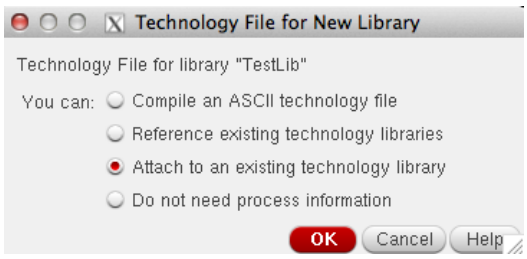


(a) Create New Library

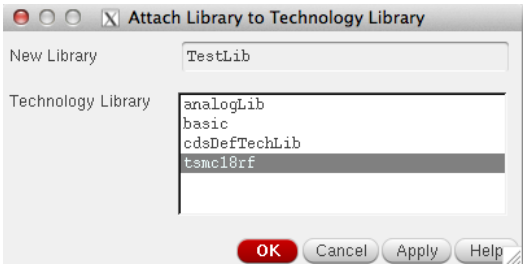


(b) New Library Name

Figure 4: Steps to Create New Library



(a)



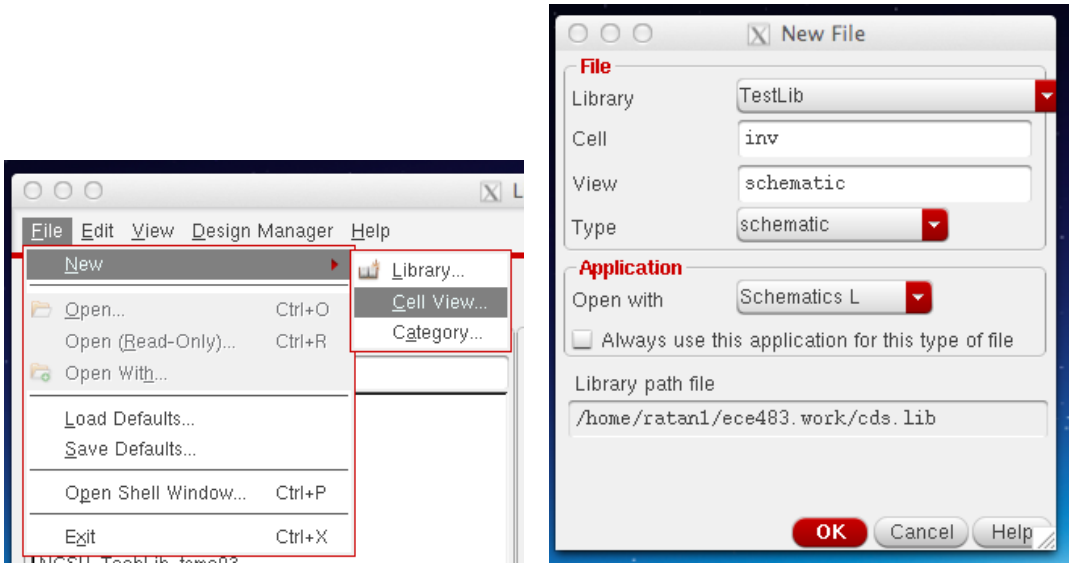
(b)

Figure 5: Attaching Tech File

3.2 Creating a New Library

1. To create a new schematic click on on the library you created above, i.e. click on 'TestLib' which will then be highlighter. Now within the Library Manager window click on *File* → *New* → *Cell View* and call the new schematic *inv* as highlighted in Figure 6. In this tutorial we will use a CMOS Inverter as an example circuit to explore the steps involved in basic circuit simulation using Cadence ADE (Analog Design Environment).

2. Once you have created your new schematic cellview a 'Virtuoso Schematic Editor' window will open up as shown in Figure 7.



(a) Create Schematic (b) New Schematic Name

Figure 6: Steps to Create New Schematic

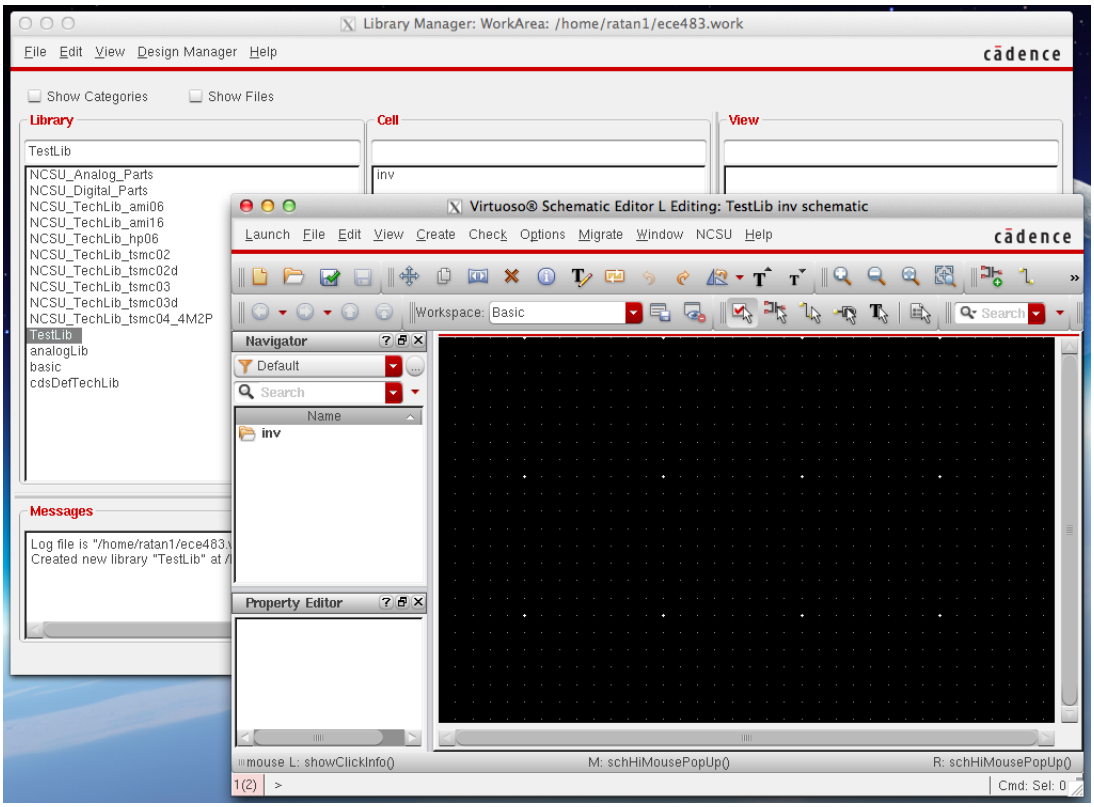


Figure 7: Schematic Window

3. In order to create a circuit in the schematic editor we need to add 'instances' or circuit-components like transistors, supply nets and wires. In the case of an inverter we need one NMOS and one PMOS transistor, thus to add an instance press **I** from your keyboard. This will open up a 'Component Browser' as shown in Figure 8. Choose the 'NCSU_Analog_Parts' library and check-off the 'Flatten' icon by clickin on the grey box next to it. This will list all the components housed within the 'NCSU_Analog_Parts' library and gives you the ability to search for a specific component from the 'Filter'. Search for 'nmos4' and follow the steps outline in Figure 9.

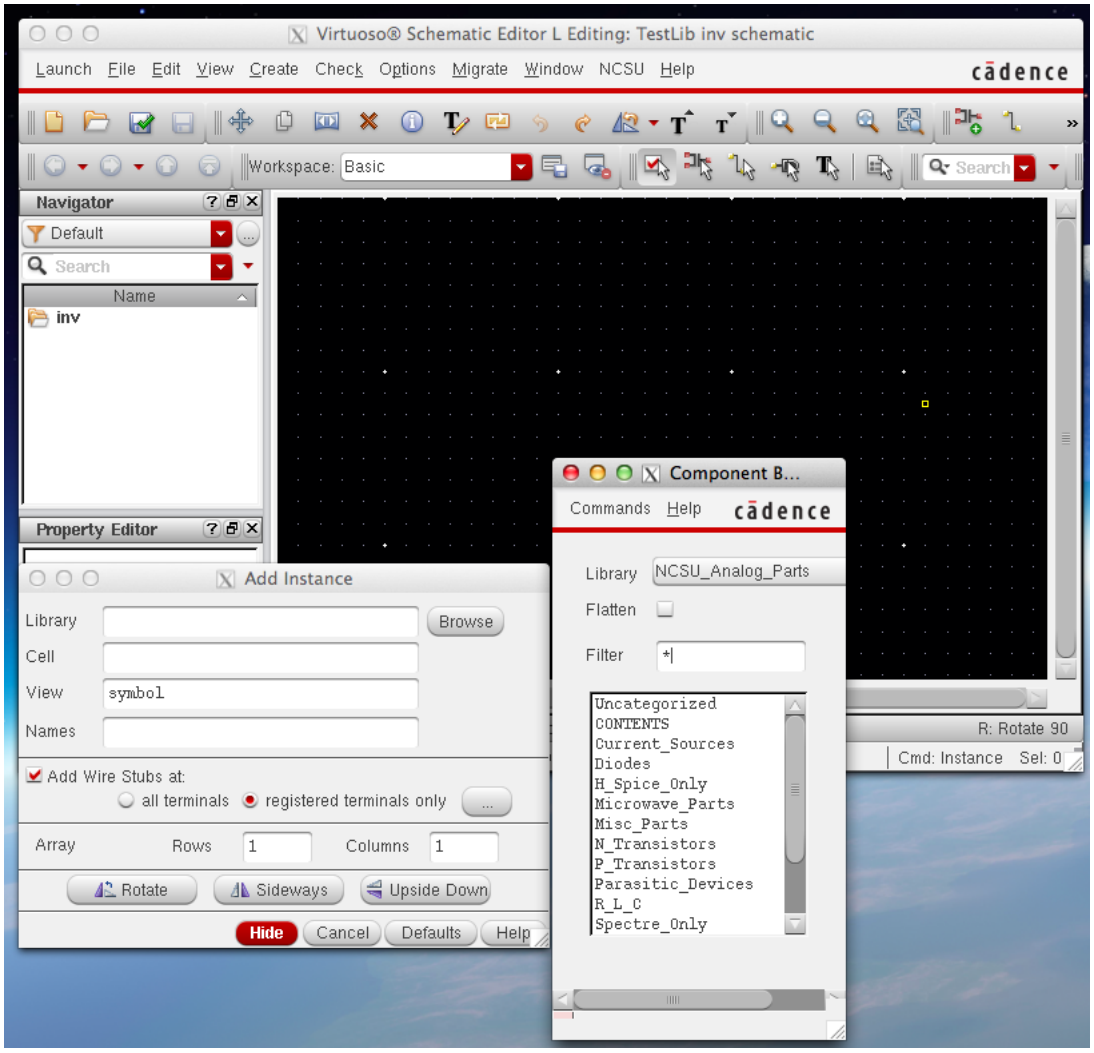
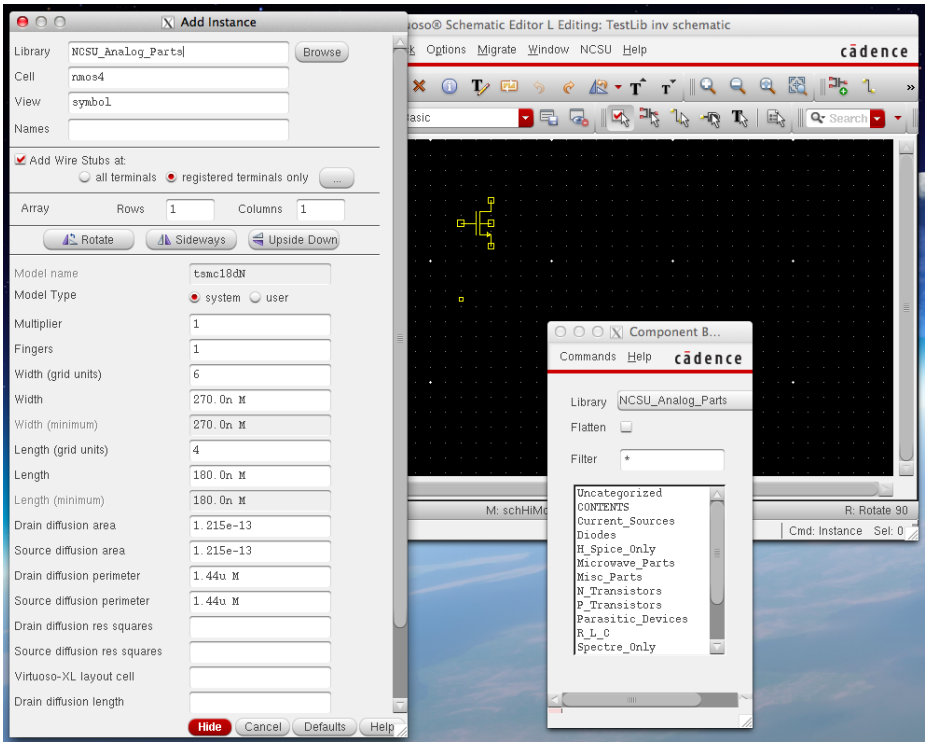
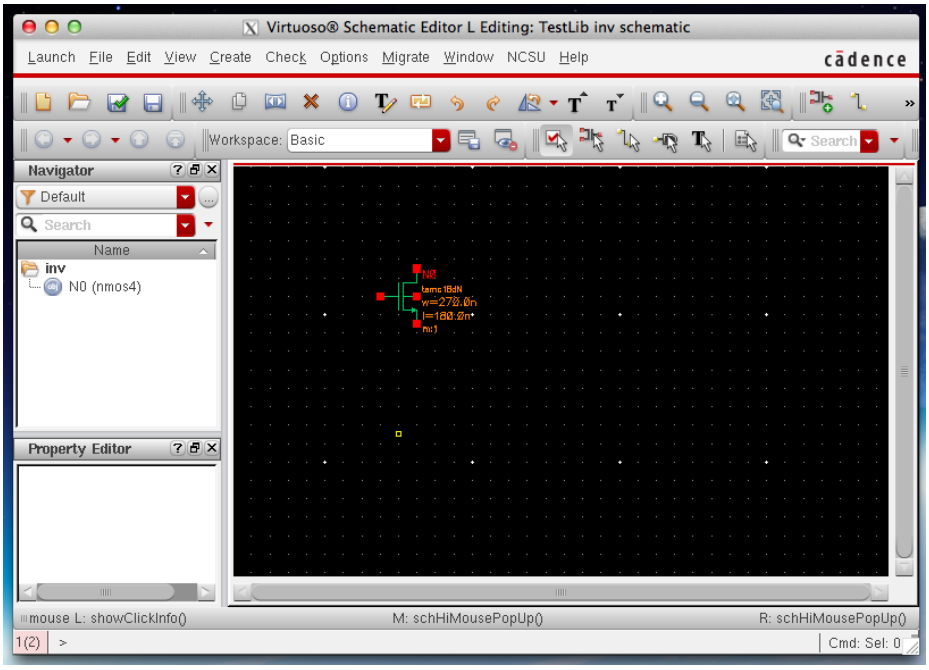


Figure 8: Adding an Instance on Schematic



(a)



(b)

Figure 9: Inserting NMOS Transistor on Schematic

4. Similarly, following the same steps as (2) add a PMOS transistor to your schematic by choosing the 'pmos4' transistor from the 'NCSU_Analog_Parts' library. Your schematic should now look like Figure 10.

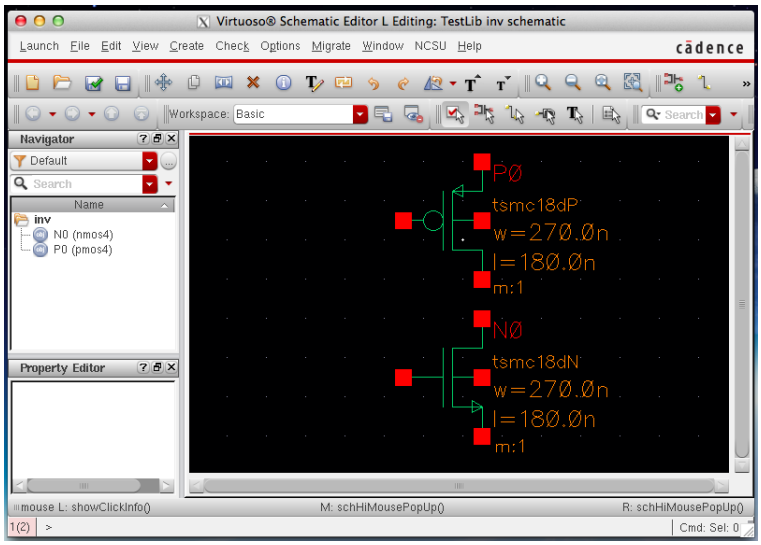
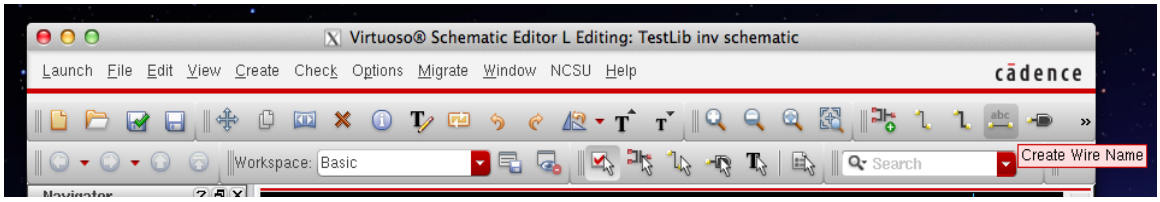
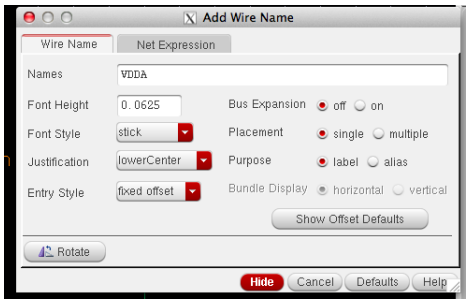


Figure 10: PMOS Transistor

5. In order to add wires to your schematic press **W** from your keyboard and make appropriate connections across all transistor elements. Figure 11 demonstrates the steps involved in labeling wires with a circuit schematic. This will come in very handy during simulation, especially when dealing with circuits with several components.



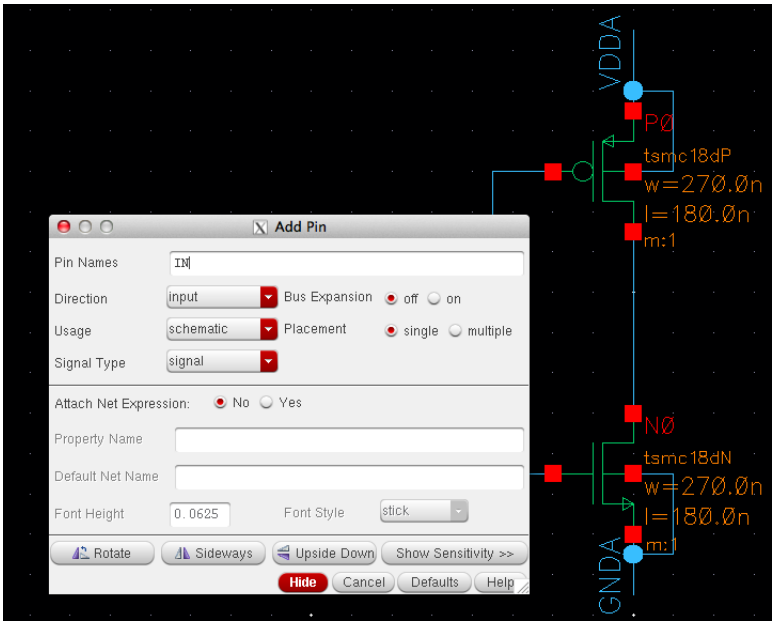
(a)



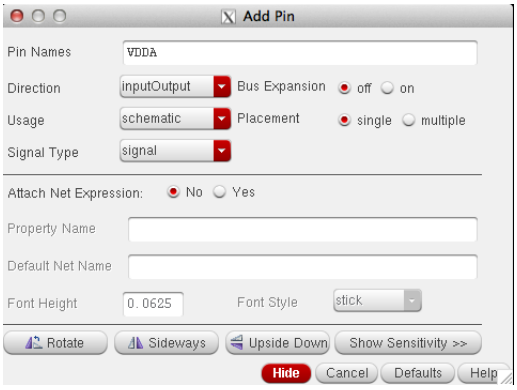
(b)

Figure 11: Inserting Wire Names on Circuit

(a)



(b)



(c)

Figure 12: Creating Pin Names

6. It is often advisable to add 'Pin' names to each of the IO terminals in a circuit. Thus, to add pins to your schematic press **P** from your keyboard or click on the pin symbol as shown in Figure 12 and make appropriate connections across all IO ports. Figure 12 demonstrates the steps involved in labeling wires with a circuit schematic.
   Note: The 'VDDA' and 'GNDA' pins should be chosen to be 'InputOutput' when selecting the 'Direction' during pin creation.

7. Finally your schematic should look like Figure 13. Now click on 'Check and Save' icon (as shown in Figure 14) in the toolbar so that you can move onto the next step of creating a symbol for the inverter schematic.

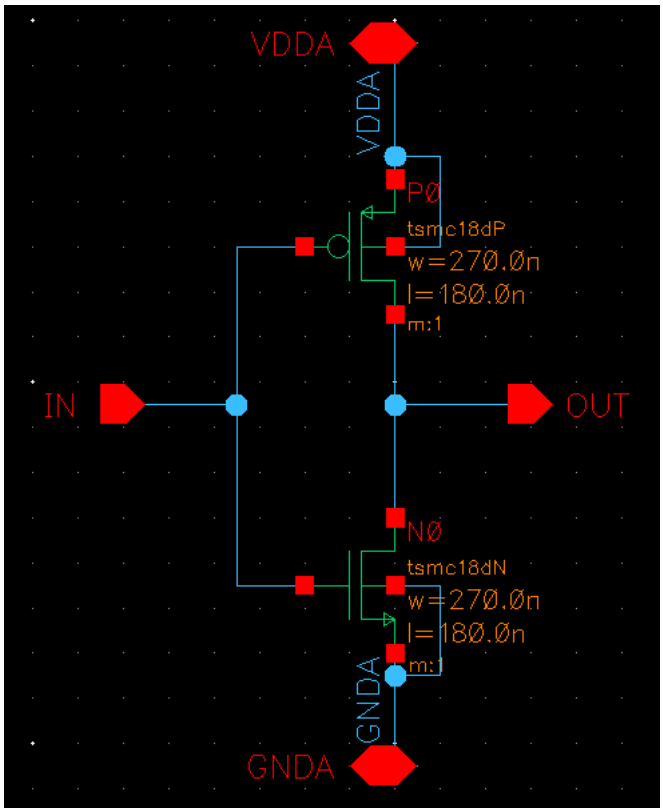


Figure 13: Inverter Schematic

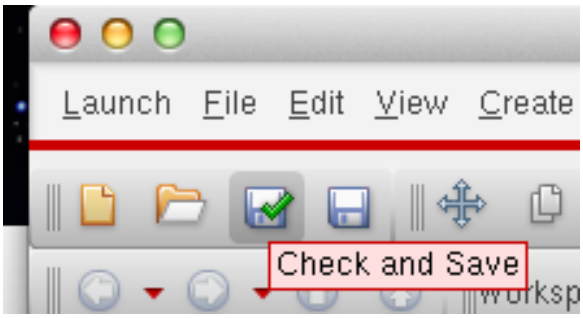
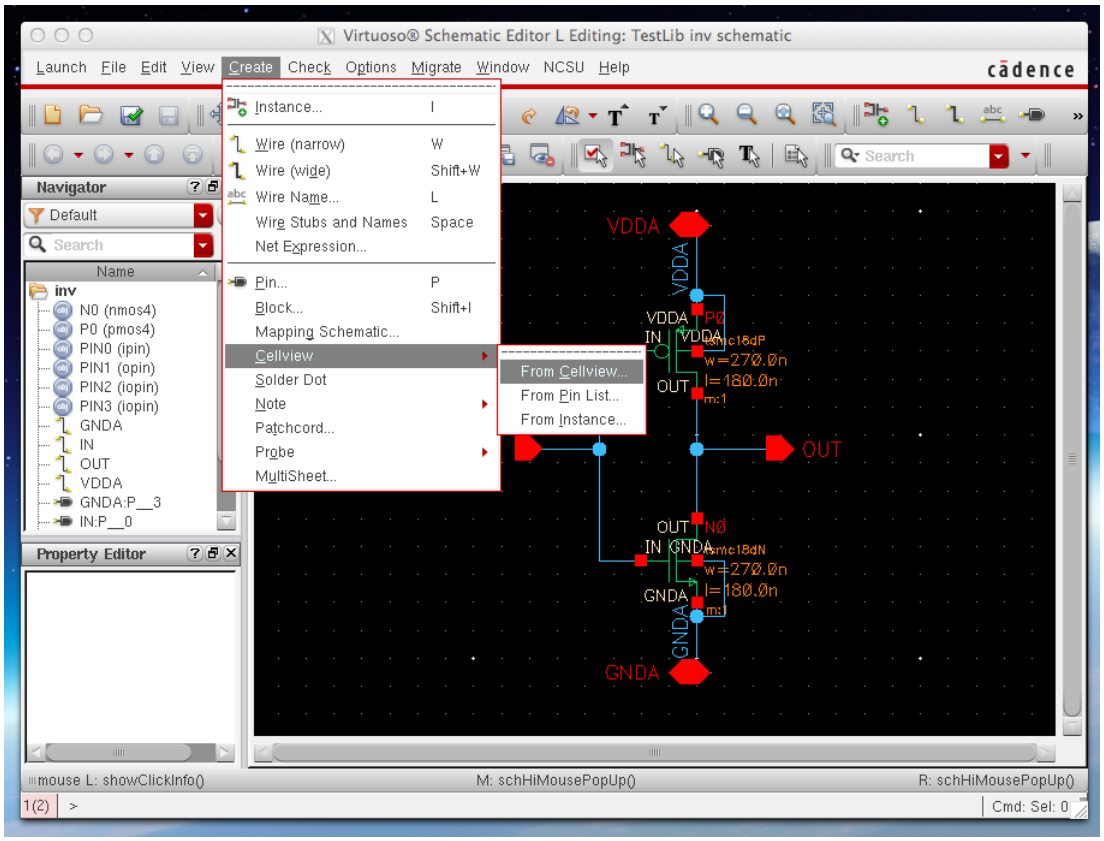


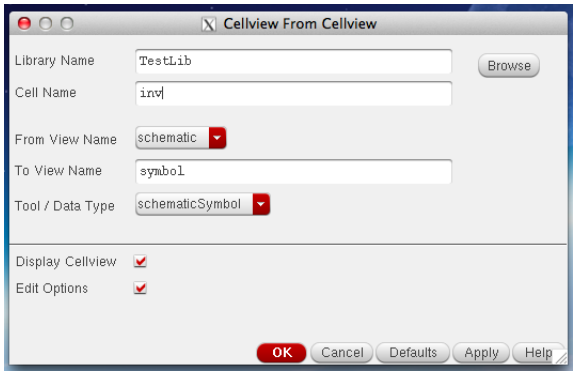
Figure 14: Check and Save

3.3 Creating a Symbol

1. When dealing with large circuits its often advisable to generate symbols for each sub-circuit in the design and perform all simulations by placing the corresponding symbols in a testbench. Figure 15 summarizes the steps involved in generating a symbol from the inverter schematic designed in the previous section.



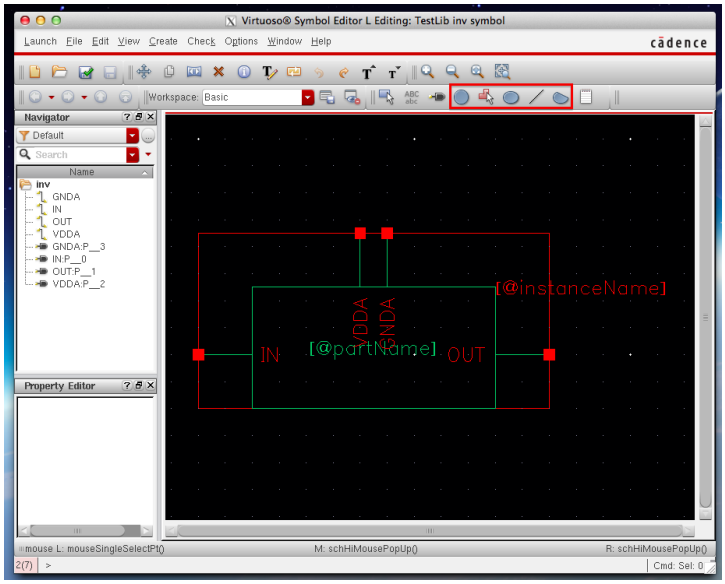
(a)



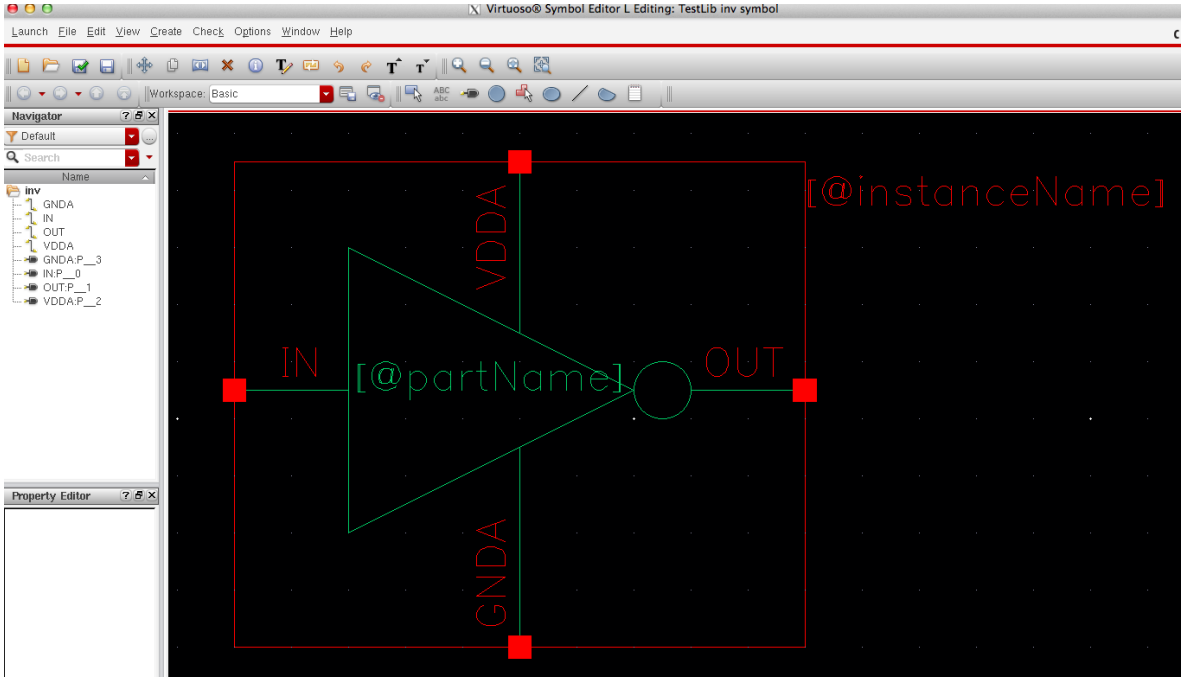
(b)

Figure 15: Generating Symbol from Schematic

2. Once you create the symbol it will pop-up. By default Cadence will generate a rectangular symbol, however you can edit the generated symbol as per your needs. In our case we will edit the symbol shape to make it resemble the traditional inverter symbol used in conventional system design (as shown in Figure 16).



(a)



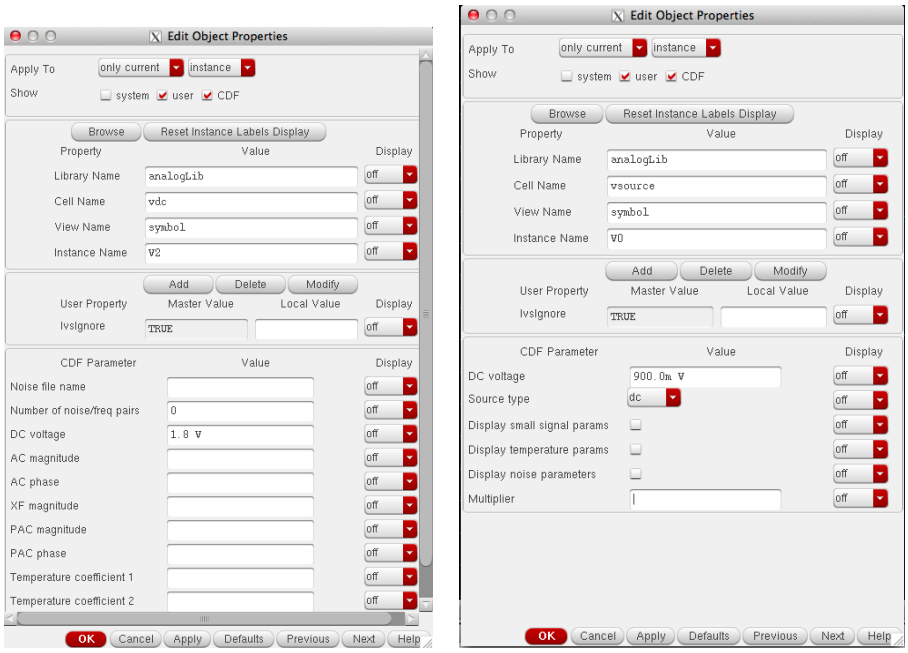
(b)

Figure 16: Designing Schematic Symbol

3.4 Creating a Testbench

Create a new-schematic following the steps outlined earlier in Section 3.1 and name it 'Tb_inv'. This will be the testbench schematic from which we will run all our simulations. Insert 'vdc', 'gnd' and 'vsource' from the Component Library by navigating to the 'Analog Parts' library. Figure 17 shows

the initial conditions to be set for the voltage sources and Figure 18 shows what your testbench schematic should look like at the end of this step.



(a) (b)

Figure 17: Inserting Sources in Testbench

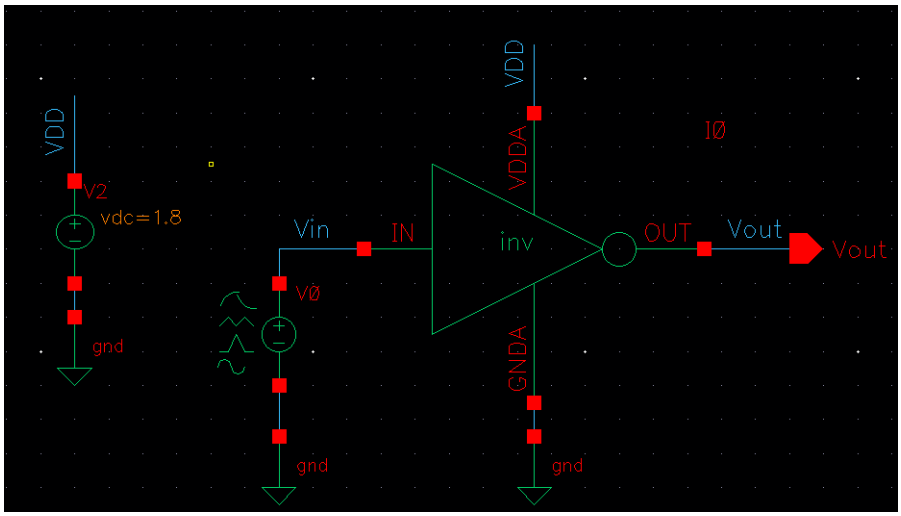


Figure 18: Designing the Testbench

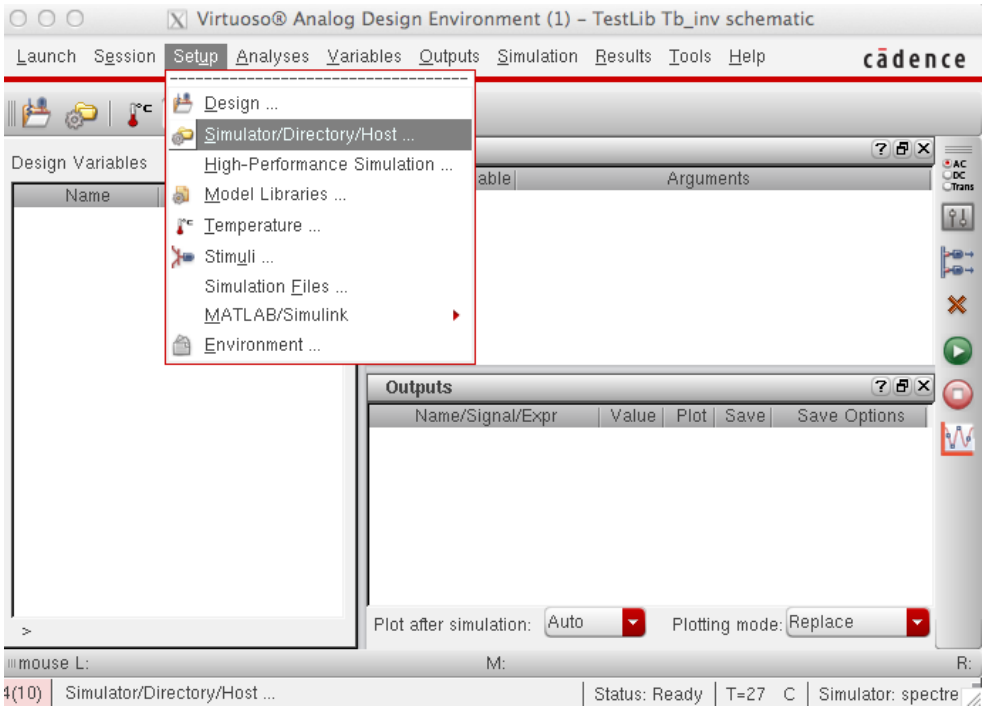
4 Circuit Simulation Using Spectre

4.1 Launching ADE

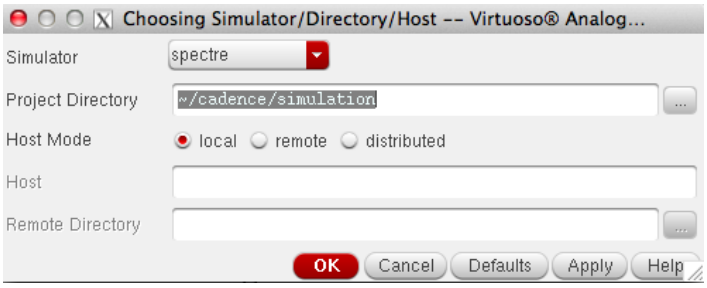
1. We will simulate our circuits using Cadence Spectre Simulation engine. Spectre is a variant of HSPICE developed by Cadence and provides greater accuracy, speed and flexibility especially when dealing with mixed signal circuits thus we will use it as our preferred simulation engine in this course as well.

2. Make sure you first 'Check and Save' your testbench schematic and click on *Launch* → *ADE* to open up the ADE window as shown in Figure 19.

3. Click on *Setup* → *Simulator* to make sure the Simulator is set to Spectre as shown in Figure 19.



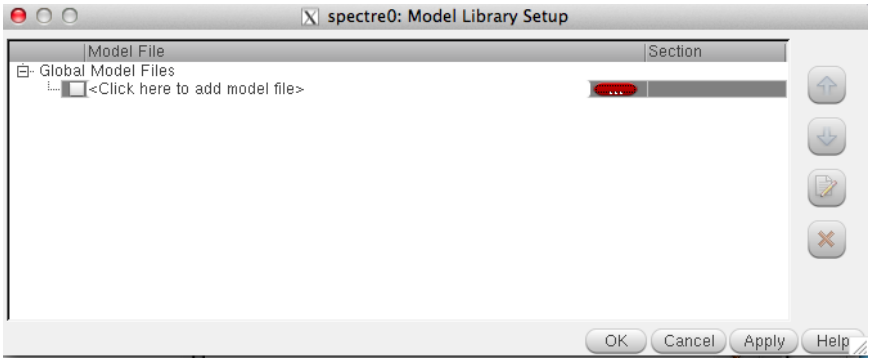
(a)



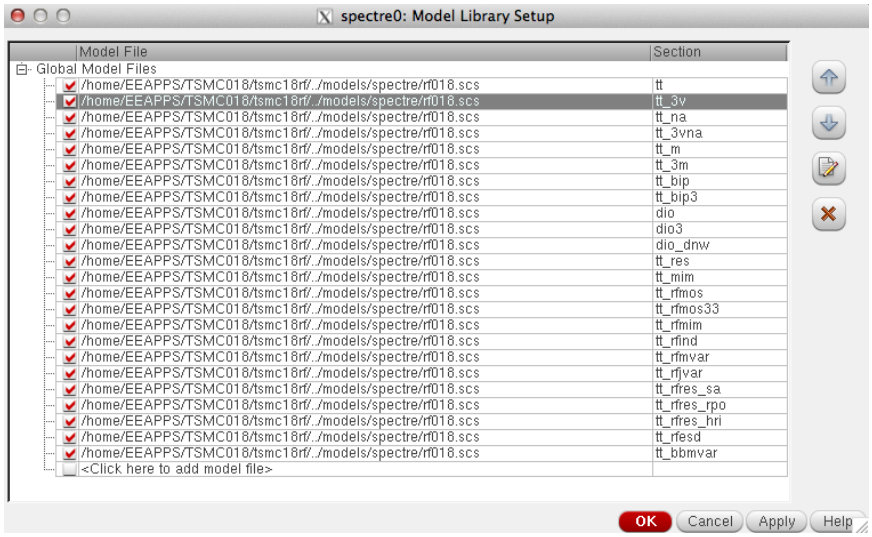
(b)

Figure 19: Simulating Circuit with ADE

4. Now click on *Setup* → *Model Libraries* to configure the Spectre model files. Figure 20 shows the path you need to browse to in order to get the correct model files for the PDK used in this course.



(a)



(b)

Figure 20: Configuring Model Files

4.2 DC Analysis

1. First simulation you will be exposed to is simulation of the DC operating point for the inverter you designed earlier.

2. Click on **AC,DC,Tran** icon on the right pane of the ADE window and a window like Figure 21 should pop open. Choose 'dc' and under 'DC Analysis' save the the DC Operating point. Note: Make sure you keep the Enabled option checked off before you click on 'Ok'.

3. The output window should look like Figure 22 after you simulate the testbench by pressing the green 'Play' button on the right sidebar of ADE.

4. Suppose we want to now view the DC Operating points for the PMOS transistor in the inverter. In order to do so we need to descend into the schematic view from the testbench schematic.

First click on *Results* → *Print* → *DC Operating Points* as shown in Figure 23. Now in order to descend into the actual schematic of the inverter and select the PMOS transistor we start off from the testbench schematic and click *Edit* → *Hierarchy* → *Descend Point* → *Click* on *inverter symbol* → *select PMOS*. The complete steps are outlined in Figures 23, 24 and 25.

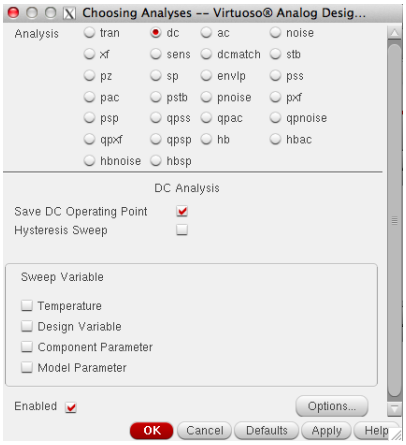


Figure 21: Configuring DC Operating Point

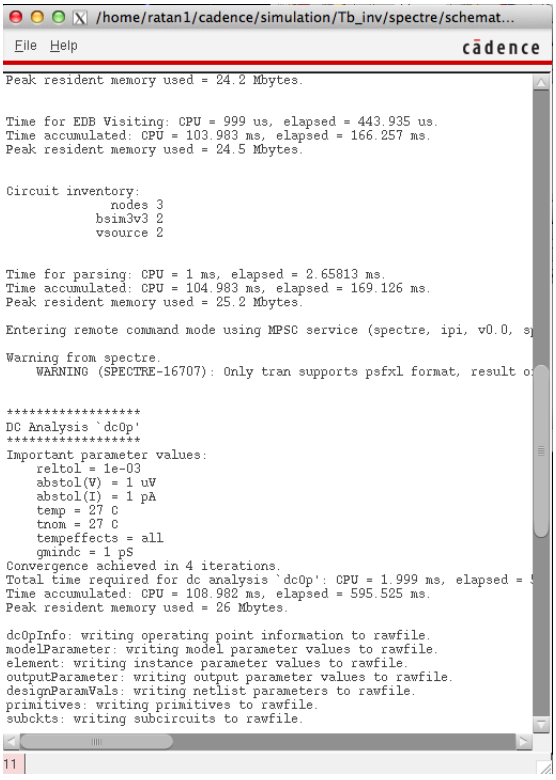


Figure 22: DC Operating Point Netlist Output

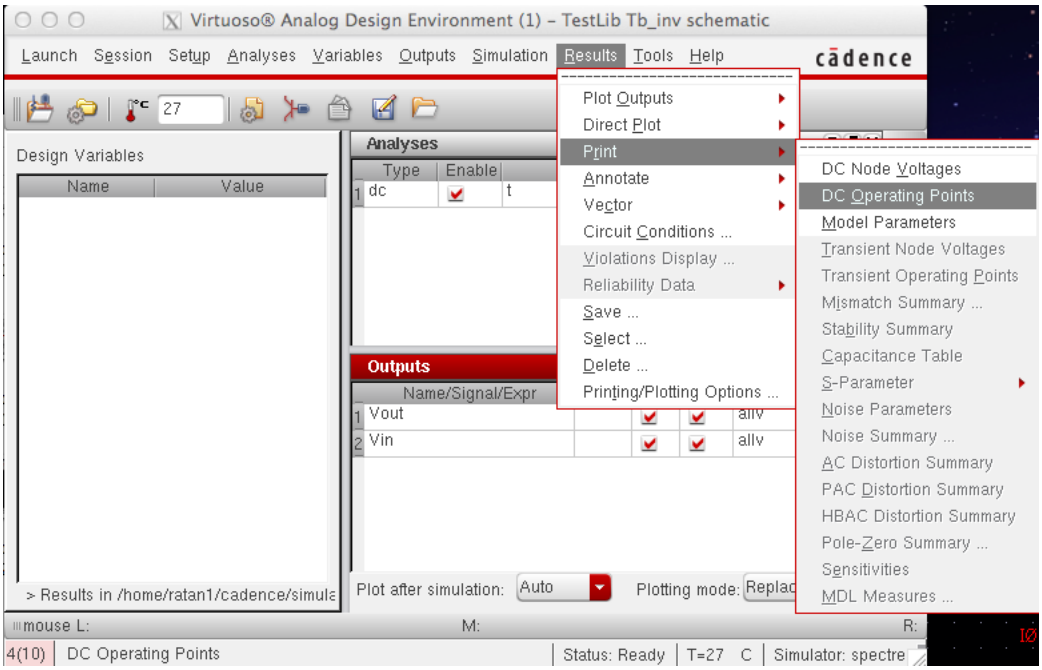


Figure 23: Viewing DC Operating Point from ADE

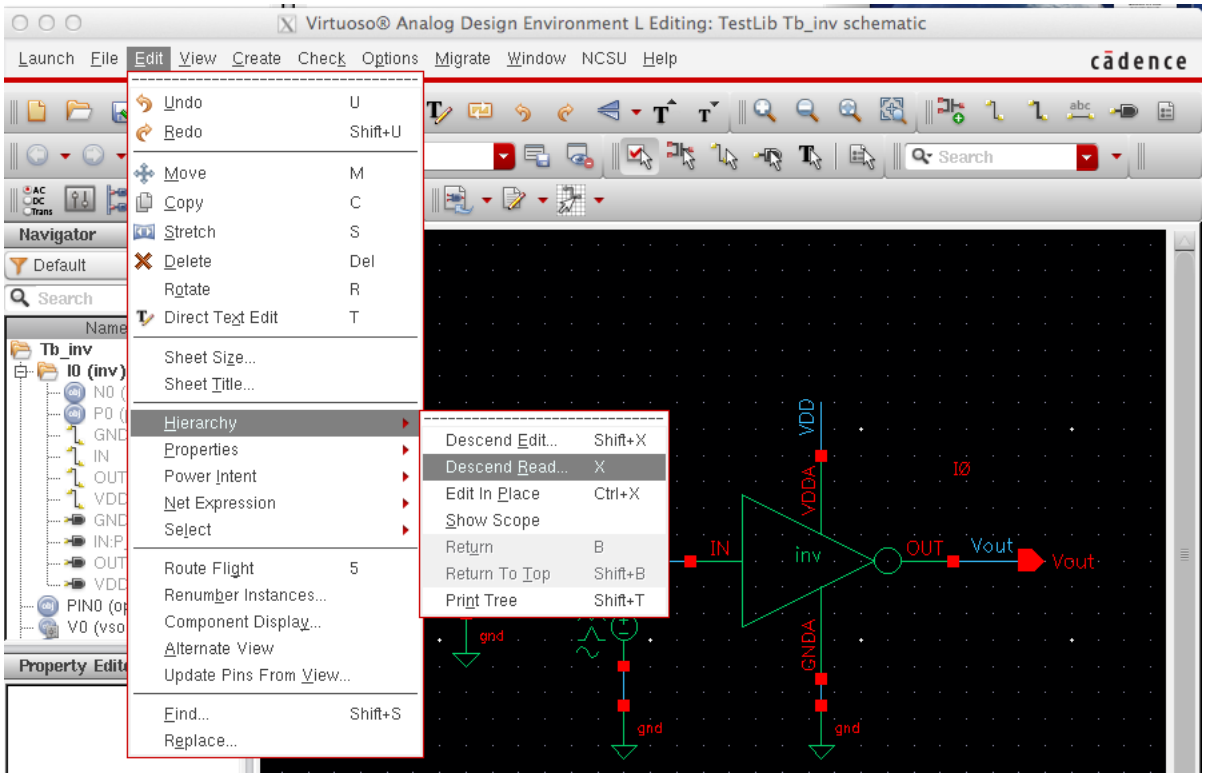
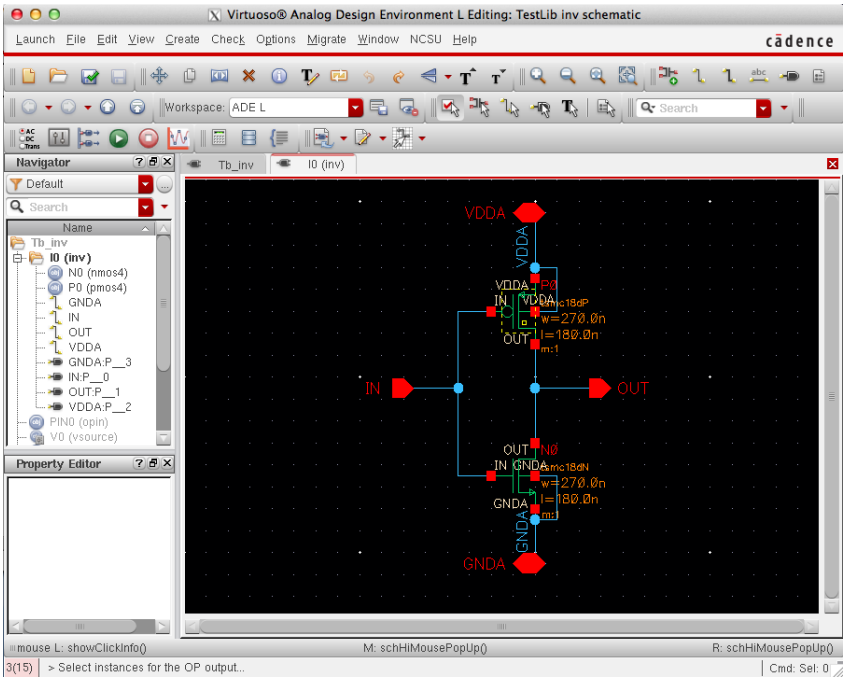
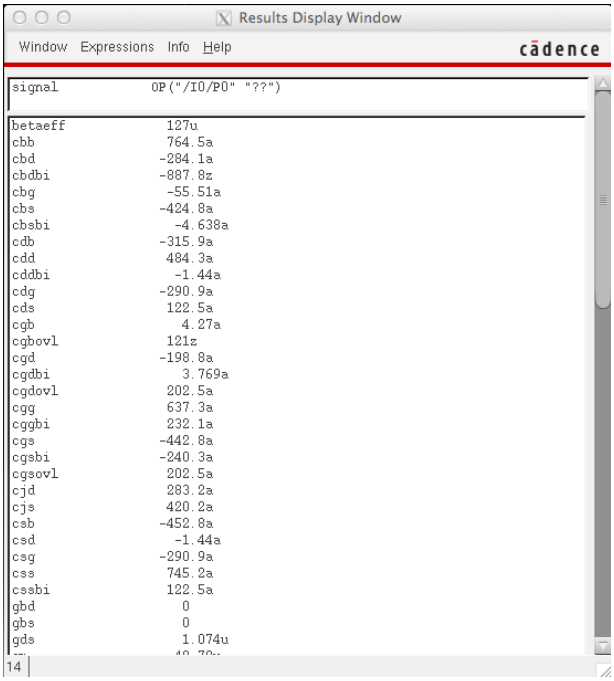


Figure 24: Viewing DC Operating Point from ADE

(a)



(b)



(c)

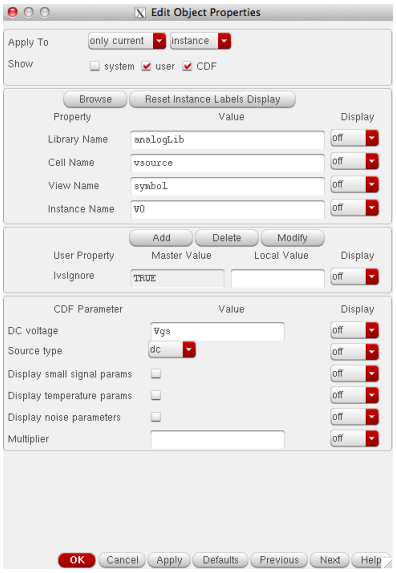
Figure 25: Final DC Operating Point Results

4.3 Parametric Sweep

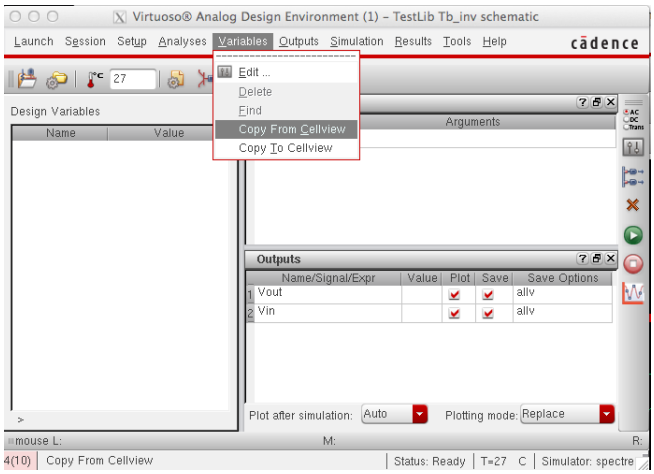
1. Often we want to sweep across a parameter so in this section we will introduce parametric sweep in Cadence ADE by performing a DC parametric sweep across V_{source}.

2. In the testbench schematic click on 'Vsource' and press **Q** to edit its properties. A window like Figure and Figure 26 (a) will pop up. Under the 'DC voltage' option type in 'Vgs' (this will be your sweep parameter). Make sure to click on 'Check and Save' and now in the ADE window click on $Variables \rightarrow Copy\ from\ Cellview$.

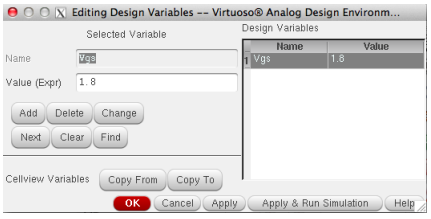
3. Click on the **AC,DC,Tran** icon on the right pane of the ADE window and follow the steps outlined in Figure 26. Under the same DC analysis window scroll down and follow the steps in Figure 27.



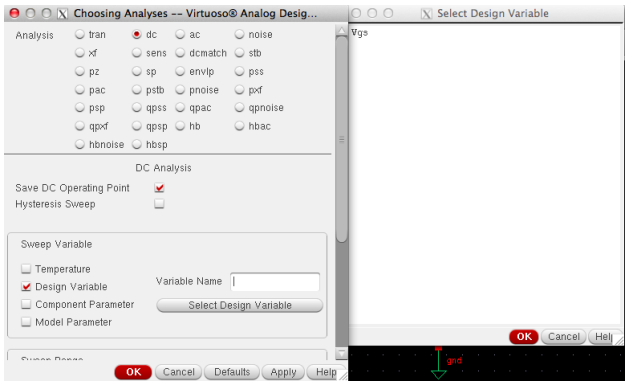
(a) Sweep Vsource



(b) Extract Sweep Parameter from Schematic



(c) Specify Sweep Parameter DC value



(d) Perform DC Sweep

Figure 26: DC Parametric Sweep of Vgs

4. Finally, click on $Tools \rightarrow Parametric\ Analysis$ (as shown in Figure 28)and a window like Figure 29 (a) will pop up. Follow the appropriate entries within this window as shown in

Figure 29 (a) and then proceed to steps outlined in 29 (b). Your final output for g_m *vs.* V_{gs} for the NMOS transistor in the inverter will look like Figure 29 (c).

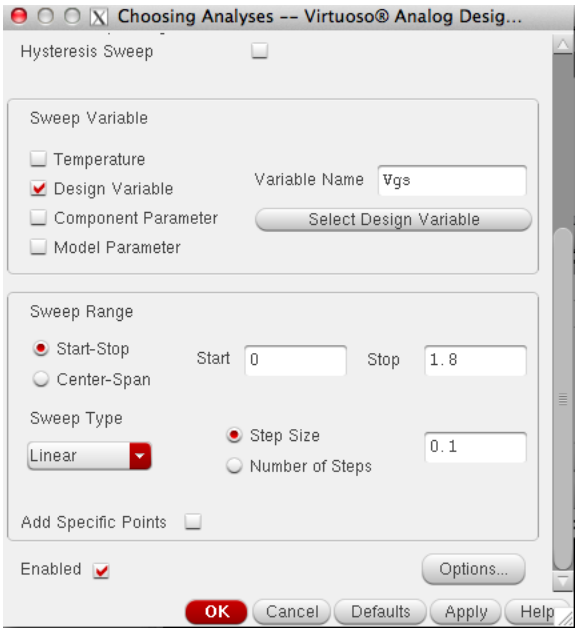


Figure 27: DC Analysis Sweep Plan

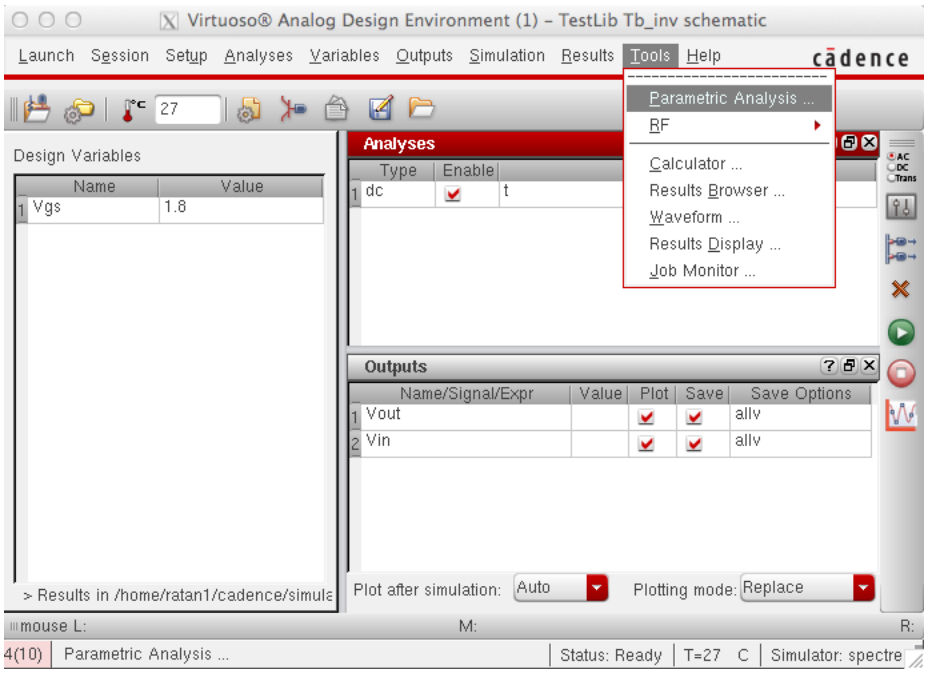
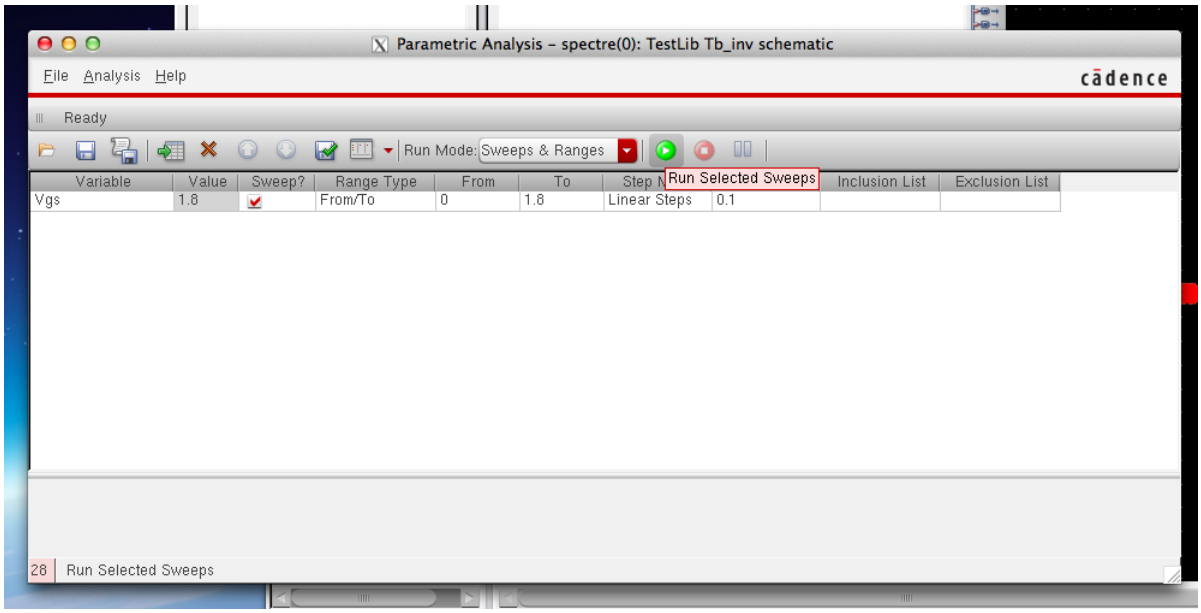
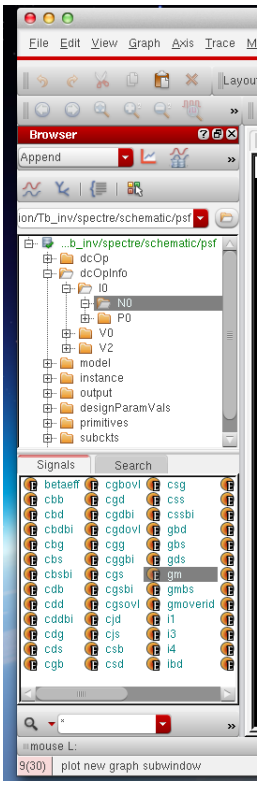


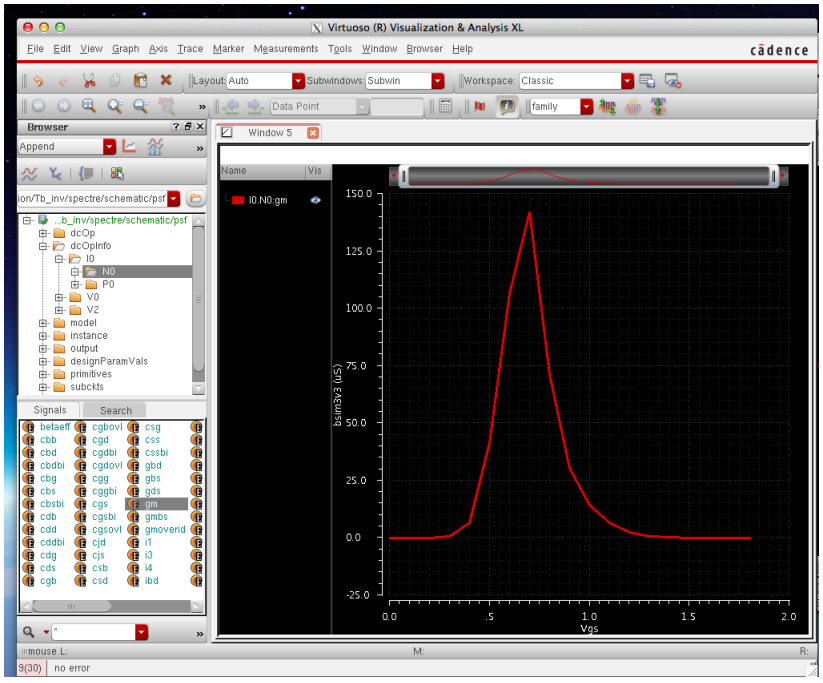
Figure 28: Parametric Analysis on Vgs



(a) Setting Parametric Analysis Plan



(b) Sweeping g_m across Vgs



(c) g_m v/s Vgs Output for NMOS Transistor

Figure 29: Parametric Analysis on Transistor Parameters

4.4 Transient Analysis

1. Transient analysis of any circuit is key to study the time domain behavior. In this section you will simulate the transient time domain responce of the inverter V_{out}, V_{in} and compute propagation delay using the in-built Calculator in ADE.

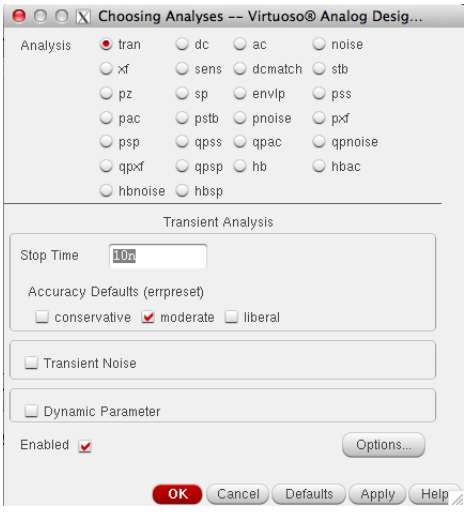
2. First open the testbench schematic and change the Vsource into a 'Pulse' type signal and configure it with the characteristics shown in Figure 30. Make sure you 'Check and Save' the schematic and now in ADE click on the **AC,DC,Tran** icon on the right pane. Choose the 'tran' simuation type, pick the stop time to be 10ns and choose 'moderate' in the 'Accuracy details'.

3. Click on the green 'Play' button to run the simulation and click on *Result* → *Direct Plot* to view the transient simulation plots.

4. In order to calculate the propagation delay of the inverter designed, in the ADE window click on *Tools* → *Calculator* and follow the instructions shown in Figure 31.

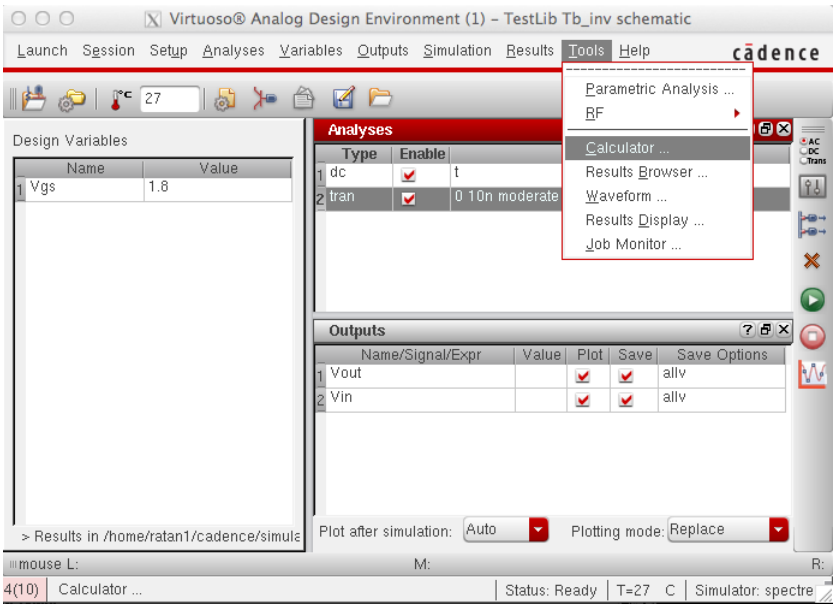
5. Finally, your propagation delay and the final transient simulation plot should look like Figure 32.

(a) Configuring Vsource for Transient Analysis

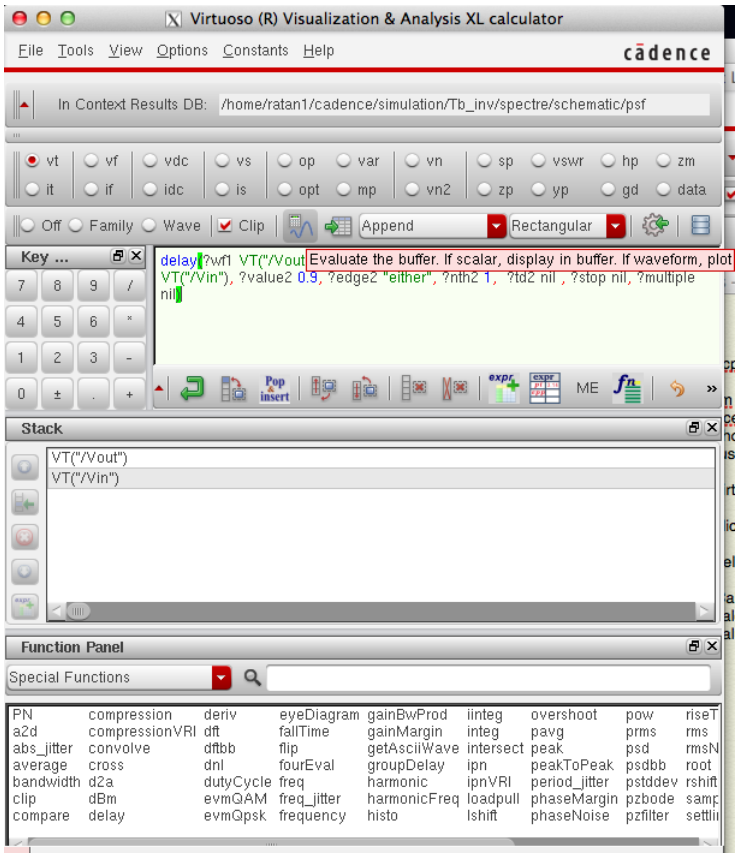


(b) Transient Simulation Configuration

Figure 30: Transient Simulation Setup

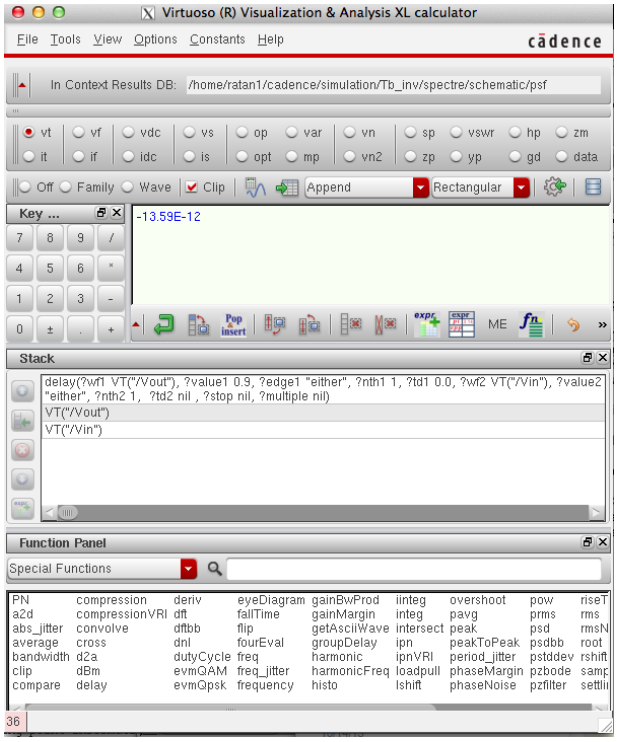


(a)

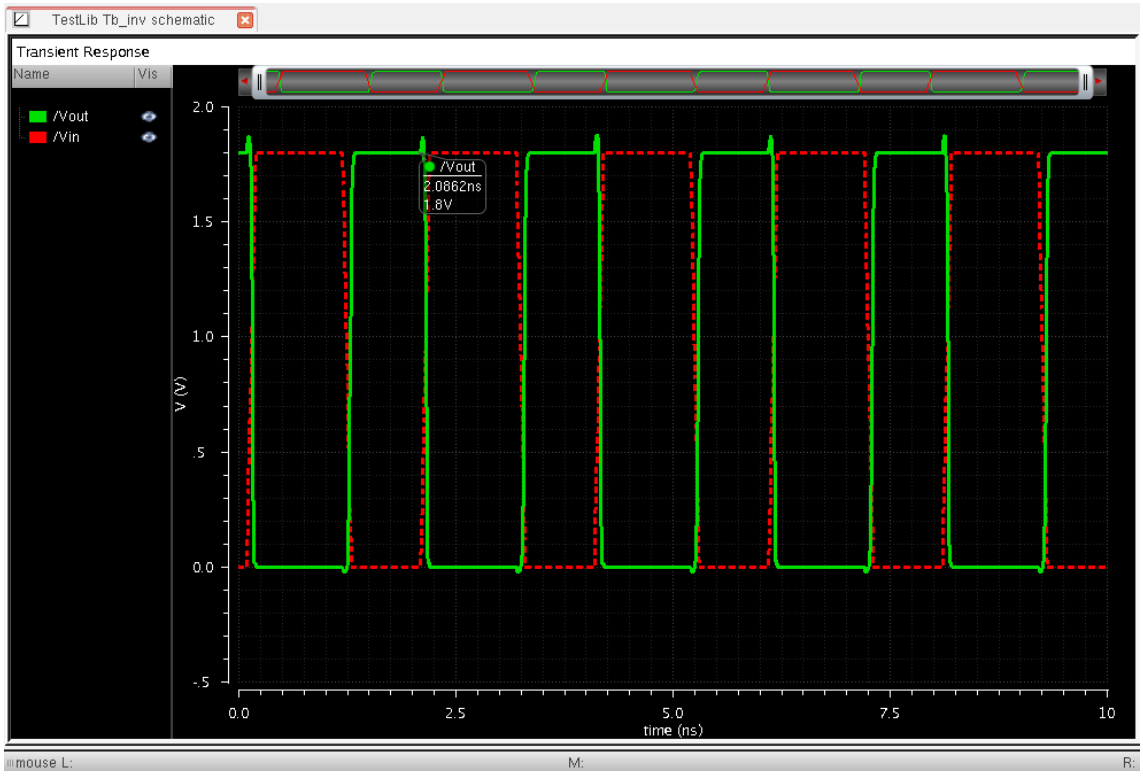


(b)

Figure 31: Propagation Delay Calculation



(a) Propagation Delay from Calculator



(b) Transient Analysis Output Plot

Figure 32: Propagation Delay and Transient Analysis Output