Cadence Virtuoso IC 6.16 Schematic Capture Tutorial

ECE 546 - Advanced Signal Integrity

Contents

1	Introduction	2
2	Environment Setup	2
3	Schematic Capture	3
	3.1 Creating a New Schematic	3
	3.2 Creating a New Library	5
	3.3 Creating a Symbol	11
	3.4 Creating a Testbench	14
4	Circuit Simulation Using Spectre	15
	4.1 Launching ADE	15
	4.2 DC Analysis	16
	4.3 Parametric Sweep	20
	4.4 Transient Analysis	23

1 Introduction

The motivation for this manual is to provide a step-by-step tutorial to design and simulate circuits using Cadence IC 6.16 Virtuoso Design Environment. In this short-tutorial students are exposed to the steps involved in remotely connecting to the EWS servers and launch the Virtuoso simulator engine from the terminal window followed by a detailed guide to create their own custom circuits and simulate them using the Cadence Spectre circuit simulator.

Cadence is an Electronic Design Automation (EDA) environment that integrates various circuit design and verifications applications and tools (both in-house proprietary as well as external third party vendor tools) in a single framework allowing unified IC design and verification in a single environment. The tools are generic and allow the designer to configure the environment depending on the fabrication technology of choice by installing the appropriate PDK (Process-Design Kit).

This tutorial document is not intended to be a one-stop reference for all the features available in Cadence Virtuoso Design Environment. Instead, it's only meant to be a quick-start guide for circuit designers to be able to use the EDA tool to effectively simulate their designs for quick prototyping and verification of their designs.

2 Environment Setup

In order to remotely login to the EWS Linux Servers follow the instructions provided below:

- 1. Windows OS Users:
 - (a) Install PuTTy[www.chiark.greenend.org.uk/~sgtatham/putty/download.html], or another such SSH client MobaXterm[http://mobaxterm.mobatek.net/download-home-edition. html] depending on your preference.
 - (b) Install Xming X Server [http://sourceforge.net/projects/xming/] for Windows to allow X-forwarding during the SSH session. Also, install Xming-fonts from [http: //sourceforge.net/projects/xming/files/Xming-fonts/] <u>Note:</u> Without installing Xming you will not be able to open Virtuoso or for that matter any application with a GUI.
 - (c) Launch your SSH client, type ssh -X yourNetId@remlnx.ews.illinois.edu, hit 'Enter'. You will be prompted to type in a password so type in your 'AD Password' and again hit 'Enter'. Now you can follow the steps outlined in Figure 1.
- 2. Mac OSX Users:
 - (a) Install XQuartz 2.7.5 for Mac OSX if you are using OSX Mountain Lion or later. If you have an older OS then you will already have X11 pre-installed in your system. Check your 'System Preferences' to check whether X11 is turned on. <u>Note:</u> Without installing XQuartz or enabling X11 (depending upon your OSX version) you will not be able to open Virtuoso or for that matter any application with a GUI.
 - (b) Launch your SSH client and type **ssh** -X **yourNetId@remlnx.ews.illinois.edu**, hit 'Enter'. You will be prompted to type in a password so type in your 'AD Password' and again hit 'Enter'. Now you can follow the steps outlined in Figure 1.
- 3. Linux OS Users:
 - (a) Launch **Terminal** and type **ssh** -X **yourNetId@remlnx.ews.illinois.edu**, hit 'Enter'. You will be prompted to type in a password so type in your 'AD Password' and again hit 'Enter'. Now you can follow the steps outlined in Figure 1.

	⊙ ○ 💮 rishiratan — ratan1@linux-v1:~/ece546.work — ssh — 80×24 🖉	
	ratan1@linux-v1:~/ece546.work	
	<pre>wirelessprvnat-172-16-130-30:~ rishiratan\$ ssh -Y ratan1@remInx.ews.illinois.edu ratan1@remInx.ews.illinois.edu's password: Last login: Fri Apr 18 21:03:06 2014 from wirelessprvnat-172-16-130-30.near.illi nois.edu [ratan1@linux-v1 ~]\$ cd ece546.work/ [ratan1@linux-v1 ece546.work]\$ module load cadence/Dec2013 [ratan1@linux-v1 ece546.work]\$ [[ratan1@linux-v1 ece546.work]\$ []</pre>	
00	🔀 Virtuoso® 6.1.6 – Log: /home/ratan1/CDS.log	
<u> </u>	<u>O</u> ptions <u>H</u> elp	cādence
COPYRIGHT @ @	9 1992-2013 CADENCE DESIGN SYSTEMS INC. ALL RIGHTS RESERVED. 9 1992-2013 UNIX SYSTEMS Laboratories INC., Reproduced with permission.	
	ш	
≡mouse L:	M:	R:
1 >		

Figure 1: Launch Instructions for Virtuoso

If connecting directly from the EWS Machines, just directly follow the steps outlined in Figure 1. When prompted by the error message shown in Figure 1 select 'Yes'.

3 Schematic Capture

3.1 Creating a New Schematic

1. To view all the libraries in the current work directory click on $Tools \rightarrow LibraryManager$ as outlined in Figure 2. and the Library Manager window will pop up as shown in Figure 3.

<u>Note:</u> If you want to manually add a library that you copied from an external source into your Cadence work directory you would need to edit the cds.lib file found in your work directory folder by opening it in a text-editor.

00	O X Virtuo	so® 6.1.5-64b - Log: /home/rishi/CDS.log.1
<u>F</u> ile	Tools Options Help	cādence
Loadi Loadi Virtu	Library Manager Library Path Editor <u>NC-Verilog</u>	checked out successfully. Total checkout time was 0.05s.
	Mixed Signal Environment ADE L ADE XL Characterization and Modeling AMS	M: R:
	Iechnology File Manager Display Resource Manager Abstract Generator Set Cell Type CDF	
	SKILL IDE <u>S</u> KILL Development Con <u>v</u> ersion Tool Box <u>U</u> niquify	

Figure 2: Launch Instructions for Library Manager

● ○ ○ X Library	Manager: WorkArea: /home/rishi/ThesisSa	mple
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
 Show Categories Show Files Library AhdlLib ambit analogLib basic cdsDefTechLib cds_assertions cds_inhconn cds_spicelib connectLib ieee ncinternal ncmodels ncutils sdilib std svnopsvs 	Cell	
Messages Log file is "/home/rishi/ThesisSample/libManage Created new library "TestLib" at /home/rishi/The	er.log". esisSample/TestLib.	
Delete		

Figure 3: Library Manager Window

2. To create a new library click on $File \rightarrow New \rightarrow Library$ and name the library as TestLib as highlighted in Figure 4. After creating the new library you need to specify the Technology File to be used in your respective PDK. In our case we will 'Attach an existing technology library', specifically the 'NCSU_TechLib_tsmc02d' which corresponds to 180nm CMOS process. Figure 5 shows the steps involved in attaching the appropriate technology file to a new library.

	😑 🔿 💫 📉 New Library
	Library
	Name TestLib Directory @ /home/rishi/ThesisSample/
○ ○ ○ 🔨 Library Manager: WorkArea: /home/rishi/ThesisSample	cds.lib cds.lib libManager.log libManager.log
Bits Upwn cådence Bind ut utery utery Bind Ctro Cill View utery Open Riss-Only) Ctri View Category utery Load Derollints Open Riss Utery utery Synthe Derollints Open Riss Utery utery Synthe Derollints Utery Utery Utery Synthe Derollints Utery Utery Utery	
Connect b eve eve eve eve eve eve eve e	Design Manager
Messages	Use NONE
Log file is "homohohuThesisSample/IbMenager.log".	Use No DM
New Library	Cancer (Telp)
(a) Create New Library	(b) New Library Name

Figure 4: Steps to Create New Library



Figure 5: Attaching Tech File

3.2 Creating a New Library

- 1. To create a new schematic click on on the library you created above, i.e. click on 'TestLib' which will then be highlighter. Now within the Library Manager window click on $File \rightarrow New \rightarrow Cell \ View$ and call the new schematic *inv* as highlighted in Figure 6. In this tutorial we will use a CMOS Inverter as an example circuit to explore the steps involved in basic circuit simulation using Cadence ADE (Analog Design Environment).
- 2. Once you have created your new schematic cellview a 'Virtuoso Schematic Editor' window will open up as shown in Figure 7.

	000	X New File
	File	
	Library	TestLib
	Cell	inv
000	X L View	schematic
<u>Eile E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp	Туре	schematic 🔽
New 🕨 🖬 Library	Application	
🗁 Open Ctrl+O Cell View	Open with	Schematics L
Open (<u>R</u> ead-Only) Ctrl+R C <u>a</u> tegory	🗌 🔲 Always u	se this application for this type of file
😂 Open Wit <u>h</u>	Library path	file
Load Defaults	/home/rata	n1/ece483.work/cds.lib
<u>S</u> ave Defaults		
Ogen Shell Window Ctrl+P		
E <u>x</u> it Ctrl+X		OK Cancel Help
(a) Create Schematic		(b) New Schematic Name

Figure 6: Steps to Create New Schematic

000	🔀 Library Ma	anager: WorkArea: /home/ratan1/ece483.work	
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> esign Manage	r <u>H</u> elp		cādence
Show Categories Show Library TestLib NCSU_Analog_Parts NCSU_TechLib_ami06 NCSU_TechLib_ami16	elles	X Virtuoso® Schematic Editor L Editing: TestLib inv schematic	
NCSU_TechLib_thpu6 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d			
NCSU_TechLib_tsmc04_4M2P TestLib analogLib basic cdsDefTechLib	Navigator ? ? X Y Default Q Search		
Messages	P inv	· · · · · · · · · · · · · · · · · · ·	
Log file is "/home/ratan1/ece483. Created new library "TestLib" at /	Property Editor ? 5 ×		
		Mi sahliMausaBanlinA	P: cohHittouroBorUnA
	1(2) >	M: scnHimousePopup()	K: schHilviousePopUp()

Figure 7: Schematic Window

3. In order to create a circuit in the schematic editor we need to add 'instances' or circuitcomponents like transistors, supply nets and wires. In the case of an inverter we need one NMOS and one PMOS transistor, thus to add an instance press I from your keyboard. This will open up a 'Component Browser' as shown in Figure 8. Choose the 'NCSU_Analog_Parts' library and check-off the 'Flatten' icon by clickin on the grey box next to it. This will list all the components housed within the 'NCSU_Analog_Parts' library and gives you the ability to search for a specific component from the 'Filter'. Search for 'nmos4' and follow the steps outline in Figure 9.



Figure 8: Adding an Instance on Schematic



(b)

Figure 9: Inserting NMOS Transistor on Schematic

8

4. Similarly, following the same steps as (2) add a PMOS transistor to your schematic by choosing the 'pmos4' transistor from the 'NCSU_Analog_Parts' library. Your schematic should now look like Figure 10.



Figure 10: PMOS Transistor

5. In order to add wires to your schematic press \mathbf{W} from your keyboard and make appropriate connections across all transistor elements. Figure 11 demonstrates the steps involved in labeling wires with a circuit schematic. This will come in very handy during simulation, especially when dealing with circuits with several components.



Figure 11: Inserting Wire Names on Circuit

9

	-	1 - 1	abc		1			
		• •	• (Create	Din			
	· 5	Bearch	•	- Create	FIL			
			(a)					
						\triangleleft		, i
						DD		
						.> _ _		
						P	0	
						ts w	mc18dP =27Ø.(Øn
00		X Add Pin				i - <u>i</u> i =	=180.0	n
Pin Names	IN				1.1	└ <mark>─</mark> ─		
Direction	input	Bus Exp	pansion 🥑 off (🔾 on				
Usage	schema	tic 🔽 Placem	ent 💿 sing	le 🔾 multiple				
Signal Type	signal	*						
Attach Net B	Expression:	🖲 No 🔾 Yes						
Property Na	ime						ø mc 18dN	
Default Net	Name				- -	. W	= 27Ø.\$	Øn
Font Height	0.0625	5 Font St	yle stick	•		=	= <mark>18Ø.Ø</mark>	n _.
42 Rotati	e 🛛 🕼 Sid	eways) 🔫 Upsid	e Down Show	Sensitivity >>		⊴●‴		
		Hide	Cancel De	faults Help		<u>8</u> .		
			(b)					
	00		X Add Pin					
	Pin Names	VDDA						
	Direction	inputOutput	Bus Expans	sion 🖲 off 🔾	on			
	Usage	schematic	Placement	🖲 single	🔾 multiple			
	Signal Type	signal				_		
	Attach Net Ex	pression: 🔍 No	Q Yes					
	Property Nam	e						
	Default Net Na	ame						
	Font Height	0.0625	Font Style	stick	-	_		
	🛛 🐴 Rotate	Sideways	Upside D	own Show Se	ensitivity >>	\bigcirc		
			Hide		Deraults	Help		
	Font Height	0.0625	Font Style	stick own Show Se Cancel E	ensitivity >> Defaults	Help		
			(c)					

Figure 12: Creating Pin Names

6. It is often advisable to add 'Pin' names to each of the IO terminals in a circuit. Thus, to add pins to your schematic press **P** from your keyboard or click on the pin symbol as shown in Figure 12 and make appropriate connections across all IO ports. Figure 12 demonstrates the steps involved in labeling wires with a circuit schematic.

<u>Note:</u> The 'VDDA' and 'GNDA' pins should be chosen to be 'InputOutput' when selecting the 'Direction' during pin creation.

7. Finally your schematic should look like Figure 13. Now click on 'Check and Save' icon (as shown in Figure 14) in the toolbar so that you can move onto the next step of creating a symbol for the inverter schematic.



Figure 13: Inverter Schematic



Figure 14: Check and Save

3.3 Creating a Symbol

1. When dealing with large circuits its often advisable to generate symbols for each sub-circuit in the design and perform all simulations by placing the corresponding symbols in a testbench. Figure 15 summarizes the steps involved in generating a symbol from the inverter schematic designed in the previous section.

ECE 546

000	🔀 Virtuoso® Schematic Editor L Editing: TestLib inv schematic	
<u>L</u> aunch <u>F</u> ile <u>E</u> dit <u>V</u> iew	<u>Create</u> Check Options <u>Migrate Window</u> NCSU <u>H</u> elp	cādence
। 🗅 🗁 🛃 🗔 । 🝕	D's Instance	abc 🛥 »
Navigator ? 5 Y Default Q Search	Wire (narrow) W Wire (wige) Shift+W Wire Name L Wire Stubs and Names Space Net Expression VDDA	
Name ▲ Inv Ono (nmos4) Ono (pino) PIN0 (pino) PIN1 (opino) PIN1 (opino)	Pin P Block Shift+I Mapping Schematic IN VDDA PC Gellview → From Cellview v=270.00n Solder Dot	
	Outer From Pin List Note From Instance Patchcord From Instance Probe OUT MultiSheet OUT	· · ·
Property Editor		
mouse L: showClickInfo()	M: schHiMousePopUp() R: schHi	MousePopUp()
1(2) >		Cmd: Sel: 0 //

(a)



Figure 15: Generating Symbol from Schematic

2. Once you create the symbol it will pop-up. By default Cadence will generate a rectangular symbol, however you can edit the generated symbol as per your needs. In our case we will edit the symbol shape to make it resemble the traditional inverter symbol used in conventional system design (as shown in Figure 16).







Figure 16: Designing Schematic Symbol

3.4 Creating a Testbench

Create a new-schematic following the steps outlined earlier in Section 3.1 and name it 'Tb_inv'. This will be the testbench schematic from which we will run all our simulations. Insert 'vdc', 'gnd' and 'vsource' from the Component Library by navigating to the 'Analog Parts' library. Figure 17 shows

the initial conditions to be set for the voltage sources and Figure 18 shows what your testbench schematic should look like at the end of this step.

00	X Edit Object Properties		••••	X Edit Object Properties	
		A	Apply To only cum	rent 🔽 instance 🔽	
Apply To Only curr	ent 🔽 instance 🔽		Show 📃 system	m 🗹 user 🗹 CDF	
Show 📃 system	m ⊻ user ⊻ CDF			(Development Labels Direlay)	
Browse	Reset Instance Labels Display		Pronerty	Value	Display
Property	Value	Display	Library Name	analootib	off
Library Name	analogLib	off 🔽	Endrary Ivanie	anarogarb	
Cell Name	vdc	off 🔽	Cell Name	vsource	
View Name	symbol	off	View Name	symbol	011
Instance Name	20 20	off 🗖	Instance Name	40	off
Instance Mane	*2			Add Delete Modify)
(Add Delete Modify		User Property	Master Value Local Value	Display
User Property	Master Value Local Value	Display	lvsignore	TRUE	off
Ivsignore	TRUE	off 🔽	L		
CDF Parameter	Value	Display	CDF Parameter	Value	Display
oise file name		off 🔽	DC voltage	900.0m V	off
umber of noise/freq pairs	0	off 🔽	Source type	dc 👻	off
C voltage	1.8 V	off	Display small signal params	s 📃	off
C magnitude		off	Display temperature params	s 🔲	off
Ciphase		off	Display noise parameters		off
F magnitude		off 🔽	Multiplier	1	off
AC magnitude		off			
AC phase		off			
emperature coefficient 1		off			
mperature coefficient 2		off 🗖 –			
OK Canc	el Apply Defaults Previous	Next Help	OK Canc	cel Apply Defaults Previous	Next He
	(a)			(b)	
	(a)			(0)	

Figure 17: Inserting Sources in Testbench



Figure 18: Designing the Testbench

4 Circuit Simulation Using Spectre

4.1 Launching ADE

- 1. We will simulate our circuits using Cadence Spectre Simulation engine. Spectre is a variant of HSPICE developed by Cadence and provides greater accuracy, speed and flexibility especially when dealing with mixed signal circuits thus we will use it as our preferred simulation engine in this course as well.
- 2. Make sure you first 'Check and Save' your testbench schematic and click on $Launch \rightarrow ADE$ to open up the ADE window as shown in Figure 19.
- 3. Click on $Setup \rightarrow Simulator$ to make sure the Simulator is set to Spectre as shown in Figure 19.



Figure 19: Simulating Circuit with ADE

4. Now click on $Setup \rightarrow Model \ Libraries$ to configure the Spectre model files. Figure 20 shows the path you need to browse to in order to get the correct model files for the PDK used in this course.

00	🔀 spectre0: Mode	el Library Setup	
Model File ⊡-Global Model Files └── C <click add<="" here="" th="" to=""><th>model file></th><th>Section</th><th></th></click>	model file>	Section	
		OK Cancel	Apply Help
	(a)		

0	S Spectre0: Model Library Setup	
_	Model File	Section
- Glo	bal Model Files	
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt
-	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_3v
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_na
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_3vna
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_m
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_3m
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_bip
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_bip3
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	dio
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	dio3
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	dio_dnw
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_res
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_mim
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfmos
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfmos33
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfmim
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfind
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfmvar
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfjvar
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfres_sa
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfres_rpo
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfres_hri
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_rfesd
	/home/EEAPPS/TSMC018/tsmc18rf//models/spectre/rf018.scs	tt_bbmvar
L[Click here to add model file>	

(b)

Figure 20: Configuring Model Files

4.2 DC Analysis

- 1. First simulation you will be exposed to is simulation of the DC operating point for the inverter you designed earlier.
- Click on AC,DC,Tran icon on the right pane of the ADE window and a window like Figure 21 should pop open. Choose 'dc' and under 'DC Analysis' save the the DC Operating point. <u>Note:</u> Make sure you keep the Enabled option checked off before you click on 'Ok'.
- 3. The output window should look like Figure 22 after you simulate the testbench by pressing the green 'Play' button on the right sidebar of ADE.
- 4. Suppose we want to now view the DC Operating points for the PMOS transistor in the inverter. In order to do so we need to descend into the schematic view from the testbench schematic.

First click on $Results \rightarrow Print \rightarrow DC$ Operating Points as shown in Figure 23. Now in order to descend into the actual schematic of the inverter and select the PMOS transistor we start off from the testbench schematic and click $Edit \rightarrow Hierarchy \rightarrow Descend Point \rightarrow Click$ on inverter symbol \rightarrow select PMOS. The complete steps are outlined in Figures 23, 24 and 25.

$\Theta \cap \cap X$	Choosing	Analyses	Virtuoso	Analog Desig	
Analysis	🔾 tran	🖲 dc	🔾 ac	🔾 noise	\square
	🔾 ×f	🔾 sens	\bigcirc dcmatch	🔾 stb	
	🔾 pz	🔾 sp	🔾 envlp	🔾 pss	
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf	
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise	
	🔾 qpxf	🔾 qpsp	🔾 hb	🔾 hbac	
	🔾 hbnois	e 🔾 hbsp			
		DC Ana	llysis		
Save DC O	perating Poi	nt 🗹			
Hysteresis :	Sweep				=
Sweep Va	riable				
Tempe	ratura				
Design	Variahla				
Compo	nent Parame	ter			
Model	Parameter				
	renemeter				
Enabled 🖌				Options	
		ок	ancel Det	aults Apply H	elp

Figure 21: Configuring DC Operating Point

<u>F</u> ile <u>H</u> elp	cādence
Peak resident memory used = 24.2 Mbytes.	
Time for EDB Visiting: CPU = 999 us, elapsed = 4 Time accumulated: CPU = 103.983 ms, elapsed = 16 Peak resident memory used = 24.5 Mbytes.	43,935 นร. 6.257 ms.
Circuit inventory: nodes 3 bsim3v3 2 vsource 2	
Time for parsing: CPU = 1 ms, elapsed = 2.65813 m Time accumulated: CPU = 104.983 ms, elapsed = 16 Peak resident memory used = 25.2 Mbytes.	ms. 9.126 ms.
Entering remote command mode using MPSC service	(spectre, ipi, v0.0, sj
Warning from spectre. WARNING (SPECTRE-16707): Only tran supports]	psfxl format, result o:
<pre>************************************</pre>	= 1.999 ms, elapsed = 5 5.525 ms.
dcOpInfo: writing operating point information to modelParameter: writing model parameter values to element: writing instance parameter values to ra outputParameter: writing output parameter values designParameVals: writing netlist parameters to ri primitives: writing primitives to rawfile. subckts: writing subcincuits to rawfile.	rawfile. o rawfile. wfile. to rawfile. awfile.

Figure 22: DC Operating Point Netlist Output

○ ○ ○ X Virtuoso® Analog	Design Environment (1) –	TestLib Tb_inv schematic	
Launch S <u>e</u> ssion Set <u>u</u> p <u>A</u> nalyses <u>V</u> ari	ables <u>O</u> utputs <u>S</u> imulation	<u>R</u> esults <u>T</u> ools <u>H</u> elp	cādence
Design Variables Name Value	Analyses Type Enable 1 dc V t	Plot Qutputs Direct Plot Print Annotate Vegtor Circuit Conditions Violations Display Reliability Data Save Select	DC Node Voltages DC Operating Points Model Parameters Transient Node Voltages Transient Operating Points Mismatch Summary Stability Summary
- Doutto in theme (retent for dames (simula	Outputs Name/Signal/Expr 1 Vout 2 Vin Plot after simulation: Auto	Printing/Plotting Options Printing/Plotting Options All All All All All All All All All Al	Capacitance Table S-Parameter Noise Parameters Noise Summary AC Distortion Summary PAC Distortion Summary HBAC Distortion Summary Pole-Zero Summary Sensitivities
> Results in /home/ratan1/cadence/simula	riot alter sinitiation.	Thotang mode. Hopice	MDL Measures
Mouse L:	M:		R: 10
4(10) DC Operating Points		Status: Ready T=27 C Sim	ulator: spectre 📈

Figure 23: Viewing DC Operating Point from ADE



Figure 24: Viewing DC Operating Point from ADE





(D)

000	X	Results Display Window	
Window	Expressions Info <u>H</u> elp		cādence
signal	OP("/IO/PO'	' "??")	A
betaeff cbb cbd cbdbi cbg cbsbi cdb cddbi cddbi cdd cdg cgbovl cgdbvl cggbvl cggbvl cggbi cgsbi cgsvi cgsbi cgsvi cgsbi cgsvi cgsbi cgsvi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgsbi cgbbi	$\begin{array}{c} 127u\\ 764, 5a\\ -284, 1a\\ -887, 8z\\ -55, 51a\\ -424, 8a\\ -4, 638a\\ -315, 9a\\ 484, 3a\\ -11, 44a\\ -290, 9a\\ 122, 5a\\ 4, 27a\\ 121z\\ -198, 8a\\ 3, 769a\\ 202, 5a\\ 637, 3a\\ 232, 1a\\ -442, 8a\\ -240, 3a\\ 202, 5a\\ 637, 3a\\ 232, 1a\\ -442, 8a\\ -240, 3a\\ 202, 5a\\ 232, 2a\\ -252, 5a\\ 233, 2a\\ 420, 2a\\ -452, 8a\\ -1, 44a\\ -290, 9a\\ 745, 2a\\ 122, 5a\\ 0\\ 0\\ \end{array}$		
14	40 70		

(c)

Figure 25: Final DC Operating Point Results

4.3 Parametric Sweep

- 1. Often we want to sweep across a parameter so in this section we will introduce parametric sweep in Cadence ADE by performing a DC parametric sweep across V_{source} .
- 2. In the testbench schematic click on 'Vsource' and press \mathbf{Q} to edit its properties. A window like Figure and Figure 26 (a) will pop up. Under the 'DC voltage' option type in 'Vgs' (this will be your sweep parameter). Make sure to click on 'Check and Save' and now in the ADE window click on Variables $\rightarrow Copy \ from \ Cellview$.
- 3. Click on the **AC**,**DC**,**Tran** icon on the right pane of the ADE window and follow the steps outlined in Figure 26. Under the same DC analysis window scroll down and follow the steps in Figure 27.



(c) Specify Sweep Parameter DC value

(d) Perform DC Sweep

Figure 26: DC Parametric Sweep of Vgs

4. Finally, click on Tools → Parametric Analysis (as shown in Figure 28)and a window like Figure 29 (a) will pop up. Follow the appropriate entries within this window as shown in

Figure 29 (a) and then proceed to steps outlined in 29 (b). Your final output for $g_m vs. V_{gs}$ for the NMOS transistor in the inverter will look like Figure 29 (c).

😑 🔿 🔿 📉 Choosing Analy	yses Virtuoso® Analog Desig
Hysteresis Sweep	
Sweep Variable	
🔲 Temperature 🗹 Design Variable	Variable Name Vgs
 Component Parameter Model Parameter 	Select Design Variable
Sweep Range	
● Start-Stop Start ○ Center-Span	0 Stop 1.8
Sweep Type	Step Size 0.1
Add Specific Points 📃	
Enabled 🖌	Options
ОК	Cancel Defaults Apply Help

Figure 27: DC Analysis Sweep Plan

000	X Virtuoso® A	nalog Desig	gn Enviro	nment (1	1) – 1	TestLib 1	Tb_inv	schen	natic		
Launch S <u>e</u> ssion	Set <u>u</u> p <u>A</u> nalyses	<u>V</u> ariables	<u>O</u> utputs	<u>S</u> imulati	ion <u>I</u>	<u>R</u> esults	<u>T</u> ools	<u>H</u> elp		cād	dence
I 💾 🧽 I 📭 🤇	27 🛛 🔊 🏅	• 🖄 🕑	1 🖻				<u>P</u> ara <u>R</u> F	ametric	Analysi	is	
Design Variables Name 1 Vgs	Value 1.8		alyses Type Er ⊻	t t			<u>C</u> alı Res <u>W</u> av Res <u>J</u> ob	culator ults <u>B</u> ro veform ults <u>D</u> is Monito	 iwser play ir		AC OC Trans
		Ou	itputs							?(
		- 1 Vo	Name/S out	ignal/Exp	r	Value	Plot	Save	Save allv	• Option	s 🕅
		2 Vi	n				<u> </u>	<u> </u>	allv		
> Results in /home	/ratan1/cadence/s	imula Plot	after simul	ation: A	uto		Plottin	ıg mode	: Repla	се	
≡mouse L:				M:							R:
4(10) Parametric A	nalysis					Status: R	eadv	T=27	c si	mulator:	spectre

Figure 28: Parametric Analysis on Vgs

00

0	0 0			X Par	ametric An	alysis – spe	ctre(0): TestLib	Tb_inv schemati	ic		
<u>E</u> ile	e <u>A</u> nalysis	<u>H</u> elp									cādence
	Ready	_	_		_	_					
1	8	🔊 🗙	\bigcirc	🛃 💷 🗕 Ru	ın Mode: Sw	eeps & Rang	es 🔽 📀 🤇				
Vas	Variable	Value	Sweep?	Range Type From/To	From	To	Step NRun S Linear Steps	elected Sweeps	Inclusion List	Exclusion List	
:			2			1					
28	Run Select	ed Sweeps									1
						40					

(a) Setting Parametric Analysis Plan



(b) Sweeping g_m across Vgs

(c) g_m v/s Vgs Output for NMOS Transistor

Figure 29: Parametric Analysis on Transistor Parameters

4.4 Transient Analysis

- 1. Transient analysis of any circuit is key to study the time domain behavior. In this section you will simulate the transient time domain responce of the inverter V_{out} , V_{in} and compute propagation delay using the in-built Calculator in ADE.
- 2. First open the testbench schematic and change the Vsource into a 'Pulse' type signal and configure it with the characteristics shown in Figure 30. Make sure you 'Check and Save' the schematic and now in ADE click on the **AC,DC,Tran** icon on the right pane. Choose the 'tran' simulation type, pick the stop time to be 10ns and choose 'moderate' in the 'Accuracy details'.
- 3. Click on the green 'Play' button to run the simulation and click on $Result \rightarrow Direct \ Plot$ to view the transient simulation plots.
- 4. In order to calculate the propagation delay of the inverter designed, in the ADE window click on $Tools \rightarrow Calculator$ and follow the instructions shown in Figure 31.
- 5. Finally, your propagation delay and the final transient simulation plot should look like Figure 32.

Browse	Reset Instance Labels Display					
Property	Value	Display				
Library Name a	nalogLib	off 🔽				
Cell Name 🛛 🛛	source	off 🔽				
View Name sy	ymbol	off 🔽				
Instance Name)	off 🔽				
Licer Dreparty	Add Delete Modify	Dianlau				
User Property	Master value Local value	Dispiay				
	IVE .					
CDF Parameter	Value	Display	$\Theta \cap \cap \mathbf{X}$	Choosing	Analyses Virtuos	® Analog
C voltage	Vgs V	off 🔽	Analysis	 tran 	⊖dc ⊖ac	 noise
ource type	pulse 🔻	off 🔽		⊖ ×f	🔾 sens 🔾 dcmatch	n 🔾 stb
Frequency name 1		off 🔽		🔾 pz	🔾 sp 🛛 🔾 envlp	🔾 pss
Delay time	100p s	off 🔽		🔾 pac	🔾 pstb 🔾 pnoise	🔾 pxf
/pe of rising & falling edge		off 🔽		🔾 beb	🔾 qpss 🔾 qpac	🔾 qpnoi
Zero value	0 4	off 🔽		⊖ qpxf	🔾 qpsp 🔾 hb	🔾 hbac
One value	1.8 ¥	off 🔽		 hbnoise 	O hbsp	
Period of waveform	2n s	off 🔽		1	Transient Analysis	
Rise time	100p s	off	Stop Time	10n		
Fall time	100p s	off	Accuracy	Defaults (err	preset)	
Pulse width	ln s	off	🗆 conse	rvative ⊻ m	noderate 🔲 liberal	
splay small signal params		off	Transla	- A blair -		
splay temperature params		off 🔽		nt NOISE		
		off 🔽	🗌 🗌 Dynami	c Parameter		
splay noise parameters						

Figure 30: Transient Simulation Setup

○ ○ ○ X Virtuoso® Analog	Design Environment (1) -	- TestLib	Tb_inv s	schema	atic	
Launch S <u>e</u> ssion Set <u>up A</u> nalyses <u>V</u> aria	ables <u>O</u> utputs <u>S</u> imulation	<u>R</u> esults	<u>T</u> ools <u>I</u>	<u>H</u> elp	cā	dence
I 🚰 🧽 I 🦵 27 🛛 💩 🎾 🖆	Dealwaas		<u>P</u> arar <u>R</u> F	metric A	Analysis	
Design Variables	Type Fnable		<u>C</u> alcu	ulator		AC COC
Name Value	1 dc ⊻ t		Resu	Its <u>B</u> row	vser	Trans
1 Vgs 1.8	2 tran 🗹 0 10n	moderate	<u>W</u> ave	eform		Ϋ́
			Resu	lts <u>D</u> isp	lay	
			<u>J</u> ob N	Monitor		~
	Outputs	L Malua	Dist	Cours I	Cause Outline	
	1 Vout	value		Jave a	ally ally	
	2 Vin		v 1	<u>→</u> a	allv	
> Results in /home/ratan1/cadence/simula	Plot after simulation: Auto		Plotting	mode:	Replace	
mouse L:	M:					R:
4(10) Calculator		Status: R	eady 1	T=27 (C Simulator	: spectre

(a)



(b)

Figure 31: Propagation Delay Calculation

XV	'irtuoso (R)	Visualizatio	on & Analysis	XL calcu	lator		
.s <u>∨</u> iew <u>O</u> ption	is <u>C</u> onstar	its <u>H</u> elp				cāder	nce
ontext Results DE	3: /home/ra	atan1/cadenc	e/simulation/Tb	_inv/spe	ctre/schematic	/psf	
Ovf Ovdc Oif Oidc	○ vs ○ is	⊖op ⊖v ⊖opt ⊖n	var 🔾 vn np 🔾 vn2	⊖ sp ⊖ zp	Ovswr O Oyp O	hp ⊖a gd ⊖ (zm data
Family 🔾 Wave	e 🗹 Clip) 🗫 🥀 ا	Append	Re	ectangular 🔽	🏟	B
9 / 6 * 3 -	9E-12	ert 🗐 🗊	à ∃≋ ≬ ≋	expr-	ME J	f<u>a</u> %	»
						_	đΧ
(?wf1 VT("/Vout" ar", ?nth2 1, ?td2 Vout") Vin")	'), ?value1 2 nil , ?stop	0.9, ?edge1 ' nil, ?multiple	'either", ?nth1 nil)	1, ?td1 O.	0, ?wf2 VT("/\	/in"), ?va	Jue2
Panel							ð×
nctions	- Q						
compression compressionVRI convolve cross d2a dBm	deriv dft dftbb dnl dutyCycle evmQAM	eyeDiagram fallTime flip fourEval freq freq_jitter	gainBwProd gainMargin getAsciiWave groupDelay harmonic harmonicFreq	iinteg integ intersect ipn ipnVRI loadpull	overshoot pavg peak peakToPeak period_jitter phaseMargin	pow prms psd psdbb pstddev pzbode	riseT rms rmsN root rshift
	S View Option ontext Results DE orf Orde If O	Virtuoso (R) S View Options Constart ontext Results DB: /home/ra ontext Results DB: // Output/ra ontext Results DB:	Virtuoso (R) Visualization View Options Constants Help ontext Results DB: /home/ratan1/cadenc vif vdc vs op v if idc is opt n Family Wave Clip Family Wave Clip 13.59E-12 3 4 2 2 2 3 4 4 2 2 3 4 3 4 3 4	Virtuoso (R) Visualization & Analysis s View Options Constants Help ontext Results DB: /home/ratan1/cadence/simulation/Tt vf vdc vs op var vn if oldc is opt mp vn2 Family Wave Clip A Append 13.59E-12 3 / 13.59E-12 3 / 13.59E-12 9 / 2 / 2 / 2 / 2 / 2 / 2 / 2 / 2 / 2 /	Nituoso (R) Visualization & Analysis XL calcu s View Options Constants Help ontext Results DB: /home/ratan1/cadence/simulation/Tb_inv/spect vf vdc vs op var vn sp vif vdc vs op var vn sp if idc is opt mp vn2 zp Family Wave ✓ Clip Append Re Re if idc is opt mp vn2 zp Family Wave ✓ Clip Append Re Re if idc is opt mp vn2 zp Family Wave ✓ Clip Append Re Re Re if vdc Ymax Re Re Re Re Re if vdc Re Re Re Re Re Re if vdc Re Re Re Re Re Re Re if vdc Re Re	Virtuoso (R) Visualization & Analysis XL calculator s View Options Constants Help ontext Results DB: /home/ratan1/cadence/simulation/Tb_inv/spectre/schematic vf vdc vs op var vn sp vswr if vide is opt mp vn2 zp yp Family Wave Clip A Append Rectangular Family Wave Clip A Append Rectangular 13.59E-12 13.59E-12 13.59E-12 13.59E-12 13.59E-12 13.59E-12 13.59E-12 13.702 Panel Interime 1, 7d2 nil, 7stop nil, 7multiple nil) Vout) Your) Panel compression deriv eyeDlagram gainBwProd linteg overshoot compression VRI dtt falTime gainMargin integ pavg convolve dtbb fourEval gainMargin parktoPeak cross dnl fourEval groupPleay ipn peaktoPeak groupPleay ipn peak	N Virtuoso (R) Visualization & Analysis XL calculator s View Options Constants Help cāder ontext Results DB: /home/ratan1/cadence/simulation/Tb_inv/spectre/schematic/psf vf vdc vs op var vn sp vswr hp z vf vdc vs op var vn sp vswr hp z vf vdc vs op var vn sp vswr hp z if idc is opt mp vn2 zp yp gd is Family Wave Clip Image: Append Rectangular Image: Append Rectangular Image: Append Image:

(a) Propagation Delay from Calculator



(b) Transient Analysis Output Plot

Figure 32: Propagation Delay and Transient Analysis Output