Design and Analysis of Redistribution Layer Interposer Channel Considering Signal Integrity for High Bandwidth Memory Module

Jiwon Yoon*, Hyunwook Park**, Hyunwoo Kim*, Boogyo Sim*, Jonghyun Hong*, Seongguk Kim*, Keeyoung Son*, Keunwoo Kim*, Yigyeong Kim***, Sujin Park***, Youngsu Kwon*** and Joungho Kim*
* School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Republic of Korea
** EMC Laboratory, Missouri University of Science and Technology (MST), Rolla, MO, USA
*** PIM AI HPU Group, Electronics and Telecommunications Research Institute (ETRI), Daejeon, Republic of Korea
jiwon.yoon@kaist.ac.kr

***Abstract*— In this paper, we designed and analyzed redistribution layer (RDL) interposer channels for high bandwidth memory (HBM) module. The physical dimensions and material properties were designed based on recent RDL process technology. We analyzed the electrical performance of the RDL interposer channels in terms of insertion loss and far-end crosstalk (FEXT) with comparison to silicon interposer. To verify the performance of RDL interposer channels, eye diagram simulation was conducted based on the HBM3 setup conditions. Conventional RDL interposer show improved performance in terms of IL, but shows significant FEXT at high frequencies. From eye diagram of interposer channels, RDL show high eye distortion due to the composite effect of crosstalk and voltage ringing. As a future projection, RDL interposer was designed and analyzed considering the rise in maturity of RDL based process. As a result, we have shown that with future advances in RDL fabrication technology, RDL interposer channels can successfully be utilized for HBM3 applications at a data rate of 6.4 Gb/s.**

***Index Terms*—High bandwidth memory, redistribution layer interposer, signal integrity, silicon interposer.**

I. INTRODUCTION

Recently, with the rapid growth of hyper-scale artificial intelligence (AI) models, the requirement for high computing power and memory bandwidth has continued to increase. To satisfy this demand, chip manufacturers begin to integrate processor and high bandwidth memory (HBM) on one package. High-density interconnection between the HBM and processor are realized through ultra-fine pitch interposer channels. Silicon is the most frequently used material for fabricating the interposer, with its mature fabrication technology. However, due to the high fabrication cost and low productivity of silicon, it is challenging to use silicon interposer for low cost, large-area applications [1].

An alternative solution to overcome the challenges of silicon interposer is redistribution layer (RDL) interposer, as shown in Fig. 1. Previous works have suggested the feasibility of RDL interposer as a substitute for silicon interposer [1]. Also, signal integrity (SI) analysis was conducted to guarantee high speed data transfer across the RDL interposer channels. However, previous works have focused on past generation HBM (HBM2), up to a data rate up to 3.2 Gb/s, which does not ensure SI at higher data rates of most recent HBM (HBM3) [1], [2]. In order to ensure the utilization of RDL interposer for its application to HBM3 module, it is essential to analyze RDL interposer channel considering most recent technology.

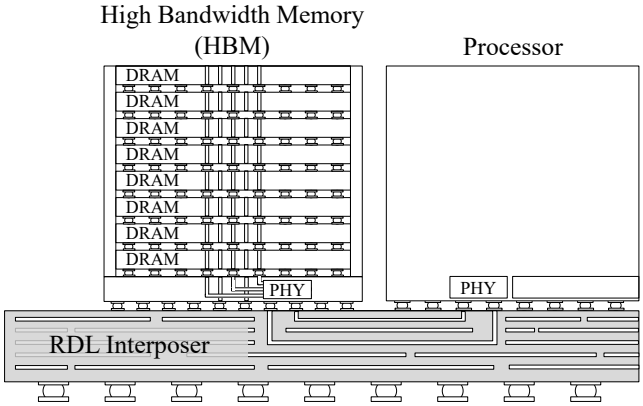

Fig. 1. Conceptual view of 2.5D integration method for HBM module using RDL interposer.

In this paper, we compared conventional silicon interposer channel and RDL interposer channel in terms of SI. The target application of this research is HBM3, with a data rate of 6.4 Gb/s [3]. Considering the conventional RDL fabrication process and stack-up of silicon interposer, interposer channels were designed with variance in physical dimensions and materials. In addition, as a future projection in RDL fabrication process, we assumed the fineness of RDL to be scaled down to that of silicon. Finally, the designed RDL interposer was analyzed in terms of insertion loss, far-end crosstalk (FEXT), and eye-diagram at a data rate of 6.4 Gb/s, to ensure its potential as a substitute for silicon interposer at HBM3 applications.

II. PROPOSED DESIGN OF RDL INTERPOSER CHANNEL

In this section, silicon and RDL interposer channels are designed. Fig. 2 shows the stack-up of interposer channels, The physical dimensions and material properties of silicon and RDL interposer channels are shown in Table. 1, based on previous works [2], [4], [5]. Two metal layers in the form of microstrip and stripline are utilized for signal routing, and adjacent metal pattern layers are ground and power layers in the form of a mesh [3]. The minimum required pitch of a single channel is designed to have a width/space (w/s) value of 2 μm,

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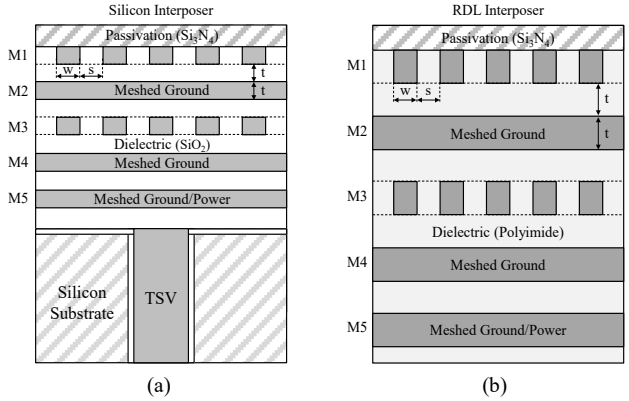

Fig. 2. Stack-up of 6-layer (a) silicon interposer and (b) RDL interposer channels for HBM module.

which ensures all the signal channels to be fully routed across the interposer between the bump field. Each channel is assumed to have an equal length of 5 mm considering the physical dimensions of HBM3 module.

The difference in fabrication process of silicon and RDL interposer are considered in terms of physical dimensions and material properties. Compared to RDL, silicon interposer has finer conductor and dielectric layers, using silicon process [1], [2]. Also, RDL interposer uses polymer based dielectric material [5], [6]. For this work, we assumed the thickness of RDL to be 3 μm, to reflect the relatively thick fabrication of RDL process [7]. As a future projection considering the rise in maturity of RDL process, we assumed the thickness of RDL will be scaled down to that of silicon.

III. Signal Integrity Analysis of Proposed RDL Interposer Channel

Fig. 3 shows the simulation results of interposer channels. S-parameter analysis was conducted in terms of insertion loss and FEXT using 3D EM simulation tool (ANSYS HFSS). Simulated results of insertion loss are shown in Fig. 3(a). At the Nyquist frequency ($f_{nyquist}$), RDL interposer channel layers show lower values of insertion loss. Compared to silicon interposer, insertion loss is decreased at microstrip, and stripline by 1.6 dB and 2.9 dB, respectively. This is due to low conductor loss caused by the thicker RDL. As the thickness is scaled down to 1 μm, RDL show similar conductor loss at low frequencies, and slightly lower levels of dielectric loss than silicon at higher frequencies, due to the lower effective permittivity of polymer substrate.

TABLE I
Physical Dimensions and Material Properties of Interposer Channels

	Channel Width/Space	Conductor & Dielectric Thickness	Dielectric Material Properties
Silicon	2 μm / 2 μm	1 μm	SiO_2 (ε_r = 4.1, tanδ = 0.001)
RDL (Conventional)	2 μm / 2 μm	3 μm	Polyimide (ε_r = 3.3, tanδ = 0.004)
RDL (Scaled-down)	2 μm / 2 μm	1 μm	Polyimide (ε_r = 3.3, tanδ = 0.004)

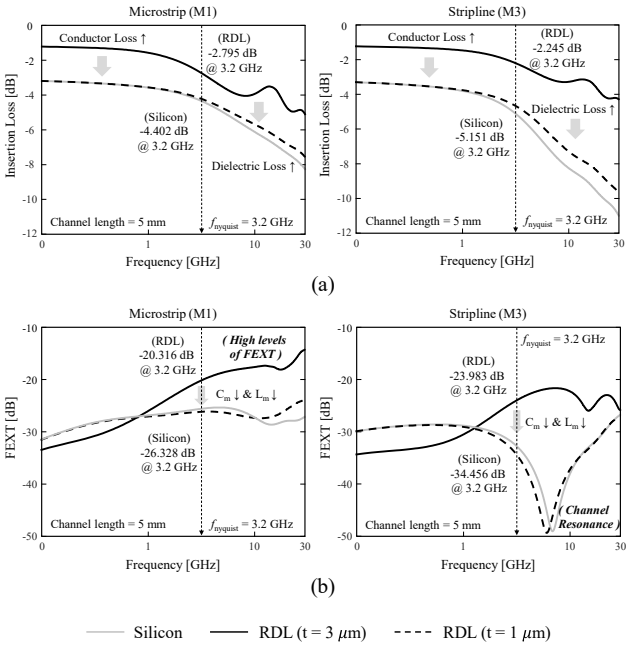

Fig. 3. Simulated (a) insertion loss and (b) FEXT of silicon and RDL interposer channels.

Simulated results of FEXT are shown in Fig. 3(b). RDL interposer channels show high levels of FEXT compared to silicon interposer, especially at microstrip with 20.3 dB. This is due to the thicker conductor layers of channel and dielectric compared to the spacing between adjacent channels, which does not ensure return current path. Also, at high frequency ranges above $f_{nyquist}$, FEXT is dominated by high capacitive coupling between adjacent channels. As the RDL is scaled down to that of silicon, FEXT is significantly suppressed due to lower mutual inductance and capacitance between adjacent channels, especially at RDL stripline showing a value of 34.5 dB with the effect of channel resonance.

Electrical characteristics of RDL interposer channels were verified through eye diagram simulation based on the data rate of HBM3 I/O interface. To fully consider crosstalk which have an effect on a single victim channel, 8 aggressor channels were taken into account for eye simulation. The eye diagram simulation setup is shown in Fig. 4 with Tx/Rx conditions assumed as simplified RC circuit parameters calculated based on HBM3 JEDEC [3]. The simulated eye diagrams of interposer channels are shown in Fig. 5. Compared to silicon, RDL interposer show high levels of eye distortion, in terms of eye height voltage and voltage overshoot. As shown in Fig. 5(a) and (b), the eye height of RDL microstrip and stripline are decreased

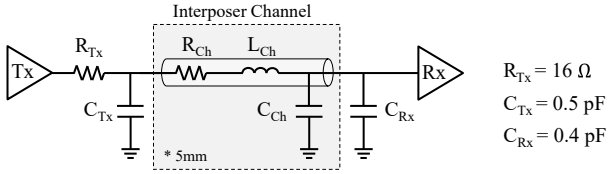

Fig. 4. Simplified RLC model of interposer channel with Tx/Rx conditions of HBM3 interface

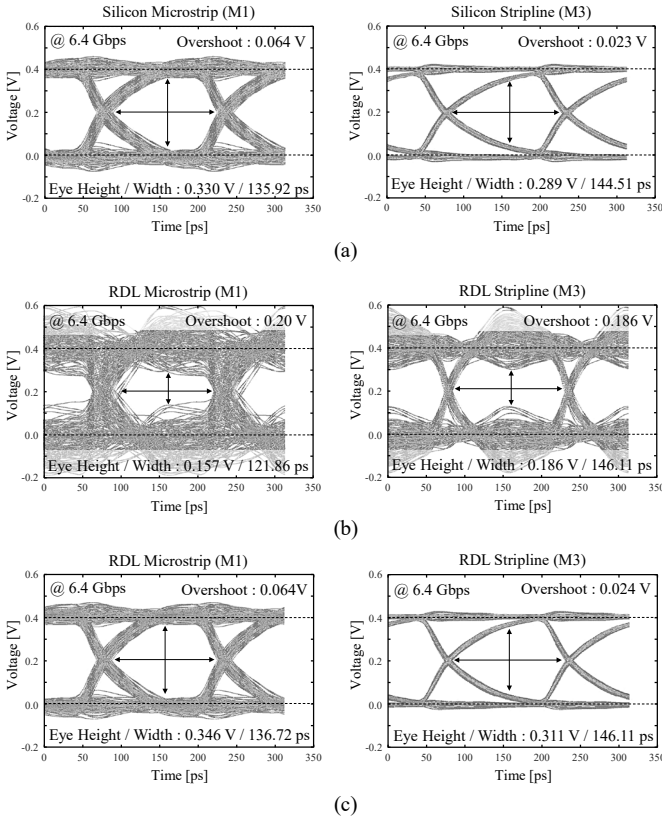

Fig. 5. Simulated eye diagrams of (a) silicon interposer, (b) RDL interposer (t = 3 μm) and (c) RDL interposer with scaled thickness (t = 1 μm).

by 0.17 V and 0.10 V compared to that of silicon. This is due to the high levels of coupled voltage ringing from aggressor lines, with significant levels of FEXT above at high frequencies. To consider the composite effect of crosstalk and voltage ringing, the damping properties of interposer channel was derived. [8] Each channel was assumed as a simplified RLC circuit as shown in Fig. 4, where the values of R_{ch}, C_{ch}, L_{ch} of the channel were extracted using a 3D EM solver (ANSYS Q3D). The damping factor (ζ) of the interposer channel is calculated using the following equation

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \quad (1)$$

$$(R = R_{Tx} + R_{ch},\ C = C_{ch} + C_{Rx},\ L = L_{ch})$$

The extracted RLC values and the calculated damping factor (ζ) of interposer channels are summarized at Table. II. An RLC system is considered to be underdamped when the damping ratio is below 1. From the simulated eye diagram results, it can be seen that RDL interposer channels show highly underdamped properties with a low damping ratio under 0.3, which lead to high levels of overshoot. As the thickness of RDL metal layer is scaled to 1 μm, R_{ch} is increased by 12.6 Ω at microstrip and 8.1 Ω at stripline. The increase in R_{ch} leads to higher damping ratio of 0.436 and 0.580 at microstrip and stripline, respectively. This results in suppressed voltage overshoot due to higher levels of damping, showing similar eye diagrams to that of silicon. This ensures the use of RDL interposer for HBM3 applications operating at a data rate of 6.4 Gb/s.

TABLE II
EXTRACTED RLC PARAMETERS OF INTERPOSER CHANNEL AND DAMPING FACTOR

		R_{ch} [Ω]	L_{ch} [nH]	C_{ch} [pF]	Damping Factor (ζ)
Silicon (t = 1 μm)	M1	27.415	2.835	1.360	0.464
	M3	21.231	1.352	1.744	0.624
RDL (t = 3 μm)	M1	14.828	3.790	1.285	0.295
	M3	13.133	2.461	1.236	0.335
RDL (t = 1 μm)	M1	27.415	2.835	1.182	0.436
	M3	21.231	1.352	1.493	0.580

IV. CONCLUSION

In this paper, we designed RDL interposer channel for HBM module by comparison with silicon interposer. The design was analyzed in terms of insertion loss, FEXT and verified through eye diagram. From frequency domain simulation results, conventional RDL interposer channels show improved performance in terms of insertion loss, but have higher levels of FEXT due to mutual coupling especially at microstrip. Eye diagram results of conventional RDL interposer show high levels of eye distortion from the composite effect of crosstalk and voltage ringing from underdamped channel properties. As the physical dimensions of RDL are scaled down to silicon based dimensions, simulated results show improved electrical performance in terms of eye opening and voltage overshoot, which ensures SI at RDL interposer channel for its application at HBM3 module.

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