## Semiconductor Technology Trends

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Chip size (mm²)</strong></td>
<td>300</td>
<td>430</td>
<td>520</td>
<td>750</td>
</tr>
<tr>
<td><strong>Number of transistors (million)</strong></td>
<td>11</td>
<td>76</td>
<td>200</td>
<td>1400</td>
</tr>
<tr>
<td><strong>Interconnect width (nm)</strong></td>
<td>200</td>
<td>100</td>
<td>70</td>
<td>35</td>
</tr>
<tr>
<td><strong>Total interconnect length (km)</strong></td>
<td>2.16</td>
<td>2.84</td>
<td>5.14</td>
<td>24</td>
</tr>
</tbody>
</table>
The Interconnect Bottleneck

<table>
<thead>
<tr>
<th>Technology Generation</th>
<th>MOSFET Intrinsic Switching Delay</th>
<th>Response Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 µm</td>
<td>~ 10 ps</td>
<td>~ 1 ps</td>
</tr>
<tr>
<td>0.01 µm</td>
<td>~ 1 ps</td>
<td>~ 100 ps</td>
</tr>
</tbody>
</table>
The Interconnect Bottleneck

SPEED/PERFORMANCE ISSUE

- Gate Delay
- Sum of Delays, Al & SiO2
- Sum of Delays, Cu & Low K
- Interconnect Delay, Al & SiO2
- Interconnect Delay, Cu & Low K

Gate wi Al & SiO2

- Gate

Al $3.0 \, \mu \Omega \cdot \text{cm}$
Cu $1.7 \, \mu \Omega \cdot \text{cm}$
SiO2 $\kappa = 4.0$
Low $\kappa = 2.0$
Al & Cu $0.8 \mu$ Thick
Al & Cu Line $43 \mu$ Long

Delay (ps)

Generation (nm)
Chip-Level Interconnect Delay

Pulse Characteristics:
- rise time: 100 ps
- fall time: 100 ps
- pulse width: 4 ns

Line Characteristics
- length: 3 mm
- near end termination: 50 Ω
- far end termination: 65 Ω
Interconnect

- Total interconnect length ($\text{m/cm}^2$) – active wiring only, excluding global levels will increases:

<table>
<thead>
<tr>
<th>Year</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Length</td>
<td>579</td>
<td>688</td>
<td>907</td>
<td>1002</td>
<td>1117</td>
<td>1401</td>
<td>1559</td>
</tr>
</tbody>
</table>

- Interconnect power dissipation is more than 50% of the total dynamic power consumption in 130nm and will become dominant in future technology nodes

- Interconnect centric design flows have been adopted to reduce the length of the critical signal path
Metallic Conductors

\[ R = \frac{\text{Length}}{\sigma \text{ Area}} \]

Package level:
- \( W=3 \) mils
- \( R=0.0045 \ \Omega/\text{mm} \)

Submicron level:
- \( W=0.25 \) microns
- \( R=422 \ \Omega/\text{mm} \)
Integration & Signal Speed

Before

Today

I(t)

current

time

I(t)

current

time
Signal Integrity

Ideal

Transmission Channel

Common

Transmission Channel

Noisy

Transmission Channel
Signal Degradation
Modeling Interconnections

Low Frequency

Mid-range Frequency

High Frequency

Transmission Line

Lumped Reactive CKT

Short
WAVE PROPAGATION

Wavelength: \( \lambda \)

\[
\lambda = \frac{\text{propagation velocity}}{\text{frequency}}
\]
Why Transmission Lines?

In Free Space

At 10 KHz: $\lambda = 30$ km

At 10 GHz: $\lambda = 3$ cm

Transmission line behavior is prevalent when the structural dimensions of the circuits are comparable to the wavelength.
Transmission Line Model

Let $d$ be the largest dimension of a circuit

If $d \ll \lambda$, a lumped model for the circuit can be used
Transmission Line Model

If \( d \approx \lambda \), or \( d > \lambda \) then use transmission line model
Frequency Components of Digital Signal

\[ C_0 \times \quad + \quad \]
\[ C_1 \times \quad + \quad \]
\[ C_2 \times \quad + \quad \]
\[ C_3 \times \quad + \quad \]
\[ C_4 \times \]
RC Network

\[ A = \frac{v_o(f)}{v_i(f)} \]

The gain falls to 0.707 of its low-frequency value at the frequency \( f_2 \). \( f_2 \) is the upper 3-dB frequency or the 3-dB bandwidth of the RC network.
RC Network

\[ v_o = V \left(1 - e^{-t/RC}\right) \]
RC Network

Rise time: \( t_r = t_{90\%} - t_{10\%} \)

\[
\begin{align*}
   t_r &= 2.2 \cdot R \cdot C = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2}
\end{align*}
\]

**Observation:** Simulating a 1-ns rise-time step requires a 3-dB bandwidth in the order of 350 MHz.

**Rule of thumb:** A 1-ns pulse requires a circuit with a 3-dB bandwidth of the order of 2 GHz.
Frequency Dependence of Lumped Circuit Models

At higher frequencies, a lumped circuit model is no longer accurate for interconnects and one must use a distributed model. Transition frequency depends on the dimensions and relative magnitude of the interconnect parameters.

\[ f \approx \frac{0.3 \cdot 10^9}{10d \sqrt{\varepsilon_r}} \quad t_r \approx \frac{0.35}{f} \]
Lumped Circuit or Transmission Line?

A) Determine frequency or bandwidth of the signal

- **Microwave**: $f = \text{operating frequency}$

- **Digital**: $f = \frac{0.35}{\text{rise time}}$

B) Determine propagation velocity in medium, $v$, next calculate wavelength $\lambda = \frac{v}{f}$
Lumped Circuit or Transmission Line?

C) Compare wavelength with dimensions (feature size) d.

**Case 1:** If $\lambda \gg d$ use lumped circuit equivalent

- Total inductance = $L \times \text{length}$
- Total capacitance = $C \times \text{length}$

**Case 2:** If $\lambda \approx 10d$ or $\lambda < 10d$, use transmission-line model
# Frequency Dependence of Lumped Circuit Models

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Frequency</th>
<th>Rise time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Printed circuit line (epoxy, glass)</td>
<td>10 in</td>
<td>&gt;55 MHz</td>
</tr>
<tr>
<td>Package lead frame (ceramic)</td>
<td>1 in</td>
<td>&gt;400 MHz</td>
</tr>
<tr>
<td>VLSI interconnection* (silicon)</td>
<td>100 μm</td>
<td>&gt;8 GHz</td>
</tr>
</tbody>
</table>

* Using RC criterion for distributed effect
Connector Design

• Minimize physical length of connector pins.

• Maximize the ratio of power and ground pins to the signal pins. If possible these ratios should be < 1.

• Place each signal pin as close as possible to a current return pin.

• Place power pins adjacent to ground pins.
8-Bit Connector Pin-Out Options

inferior

improved

More improved

Optimal
A chip has a 2-μm-long data bus of 0.6-μm wires on 1.2μm centers. Use the table values. Assume that the perpendicular wires on adjacent layers are all grounded. Each driver can be modeled as a voltage source in series with a 1-kΩ resistor. All lines switch simultaneously to random states. What is the worst-case maximum and minimum delay of a line.

<table>
<thead>
<tr>
<th>Description</th>
<th>Capacitance</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vertical parallel-plate capacitance</td>
<td>0.05</td>
<td>fF/μm²</td>
</tr>
<tr>
<td>Vertical parallel-plate capacitance (minimum width)</td>
<td>0.03</td>
<td>fF/μm</td>
</tr>
<tr>
<td>Vertical fringing capacitance (each side)</td>
<td>0.01</td>
<td>fF/μm</td>
</tr>
<tr>
<td>Horizontal coupling capacitance (each side)</td>
<td>0.03</td>
<td>fF/μm</td>
</tr>
</tbody>
</table>
A chip has a 2-μm-long data bus of 0.6-μm wires on 1.2μm centers. Use the table values. Assume that the perpendicular wires on adjacent layers are all grounded. Each driver can be modeled as a voltage source in series with a 1-kΩ resistor. All lines switch simultaneously to random states. What is the worst-case maximum and minimum delay of a line.
The resistance of the wires are much smaller than the 1kΩ of the drivers and thus can be ignored.

Worst case condition which will cause maximum delay is when the effective capacitance is maximum. If the 2 side aggressor lines transition in the opposite direction of the main driver on the victim line, this will create the most amount of capacitance (Miller effect).
Typical TL Parameters and Coupling Coefficients

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>Electrical Parameters</th>
<th>Coupling Coefficients</th>
</tr>
</thead>
<tbody>
<tr>
<td>W  S  H</td>
<td>C  C_m  L  M  Z</td>
<td>k_{cx}  k_{lx}  k_{fx}  k_{rx}</td>
</tr>
<tr>
<td>8  8  6</td>
<td>88  6.4  355  57.5  63</td>
<td>0.068  0.162  -0.047  0.058</td>
</tr>
<tr>
<td>8  8  3</td>
<td>137  3.0  240  18.5  42</td>
<td>0.021  0.077  -0.028  0.025</td>
</tr>
<tr>
<td>8  16  6</td>
<td>87  2.0  356  28.7  64</td>
<td>0.023  0.081  -0.029  0.026</td>
</tr>
<tr>
<td>8  16  3</td>
<td>136  1.0  240  8.2  42</td>
<td>0.007  0.034  -0.013  0.010</td>
</tr>
<tr>
<td>8  8  6*</td>
<td>148  6.6  302  13.4  45</td>
<td>0.043  0.044  0.000  0.022</td>
</tr>
<tr>
<td>8  8  3*</td>
<td>233  1.2  191  1.0  29</td>
<td>0.005  0.005  0.000  0.003</td>
</tr>
<tr>
<td>8  16  6*</td>
<td>147  1.3  302  2.6  45</td>
<td>0.008  0.009  0.000  0.004</td>
</tr>
<tr>
<td>8  16  3*</td>
<td>233  0.3  191  0.2  29</td>
<td>0.001  0.001  0.000  0.001</td>
</tr>
</tbody>
</table>
Example

Full-swing (3.3V) CMOS signal with a fast 500 ps rise time next to a low-swing (300 mV) signal for a 10 cm run of microstrip line. The lines are each 8 mils wide spaced 6 mils above a ground plane and spaced 8 mils from one another (see previous Table). Is the noise induced in the low-swing line a concern?

- From table, we get $k_{fx} = -0.047$, $k_{rx} = 0.058$

Far end crosstalk

$$C = C + C_m = 88 + 6.4 = 94.4 \text{ pF/m}$$

$$L = 355 \text{ nH/m}$$

$$v = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{94.4 \text{ pF/m} \times 355 \text{nH/m}}} = 1.73 \times 10^8 \text{ m/s}$$

$$t_x = \frac{10 \text{ cm}}{1.73 \times 10^8} = 0.578 \text{ ns}$$
Example

In worst case, near- and far-end crosstalk will be added

\[ V_{x_{\text{talk}}} = k_{fs} \times t_x \times \frac{\Delta V_{\text{aggressor}}}{\Delta t} + \Delta V_{\text{aggressor}} \times k_{rx} \times k_r \]

\[ = 0.047 \times 0.578 \text{ns} \times \frac{3.3}{500 \text{ps}} + 3.3 \times 0.058 \times 1 = 0.37 \text{ V} \]

0.37 V is bigger than 300 mV/2=150 mV \(\Rightarrow\) This will cause problem to the system

Victim line also produces crosstalk on the aggressor. However, only second order effect is considered.
Signaling Conventions

• A good signaling convention isolates a signal from noise to provide noise immunity.

• Most signaling conventions in common use are based on standards and are actually quite poor.

• Many modern systems define their own signaling conventions rather than employ the standards.
Transmission Systems

Full-swing CMOS transmission system

Low-swing current-mode transmission system
# Transmission Systems

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>LSC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Signaling</strong></td>
<td>Voltage mode: 0=GND, 1=V\textsubscript{dd}</td>
<td>Current mode: 0=-3.3 mA, 1=+3.3 mA</td>
</tr>
<tr>
<td><strong>Reference</strong></td>
<td>Power supply: V\textsubscript{r}~V\textsubscript{dd}/2</td>
<td>Self-centered: I\textsubscript{r}=0 mA</td>
</tr>
<tr>
<td><strong>Termination</strong></td>
<td>Series terminated in output impedance of driver</td>
<td>Parallel-terminated at receiver with R\textsubscript{T} within 10% of Z\textsubscript{o}</td>
</tr>
<tr>
<td><strong>Signal energy</strong></td>
<td>1.3 nJ</td>
<td>22 pJ</td>
</tr>
<tr>
<td><strong>Power dissipation</strong></td>
<td>130 mW</td>
<td>11 mW</td>
</tr>
<tr>
<td><strong>Noise immunity</strong></td>
<td>1.2:1 actual:required signal swing (with LSC receiver)</td>
<td>3.6:1</td>
</tr>
<tr>
<td><strong>Delay</strong></td>
<td>18 ns</td>
<td>6 ns</td>
</tr>
</tbody>
</table>
# Transmission Systems

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>LSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>0.3</td>
<td>165</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>0.0</td>
<td>-165</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>2.2</td>
<td>10</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>1.1</td>
<td>-10</td>
</tr>
<tr>
<td>$V_{MH}$</td>
<td>1.1</td>
<td>155</td>
</tr>
<tr>
<td>$V_{ML}$</td>
<td>1.1</td>
<td>155</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>LSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receiver sensitivity</td>
<td>300</td>
<td>10</td>
</tr>
<tr>
<td>Receiver offset</td>
<td>250</td>
<td>10</td>
</tr>
<tr>
<td>Power supply noise</td>
<td>300</td>
<td>3</td>
</tr>
<tr>
<td>Total noise (swing-independent)</td>
<td>850</td>
<td>23</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>LSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Self-induced power supply noise ($K_{in}$)</td>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>Crosstalk from other signals ($K_{xt}$)</td>
<td>250</td>
<td>10</td>
</tr>
<tr>
<td>Reflections of the same signal from previous clock cycles ($K_r$)</td>
<td>large($&gt;$5)</td>
<td>5</td>
</tr>
<tr>
<td>Transmitter offset ($K_{to}$)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Total proportional noise fraction ($K_N$)</td>
<td>&gt;35</td>
<td>25</td>
</tr>
</tbody>
</table>
CMOS vs LSC

• With the worst-case combinations of noise sources the CMOS signaling system will fail.

• The LSC system has 3.6 times the signal swing required.

• The transmission delay of the LSC system is the one-way delay of the transmission line.

• The CMOS driver must wait for the line to ring up to the full voltage.
CMOS vs LSC

• Basic CMOS system is most commonly used and yet is far from optimal

• Large energy signal is used where it is not needed

• Transmitted signal not isolated from supply noise

• Receiver uses reference that changes significantly with process variations
Signaling Modes for Transmission Lines

- Signal return impedances $Z_{RT}$ and $Z_{RR}$
- Coupling to local power supply $Z_{GT}$ and $Z_{GR}$
- Introduce noise $V_N$
- Sections can be separated if TL is terminated into match impedance
Transmitter Signaling Parameters

• Output impedance, $R_o$

• Coupling between signal and power supply $Z_{GT}$

• Polarity of signal

• Amplitude of signal
Current-Mode Transmission

\[ V(t, x) = I_T \left( t - \frac{x}{v} \right) Z_o \]

Provides isolation of both the signal and current return from the local power supplies

- Large \( Z_{GT} \)
Voltage-Mode Transmission

\[ V(t, x) = V_T \left( t - \frac{x}{v} \right) \]

Makes a difference in:
- Signal return crosstalk
- Single power supply noise
Current- & Voltage-Mode Transmission

Current-Mode Transmission

Output impedance $>> Z_o$

Voltage-Mode Transmission

Output impedance $<< Z_o$
Transmitter Signal-Return Crosstalk

• A signal return path is typically shared among a group of N signals (typically 2 to 8) to reduce cost.
• Sharing occurs at both ends of line.
• $Z_{RT}$ approximates the return path impedance at the transmitter end.
• The return current from all N transmission lines passes through impedance $Z_{RT}$.
• The current $I_{T1} = V_{T1}/Z_0$ sees the shared return impedance in parallel with the series combination of the line and output impedances from other signals.
• The total return impedance is $Z_X$. 
Transmitter Signal Return Crosstalk

With voltage-mode signaling, $R_o=0$, the transmitter signal return crosstalk is a maximum. For current-mode signaling, $R_o$ is infinite and this form of crosstalk is eliminated.
Receiver Signal Return Crosstalk

\[ K_{XRR} = \frac{(N-1)Z_{RR}}{(N-1)Z_{RR} + 2Z_o} \leq \frac{(N-1)Z_{RR}}{2Z_o} \]

- All N terminators return their current through \( Z_{RR} \) (shared impedance)

- No crosstalk advantage to current-mode signaling

- TL is like a matched source
Power Supply Noise

\[ V_{RN} = V_N \left[ \frac{Z_O Z_R}{2Z_O Z_R + (2Z_O + Z_R) Z_N} \right] \quad \text{if } Z_R \ll Z_o \]

\[ V_{RN} = \frac{V_N Z_R}{2(Z_R + Z_N)} \]

To reject power supply noise, \( Z_N = Z_{GT} + Z_{GR} \) must be made as large as possible. This is accomplished by using a current-mode transmitter.
Nonideal Return Paths

- A nonideal return path will appear as an inductive discontinuity
- A nonideal return path will slow the edge rate by filtering out high-frequency components
- If the current divergence path is long enough, a nonideal return path will cause signal integrity problems at the receiver
- Nonideal return paths will increase current loop area and exacerbate EMI
- Nonideal return paths may significantly increase the coupling coefficient between signals
Signal Return Crosstalk

- Return crosstalk can be reduced with rise-time control
- As rise times get faster, every signal requires its own return \( \Rightarrow \) might as well use differential signaling
- With voltage-mode signaling, the transmitter signal return crosstalk is a maximum
- High output impedance offers advantage and reduces transmitter return crosstalk
- For current-mode signaling, this form of crosstalk is completely eliminated
Application: Return Signal Optimization

Voltage-mode signaling with $Z_o=50 \ \Omega$ and rise time $t_r=2 \ \text{ns}$ and $Z_{RT}$ dominated by 5 nH inductance.

Approximate $Z_{RT}=L/t_r = 2.5 \ \Omega$
Want $k_{XRT} = 0.1$

Solving for $N$ shows that we will need 1 return for every 3 signal traces to meet the spec.

If the rise time is decreased to 1 ns, we will need 1 return for every 2 signal line to keep the same spec.

If the rise time is lower than 1 ns, we will need 1 return for every signal ➔ might as well use differential signaling
Signaling Over Lumped RLC Interconnect

\[ \omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \]

\[ V_R(t) = 1 - \exp\left(-\frac{RT}{2L}\right)\cos(\omega t) \]

\[ Q = \frac{1}{\pi R} \sqrt{\frac{L}{C}} \]
Example

Determine the amount of supply noise $V_N$ that appears across $R_T$ as a function of frequency. How much signal swing is required to keep the power-supply noise less than 10% of the signal swing across the spectrum from DC to 1GHz.

- $Z_O = R_T = 50\, \Omega$
- $R_O = 1\, \text{k}\, \Omega$
- $C_N = 5\, \text{pF}$
- $L_R = 5\, \text{nH}$
- $V_N = 500\, \text{mV}$
Example

$$V_{RN} = \frac{V_N(Z_O j\omega L_R)}{2Z_O j\omega L_R + (2Z_O + j\omega L_R)(j\omega C)^{-1}}$$

$$= \frac{V_N 4\pi^2 Z_O L_R C f^2}{8\pi^2 Z_O L_R C f^2 + 2Z_O + 2\pi f L_R}$$

$$= \frac{-2.5 \times 10^{-18} f^2}{-98.5 \times 10^{-18} f^2 + 100 + j31.4 \times 10^{-9} f}$$

We want 0.1 $V_s > V_{RN} \Rightarrow V_s > 10V_{RN}$
Required Voltage Swing
Ringback and Rise Time Control

- Violation into threshold region
- Detrimental even if threshold is not crossed
- Can exacerbate ISI
- Can be aggravated by nonlinear (time varying) terminations
- Can increase skew between signals
Voltage Reference Uncertainty

Major Contributors

- Power supply effects (SSN, ground bounce, rail collapse)
- Noise from IC
- Receiver transistor mismatches
- Return path discontinuities
- Coupling to reference voltage circuitry
Efficient Bus Design Methodology

- Spreadsheets & metrics
- Signal categories
- Topology options
- Sensitivity analysis
- Routing guidelines
- Reference design
- Simulation of design
- Design check
- Tapeout

Flowchart:
- Pass to Tapeout
- Fail to Design check
- Fix to Reference design
- Reference design to Buffer guidelines
- Buffer guidelines to Signal categories
Bus System Variables

- I/O capacitance
- Trace length, velocity, and impedance
- Interlayer impedance variations
- Buffer strengths and edge rates
- Termination values
- Receiver setup and hold times
- Interconnect skew specifications
- Package, daughtercard, and parameters
Differential vs Single-Ended

Line impedance: \( Z_o = 50 \) \( \Omega \)
Source Resistance: \( R_o = 50 \) \( \Omega \)
Lead Inductance: \( L = 5 \) nH
Pin count: \( P = 32 \)
Data rate: \( TBR = 8GB/s \)

\[
S + N = P
\]
\[
S \times B = TBR
\]

\[
K_{XRT} \leq \frac{(N-1)Z_{RT}}{R_o + Z_o}
\]

\( Z_{RT} \) is due to the lead inductance
\( Z_{RT} \to Z_{RT}/N \) since there are \( N \) ground pins
Need to determine \( S \) and \( N \)

B: Bit rate per signal pin
TBR: Total bit rate
S: Number of signal pins
N: Number of return pins
Coupled Transmission Lines

\[ V_1, I_1, C_s, C_m, L_m, V_2, I_2, \varepsilon_T, h, w, s \]
Even Mode

\[- \frac{\partial V_e}{\partial z} = (L_{11} + L_{12}) \frac{\partial I_e}{\partial t} \]
\[- \frac{\partial I_e}{\partial z} = (C_{11} + C_{12}) \frac{\partial I_e}{\partial t} \]

Add voltage and current equations

\[V_e : \text{Even mode voltage} \quad V_e = \frac{1}{2}(V_1 + V_2)\]

\[I_e : \text{Even mode current} \quad I_e = \frac{1}{2}(I_1 + I_2)\]

\[Z_e = \frac{\sqrt{L_{11} + L_{12}}}{\sqrt{C_{11} + C_{12}}} = \sqrt{\frac{L_s + L_m}{C_s}} \quad \text{Impedance}\]

\[v_e = \frac{1}{\sqrt{(L_{11} + L_{12})(C_{11} + C_{12})}} = \frac{1}{\sqrt{(L_s + L_m)C_s}} \quad \text{velocity}\]
Odd Mode

\[-\frac{\partial V_d}{\partial z} = (L_{11} - L_{12}) \frac{\partial I_d}{\partial t}\]

\[-\frac{\partial I_d}{\partial z} = (C_{11} - C_{12}) \frac{\partial I_d}{\partial t}\]

V_d : Odd mode voltage

\[V_d = \frac{1}{2}(V_1 - V_2)\]

I_d : Odd mode current

\[I_d = \frac{1}{2}(I_1 - I_2)\]

\[Z_d = \sqrt{\frac{L_{11} - L_{12}}{C_{11} - C_{12}}} = \sqrt{\frac{L_s - L_m}{C_s + 2C_m}}\]

\[V_d = \frac{1}{\sqrt{(L_{11} - L_{12})(C_{11} - C_{12})}} = \frac{1}{\sqrt{(L_s - L_m)(C_s + 2C_m)}}\]

Impedance velocity
Mode Excitation

EVEN

ODD
PHYSICAL SIGNIFICANCE OF EVEN- AND ODD-MODE IMPEDANCES

* $Z_e$ and $Z_d$ are the wave resistance seen by the even and odd mode travelling signals respectively.

* The impedance of each line is no longer described by a single characteristic impedance; instead, we have

\[
V_1 = Z_{11} I_1 + Z_{12} I_2 \\
V_2 = Z_{21} I_1 + Z_{22} I_2
\]
Definitions

**Even-Mode Impedance: \( Z_e \)**
Impedance seen by wave propagating through the coupled-line system when excitation is symmetric \((1, 1)\).

**Odd-Mode Impedance: \( Z_d \)**
Impedance seen by wave propagating through the coupled-line system when excitation is anti-symmetric \((1, -1)\).

**Common-Mode Impedance: \( Z_c = 0.5Z_e \)**
Impedance seen by a pair of line and a common return by a common signal.

**Differential Impedance: \( Z_{diff} = 2Z_d \)**
Impedance seen across a pair of lines by differential mode signal.
Mutual Impedances

$Z_{11}, Z_{22} : \text{Self Impedances}$

$Z_{12}, Z_{21} : \text{Mutual Impedances}$

For symmetrical lines,

$Z_{11} = Z_{22}$ and $Z_{12} = Z_{21}$
Even and Odd Modes

\[ V_d = \frac{1}{\sqrt{(L_s - L_m)(C_s + 2C_m)}} \]
\[ Z_d = \sqrt{\frac{L_s - L_m}{C_s + 2C_m}} \]

\[ V_e = \frac{1}{\sqrt{(L_s + L_m)C_s}} \]
\[ Z_e = \sqrt{\frac{L_s + L_m}{C_s}} \]

*In general, odd-mode impedance is smaller than even-mode impedance.*

*In general, odd-mode velocity is larger than even-mode velocity.*
Coupled Lines

Line Space

\[ V_1 = Z_{11} I_1 + Z_{12} I_2 \]

\[ V_2 = Z_{21} I_1 + Z_{22} I_2 \]

\[
\begin{bmatrix}
V_1 \\
V_2 \\
\end{bmatrix} =
\begin{bmatrix}
Z_{11} & Z_{12} \\
Z_{21} & Z_{22} \\
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2 \\
\end{bmatrix}
\]

Modal Space

\[ V_e = Z_e I_e \]

\[ V_d = Z_d I_d \]

\[
\begin{bmatrix}
V_e \\
V_d \\
\end{bmatrix} =
\begin{bmatrix}
Z_e & 0 \\
0 & Z_d \\
\end{bmatrix}
\begin{bmatrix}
I_e \\
I_d \\
\end{bmatrix}
\]
Example - Microstrip

**Single Line**
- Dielectric height = 6 mils
- Width = 8 mils

\[ \varepsilon_r = 4.3 \]
\[ Z_s = 56.4 \, \Omega \]

**Coupled Lines**
- Height = 6 mils
- Width = 8 mils
- Spacing = 12 mils

\[ \varepsilon_r = 4.3 \]
\[ Z_e = 68.1 \, \Omega \quad Z_d = 40.8 \, \Omega \]
\[ Z_{11} = 54.4 \, \Omega \quad Z_{12} = 13.6 \, \Omega \]
Even Mode

\[ I_{tdr} = \left[ \frac{a_e(t,0)}{Z_e} + \frac{a_d(t,0)}{Z_d} \right] + \left[ \frac{a_e(t,0)}{Z_e} - \frac{a_d(t,0)}{Z_d} \right] \]

\[ V_{tdr} = a_e(t,0) - a_d(t,0) \quad a_{d}(t,0) = 0 \]

\[ \frac{V_{tdr}}{I_{tdr}} = \frac{Z_e}{2} \quad Z_e = 2\left( \frac{1+\rho_e}{1-\rho_e} \right)Z_g \quad v_e = \frac{2l}{\tau_e} \]
Odd Mode

\[ V_{tdr} = a_e(t,0) + a_d(t,0) - \left[ a_e(t,0) - a_d(t,0) \right] = V_f + V_b \]

\[ I_{tdr} = \left[ \frac{a_e(t,0)}{Z_e} + \frac{a_d(t,0)}{Z_d} \right] \]

\[ I_{tdr} = -\left[ \frac{a_e(t,0)}{Z_e} - \frac{a_d(t,0)}{Z_d} \right] \]

\[ a_e(t,0) = 0, \quad \frac{V_{tdr}}{I_{tdr}} = 2Z_d \]

\[ Z_d = \frac{1}{2} \left( \frac{1 + \rho_d}{1 - \rho_d} \right) Z_g, \quad V_d = \frac{21}{\tau_d} \]
Measured Even-Mode Velocity

![Graph showing measured even-mode velocity vs. spacing (mils)]
Measured Odd-Mode Velocity

<table>
<thead>
<tr>
<th>Spacing (mils)</th>
<th>v_d (m/μs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.175</td>
</tr>
<tr>
<td>6</td>
<td>0.18</td>
</tr>
<tr>
<td>8</td>
<td>0.185</td>
</tr>
<tr>
<td>10</td>
<td>0.19</td>
</tr>
<tr>
<td>12</td>
<td>0.195</td>
</tr>
<tr>
<td>14</td>
<td>0.20</td>
</tr>
<tr>
<td>16</td>
<td>0.205</td>
</tr>
<tr>
<td>18</td>
<td>0.21</td>
</tr>
</tbody>
</table>

**Odd-Mode Velocity**

- h=3 mils
- h=5 mils
- h=7 mils
- h=10 mils
- h=14 mils
- h=21 mils
Even and Odd-Mode Impedances

Typical Even & Odd Mode Impedances

Distance (mils)
Measured Odd-Mode Impedance

Odd-Mode Impedance

- h=3 mils
- h=5 mils
- h=7 mils
- h=10 mils
- h=14 mils
- h=21 mils
Measured Even-Mode Impedance

![Graph showing measured even-mode impedance for different values of 'h' spacing.]
Virtual Reference Plane

For odd modes, there exists a virtual reference plane between the conductors.

Electric field is perpendicular to virtual plane.

Magnetic field is tangent to virtual plane.

Virtual reference plane.
Low-Voltage Differential Signaling (LVDS)

Definition: Method to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces or a balanced cable

Criteria for high-performance communication

- Bandwidth
- Low Power
- Low Noise

Solution exists for very short and very long distances; however for board-to-board or box-to-box, this is a challenge
Why LVDS?

1. Differential transmission is less susceptible to common mode noise

2. Consequently they can use lower voltage swings

3. In PC board (microstrip) odd-mode propagation is faster
LVDS Attributes for EMI

1. Low output voltage swing
2. Slow edge rates
3. Odd-mode operation (magnetic fields cancel)
4. Soft output corner transitions
- Majority of current flows across 100-ohm resistor
- Switching changes the direction of current
- Logic state determined by current direction
LVDS Standard

• **Maximum Switching Speed**
  – Depends on line driver
  – Depends on selected media (type and length)

• **LVDS Saves Power**
  – Power dissipated in load is small
  – LVDS devices are in CMOS=>low static power
  – Lowers system power through current-mode

• **Design Practices**
  – Matching is critical
  – Preserve balance
## Differential Signaling Technologies

<table>
<thead>
<tr>
<th>Parameter</th>
<th>RS-422</th>
<th>PECL</th>
<th>LVDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Driver Output Voltage</td>
<td>±2 to ±5V</td>
<td>±600-1000 mV</td>
<td>±250-450 mV</td>
</tr>
<tr>
<td>Receiver Input Threshold</td>
<td>±200 mV</td>
<td>±200-300mV</td>
<td>±100 mV</td>
</tr>
<tr>
<td>Data Rate</td>
<td>&lt;30Mbps</td>
<td>&gt;400Mbps</td>
<td>&gt;400Mbps</td>
</tr>
<tr>
<td>Supply Current Quad Driver (no load, static)</td>
<td>60 mA (max)</td>
<td>32-65mA (max)</td>
<td>8.0mA</td>
</tr>
<tr>
<td>Supply Current Quad Receiver (no load, static)</td>
<td>23mA (max)</td>
<td>40mA (max)</td>
<td>15mA (max)</td>
</tr>
<tr>
<td>Propagation Delay of Driver</td>
<td>11ns (max)</td>
<td>4.5ns (max)</td>
<td>1.7ns (max)</td>
</tr>
<tr>
<td>Propagation Delay of Receiver</td>
<td>30ns (max)</td>
<td>7.0ns (max)</td>
<td>2.7ns (max)</td>
</tr>
<tr>
<td>Pulse Skew (Driver or Receiver)</td>
<td>N/A</td>
<td>500ps (max)</td>
<td>400ps (max)</td>
</tr>
</tbody>
</table>