Clock Jitter Insensitive, Linear Analog-to-Digital Converters

Timir Nandi

29th Apr, 2016
ADCs are Part of Our Life

Analog signal input → ADC → DSP → DAC → Analog signal output

- Analog to digital converter
- Digital Signal Processor
- Digital to analog converter
ADC Metrics: Resolution

Resolution ⇔ Number of bits used to represent the analog input

Step size = \( \Delta \)

\[
\Delta = \frac{V_{\text{REF}}}{2^N} = \frac{10}{2^3} = 1.25
\]

Quant. Noise Power

\[
E_q = \frac{\Delta^2}{12}
\]

ADC Metrics: Sampling Rate

- The rate at which the signal is sampled

Nyquist theorem: Sampling rate > 2 * Signal Bandwidth
**DAC Pulse Shape : Non Return to Zero**

NRZ DAC is inherently nonlinear (rise-fall asymmetry)
DAC Pulse Shape: Return to Zero

\[ \frac{T_{\text{rise}} - T_{\text{fall}}}{T_s} = 1\% \]

\[ \text{HD}_2 \approx 55\text{dB (SE NRZ)} \]

\[ I_{\text{mis}} = 4\% (\text{diff}), \text{HD}_2 \approx 85\text{dB} \]
Return to Zero DAC Circuitry

- Charge transferred = \((0.5T_s)I_o\)
Effect of Clock Jitter on RZ DAC

- Jitter randomly shifts clock edges
- Varying width current pulse
- Error in the charge transferred to the loop filter
Switched Capacitor (SC) DAC

- Capacitors are charged to \( \pm V_{\text{ref}} \) during \( \Phi_1 \)
- DAC is not connected to the loop filter, \( I_{\text{DAC}} = 0 \)
**SC DAC (Discharging Phase)**

- Capacitors are discharged into the loopfilter during $\Phi_2$
- Charge transferred = $\pm CV_{\text{ref}}$

![Diagram of SC DAC](image-url)
**Effect of Clock Jitter on SC DAC**

- Transfers most of the charge in a short period
- Error due to clock jitter is smaller \((CV_{\text{ref}})\)
**SC DAC vs RZ DAC**

- DAC output peak current is higher

(a) RZ DAC waveform  
(b) SC DAC waveform
**SC DAC vs RZ DAC**

- Higher demands on the linearity of the loop filter
Introducing the SCRZ DAC

- **RZ DAC**
  - Excellent linearity
  - High jitter sensitivity

- **SC DAC**
  - Low jitter sensitivity
  - Poor linearity

- **SCRZ DAC**
Introducing the SCRZ DAC

DAC currents

Opamp inputs
**SCRZ DAC operation ($\Phi_1$)**

![Diagram of SCRZ DAC operation](image)
SCRZ DAC operation ($\Phi_1$)
SCRZ DAC operation ($\Phi_2$)
**SCRZ DAC operation** \((\Phi_2 = 0.5T_s)\)

\[
I_o = CV_{\text{ref}} / (0.5T_s)
\]

\[V_{xy} = 0\]
SCRZ DAC operation ($\Phi_3$)
SCRZ DAC operation ($\Phi_3$)
Summary: Ideal Waveforms

- With an ideal clock
- With ideal current $I_o = \frac{CV_{\text{ref}}}{0.5T_s}$
  - $I_{\text{dac}}$ has an RZ pulse shape
Effect of jitter

- Ideal – $\phi_2$ half clock cycle wide
- Jittered - $0.5T_s + \tau$
Effect of jitter

I_{dac} lasts longer than 0.5T_s

V_{xy} < 0 at end of $\phi_2$
Waveforms ($\Phi_3$)

$V_{xy} = 0$ at the end of $\Phi_3$

$I_{dac}$ is negative in $\Phi_3$
**Total DAC Charge**

\[ Q_{dac} = C(V_{xy, initial} - V_{xy, final}) \]
Total DAC Charge

Irrespective of Jitter!

\[ A_1 - A_2 = CV_{ref} \]
Role of current source

- Shapes the capacitor discharge pulse
- Smaller peak current
- Relaxed requirement - linearity of the loop filter

(a) SCRZ Waveform
(b) SC Waveform
Non ideality - Deviation of $I_o$

- $I_o(0.5T_s) = CV_{\text{ref}}$
- $I_{o,d} = 2CV_{\text{ref}}/T_s$
- Capacitors completely discharged at the end of $\Phi_2$
- $I_{\text{dac}} = 0$ during $\Phi_3$
If $I_o < I_{o,d}$

- Capacitors are incompletely discharged
- The residual charge is discharged during $\Phi_3$
- $I_{dac}$ is positive during $\Phi_3$
- Net charge supplied by the DAC remains $\pm CV_{\text{ref}}$
If $I_o > I_{o,d}$

- Capacitors are over discharged
- The capacitors are charged during $\Phi_3$
- $I_{dac}$ is negative during $\Phi_3$
- Net charge supplied by the DAC remains $\pm CV_{ref}$

![Graph showing $V_{xy}$ and $I_{dac}$ over time, with labeled sections for $0$, $0.25$, $0.5$, and $1$.]
Tune $I_o$

- $I_o = I_{o,d}$, $V_{xy} = 0$
- $V_{xy} < 0$, $I_o > I_{o,d}$
Tune $I_o$

- Comparator - sign of $V_{xy}$ at the end of $\Phi_2$
- Control $I_o$ to 6-bit accuracy
Target Modulator Specifications

- Signal Bandwidth = 2 MHz
- Sampling frequency = 256 MHz
- Quantizer range = $3.6 \, V_{pp,d}$
- Target resolution = 14 Bits
- 0.18 $\mu$m CMOS process
Chip layout and test board
Test set up

Bandpass Filter (BPS01P00-B)

Signal source (Agilent-33250A)

Transformer (ADT1-1WT)

Test board

DUT (ADC)

Clock source (Centellax TG1C1A)

Oscilloscope (DSO80204B)

MATLAB

Computer
PSD of modulator

Clock jitter
~ 1 ps rms

SCRZ mode (SNDR 82.3 dB)
RZ mode (SNDR 64.1 dB)

PSD (dBFS)

Frequency (MHz)
Controlled jitter experiment

**FM Modulation**
- Signal Generator
  - Agilent 33250A
- Clock source
- Modulator

**Test Board**

**FM modulated sampling clock**

\[
\cos \left( 2\pi f_s t + A \cos(2\pi f_m t) \right)
\]

Chosen so that RMS jitter is 50 ps

60 MHz
PSD of modulator (jittery clock)
Conclusions

- Conventional feedback DACs have problems
  - NRZ DAC: Rise-fall asymmetry
  - RZ DAC: Jitter sensitivity
  - SC DAC: Poor linearity

- The SC-RZ DAC
  - Good marriage of the SC and RZ DACs

- A high performance CTDSM incorporating an SC-RZ DAC
  - 87 dB DR in a 2MHz bandwidth
  - 16.6mW in a 180nm CMOS process